OVERVIEW

The 7051 series are 80 to 320MHz oscillator frequency, LV-PECL output, SPXO module IC with 125°C operating temperature. The output circuit used LV-PECL logic.

The 7051 series have achieved a low phase noise characteristic and small chip size allowing crystal oscillator modules to be implemented 3225 package.

FEATURES

- Operating supply voltage range: 2.375 to 3.63V
- Recommended oscillation frequency range (varies with version)
  - 80MHz to 320MHz fundamental oscillation (Ax, B1 ver.)
  - 105MHz to 170MHz 3rd overtone oscillation (M1, N1 ver.)
- -40 to 125°C operating temperature range
- LV-PECL output
- Oscillation detection circuit built-in
- Frequency divider built-in: Selectable by version: f0, f0/2, f0/4
- Standby function: High impedance in standby mode, oscillator stops
- Power-saving pull-up resistor built-in (INHN pin)
- Wafer form (WF5051xx)
- Chip form (CF5051xx)
- Phase noise characteristics (typ): -130dBc/Hz (A1 version, 1kHz offset, f=122.88MHz (γ=330, C0=1.6pF))
- -155dBc/Hz (A1 version, 10MHz offset, f=122.88MHz)
- RMS jitter (typ): 0.15ps (A1 version, 12kHz to 20MHz, f=122.88MHz)
- Application: Base station, SONET/SDH, Ethernet, Fibre Channel, LTE

SERIES CONFIGURATION

<table>
<thead>
<tr>
<th>Oscillation mode</th>
<th>Recommended oscillation frequency range f0 [MHz]</th>
<th>Output frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>f0</td>
<td>f0/2</td>
</tr>
<tr>
<td>fundamental</td>
<td>80 to 180</td>
<td>7051A1</td>
</tr>
<tr>
<td></td>
<td>180 to 320</td>
<td>7051B1</td>
</tr>
<tr>
<td>3rd overtone</td>
<td>105 to 130</td>
<td>7051M1*2</td>
</tr>
<tr>
<td>fundamental</td>
<td>130 to 170</td>
<td>7051N1*2</td>
</tr>
</tbody>
</table>

*1. Recommended values based on IC characteristics.
   The oscillator characteristics are determined by the combination of crystal element and the IC, hence the actual oscillator is not limited to these values. Always conduct thorough circuit evaluation beforehand.
   The recommended characteristics for the crystal element are R1 < 20Ω, C0 < 2.0pF.

*2. M1, N1 are available for 3rd overtone oscillation. The recommended characteristics for the crystal element are R1<60Ω, C0<2.0pF.*

*3. Versions in parentheses ( ) are under development.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Version Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>WF7051xx-4</td>
<td>Wafer form</td>
<td>WF7051□□-4</td>
</tr>
<tr>
<td>CF7051xx-4</td>
<td>Chip form</td>
<td></td>
</tr>
</tbody>
</table>
The CF7051/WF7051 incorporated standard PECL output schemes, which are un-terminated emitters.

**PIN DESCRIPTION and PAD COORDINATES**

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>I/O*</th>
<th>Function</th>
<th>PAD coordinates [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INHN</td>
<td>I</td>
<td>Output enable input. With pull-up built-in. Refer to page 6 for INHN function.</td>
<td>X: -350  Y: -370</td>
</tr>
<tr>
<td>2</td>
<td>XTN</td>
<td>O</td>
<td>Crystal connection pins</td>
<td>X: -350  Y: -194</td>
</tr>
<tr>
<td>3</td>
<td>XT</td>
<td>I</td>
<td>Crystal is connected between XIN and XOUT.</td>
<td>X: -350  Y: 34</td>
</tr>
<tr>
<td>4</td>
<td>VDD</td>
<td>-</td>
<td>(+) supply voltage</td>
<td>X: -142  Y: 370</td>
</tr>
<tr>
<td>5</td>
<td>OUTN</td>
<td>O</td>
<td>LV-PECL output pin (differential inverted output)</td>
<td>X: 83  Y: 370</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
<td>O</td>
<td>LV-PECL output pin (differential output)</td>
<td>X: 313  Y: 370</td>
</tr>
<tr>
<td>7</td>
<td>VSS</td>
<td>-</td>
<td>(-) ground</td>
<td>X: 350  Y: -355</td>
</tr>
</tbody>
</table>

*1. I: Input pin  O: Output pin
## ABSOLUTE MAXIMUM RATINGS

V<sub>SS</sub>=0V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage range&lt;sup&gt;1&lt;/sup&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Between VDD and VSS&lt;sup&gt;2&lt;/sup&gt;</td>
<td>-0.3 to +5.0</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage range&lt;sup&gt;1&lt;/sup&gt;&lt;sup&gt;2&lt;/sup&gt;</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>XT, INHN</td>
<td>-0.3 to VDD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage range&lt;sup&gt;1&lt;/sup&gt;&lt;sup&gt;2&lt;/sup&gt;</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>XTN, OUT, OUTN</td>
<td>-0.3 to VDD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Junction temperature&lt;sup&gt;3&lt;/sup&gt;</td>
<td>T&lt;sub&gt;j&lt;/sub&gt;</td>
<td>-</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range&lt;sup&gt;4&lt;/sup&gt;</td>
<td>T&lt;sub&gt;STG&lt;/sub&gt;</td>
<td>Chip form, Wafer form</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

<sup>1</sup> Parameters must not exceed ratings, not even momentarily. If a rating is exceeded, there is a risk of IC failure, deterioration in characteristics, and decrease in reliability.

<sup>2</sup> V<sub>DD</sub> is a V<sub>DD</sub> value of recommended operating conditions.

<sup>3</sup> Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

<sup>4</sup> When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

## RECOMMENDED OPERATING CONDITIONS

V<sub>SS</sub>=0V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating supply voltage</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Between VDD and VSS&lt;sup&gt;2&lt;/sup&gt;</td>
<td>2.375</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>INHN</td>
<td>0</td>
<td>-</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Ta</td>
<td>-40</td>
<td>-</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Output load</td>
<td>R&lt;sub&gt;L&lt;/sub&gt;</td>
<td>V&lt;sub&gt;1.8&lt;/sub&gt;-2V termination</td>
<td>49.5</td>
<td>50.0</td>
<td>50.5</td>
<td>Ω</td>
</tr>
<tr>
<td>Oscillator frequency&lt;sup&gt;1&lt;/sup&gt; (fundamental)</td>
<td>f&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>7051Ax</td>
<td>80</td>
<td>-</td>
<td>180</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7051B1</td>
<td>180</td>
<td>-</td>
<td>320</td>
<td>MHz</td>
</tr>
<tr>
<td>Oscillator frequency&lt;sup&gt;1&lt;/sup&gt; (3&lt;sup&gt;rd&lt;/sup&gt; overtone)</td>
<td>f&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>7051M1</td>
<td>105</td>
<td>-</td>
<td>130</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7051N1</td>
<td>130</td>
<td>-</td>
<td>170</td>
<td>MHz</td>
</tr>
</tbody>
</table>

<sup>1</sup> The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

<sup>2</sup> Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 7051 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.
ELECTRICAL CHARACTERISTICS

DC Characteristics

Measurement circuits 1 to 5 in “Conditions” are shown in Page 7 to 9 “MEASUREMENT CIRCUITS.”

V_{DD}=2.375 to 3.63V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption (Ax ver.)</td>
<td>I_{DDA}</td>
<td>Measurement circuit 1, V_{DD}-2V termination, INHN=Open</td>
<td>-</td>
<td>60</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>Current consumption (B1 ver.)</td>
<td>I_{DB}</td>
<td>Measurement circuit 1, V_{DD}-2V termination, INHN=Open</td>
<td>-</td>
<td>63</td>
<td>90</td>
<td>mA</td>
</tr>
<tr>
<td>Current consumption (M1 ver.)</td>
<td>I_{DM}</td>
<td>Measurement circuit 1, V_{DD}-2V termination, INHN=Open</td>
<td>-</td>
<td>60</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>Current consumption (N1 ver.)</td>
<td>I_{DN}</td>
<td>Measurement circuit 1, INHN=V_{SS}, oscillator :disabled, outputs :disabled, T_a=25°C</td>
<td>-</td>
<td>60</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>Standby Current</td>
<td>I_{STB}</td>
<td>Measurement circuit 1, INHN=V_{SS}, oscillator :disabled, outputs :disabled, T_a=25°C</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>HIGH-level output voltage</td>
<td>V_{OH}</td>
<td>Measurement circuit 5, OUT/OUTN</td>
<td>V_{DD}-1.025</td>
<td>V_{DD}-0.950</td>
<td>V_{DD}-0.880</td>
<td>V</td>
</tr>
<tr>
<td>LOW-level output voltage</td>
<td>V_{OL}</td>
<td>Measurement circuit 5, OUT/OUTN</td>
<td>V_{DD}-1.810</td>
<td>V_{DD}-1.700</td>
<td>V_{DD}-1.620</td>
<td>V</td>
</tr>
<tr>
<td>Output leakage current</td>
<td>I_{Z}</td>
<td>Measurement circuit 3, INHN=LOW, OUT/OUTN, T_a=25°C</td>
<td>-1</td>
<td>-</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>HIGH-level input voltage</td>
<td>V_{IH}</td>
<td>Measurement circuit 2, INHN</td>
<td>0.7V_{DD}</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>LOW-level input voltage</td>
<td>V_{IL}</td>
<td>Measurement circuit 2, INHN</td>
<td>-</td>
<td>-</td>
<td>0.3V_{DD}</td>
<td>V</td>
</tr>
<tr>
<td>Power save Pull-up resistance</td>
<td>R_{PU1}</td>
<td>Measurement circuit 2, INHN=V_{SS}</td>
<td>1</td>
<td>3</td>
<td>14</td>
<td>MΩ</td>
</tr>
<tr>
<td>Pull-up resistance</td>
<td>R_{PU2}</td>
<td>Measurement circuit 2, INHN=0.7V_{DD}</td>
<td>50</td>
<td>100</td>
<td>200</td>
<td>kΩ</td>
</tr>
<tr>
<td>Oscillator feedback resistance (Ax ver.)</td>
<td>R_{FA}</td>
<td>Measurement circuit 4, XT-XTN</td>
<td>8</td>
<td>17.5</td>
<td>40</td>
<td>kΩ</td>
</tr>
<tr>
<td>Oscillator feedback resistance (B1 ver.)</td>
<td>R_{FB}</td>
<td>Measurement circuit 4, XT-XTN</td>
<td>8</td>
<td>17.5</td>
<td>40</td>
<td>kΩ</td>
</tr>
<tr>
<td>Oscillator feedback resistance (M1 ver.)</td>
<td>R_{FM}</td>
<td>Measurement circuit 4, XT-XTN</td>
<td>1</td>
<td>1.75</td>
<td>3</td>
<td>kΩ</td>
</tr>
<tr>
<td>Oscillator feedback resistance (N1 ver.)</td>
<td>R_{FN}</td>
<td>Measurement circuit 4, XT-XTN</td>
<td>1</td>
<td>1.75</td>
<td>3</td>
<td>kΩ</td>
</tr>
<tr>
<td>Oscillator capacitance (Ax ver.)</td>
<td>C_{GA}</td>
<td>Design value, excluding parasitic capacitance</td>
<td>3.0</td>
<td>4.0</td>
<td>5.0</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (Ax ver.)</td>
<td>C_{DA}</td>
<td></td>
<td>4.5</td>
<td>6.0</td>
<td>7.5</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (B1 ver.)</td>
<td>C_{GB}</td>
<td>Design value, excluding parasitic capacitance</td>
<td>1.5</td>
<td>2.0</td>
<td>2.5</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (B1 ver.)</td>
<td>C_{DB}</td>
<td></td>
<td>2.2</td>
<td>3.0</td>
<td>3.8</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (M1 ver.)</td>
<td>C_{GM}</td>
<td>Design value, excluding parasitic capacitance</td>
<td>3.0</td>
<td>4.0</td>
<td>5.0</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (M1 ver.)</td>
<td>C_{DM}</td>
<td></td>
<td>5.2</td>
<td>7.0</td>
<td>8.8</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (N1 ver.)</td>
<td>C_{GN}</td>
<td>Design value, excluding parasitic capacitance</td>
<td>1.5</td>
<td>2.0</td>
<td>2.5</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator capacitance (N1 ver.)</td>
<td>C_{DN}</td>
<td></td>
<td>5.2</td>
<td>7.0</td>
<td>8.8</td>
<td>pF</td>
</tr>
</tbody>
</table>

*1. Confirmed by acceptance sampling using wafer monitor pattern.
### AC Characteristics

Measurement circuits 5 and 6 in “Conditions” are shown in page 9 to 10 “MEASUREMENT CIRCUITS.”

The conditions for each parameter assume the timing shown in “Timing Diagram.”

V_{DD}=2.375 to 3.63V, V_{SS}=0V, Ta=-40 to +125°C unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duty cycle</td>
<td>Duty1</td>
<td>Measured at output crossing point, Ta=25°C, V_{DD}=3.3V, measurement circuit 5</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Duty2</td>
<td>Measured at 50% output amplitude, Ta=25°C, V_{DD}=3.3V, measurement circuit 5</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Output amplitude</td>
<td>V_{OPP}</td>
<td>Peak-to-peak output waveform, measurement circuit 5, single-ended output signal</td>
<td>0.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output rise time</td>
<td>t_r</td>
<td>20 to 80% output amplitude, measurement circuit 5, single-ended output signal</td>
<td>-</td>
<td>0.3</td>
<td>1.0</td>
<td>ns</td>
</tr>
<tr>
<td>Output fall time</td>
<td>t_f</td>
<td>20 to 80% output amplitude, measurement circuit 5, single-ended output signal</td>
<td>-</td>
<td>0.3</td>
<td>1.0</td>
<td>ns</td>
</tr>
<tr>
<td>Output disable propagation delay</td>
<td>t_{OD}</td>
<td>Ta=25°C, design value, measurement circuit 6</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>ns</td>
</tr>
</tbody>
</table>

*1. Output rise time and output fall time may vary depending on measurement environment.

**Notes**

- The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.
- Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.
- The recommended crystal element characteristics are R<sub>1</sub> < 20Ω and C<sub>0</sub> < 2.0pF (Fundamental).
- The recommended crystal element characteristics are R<sub>1</sub> < 60Ω and C<sub>0</sub> < 2.0pF (3rd overtone).

### Timing Diagram

The timing diagram applies to the “Conditions” in the table in “AC Characteristics.”

\[
\text{Duty1} = \frac{t_w}{t_{PER}} \times 100 \% \text{ @ Crossing Point}
\]

\[
\text{Duty2} = \frac{t_w}{t_{PER}} \times 100 \% \text{ @ 50\% Waveform}
\]

*1. On an INHN falling edge, the outputs go high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) has elapsed. When this occurs, the output signal is pulled down to V_T (termination voltage) by the load resistance. On an INHN rising edge, the output starts after the output enable propagation delay (t_{OE}) has elapsed.
FUNCTIONAL DESCRIPTION

INHN Function

<table>
<thead>
<tr>
<th>INHN (pull-up resistance built-in)</th>
<th>Oscillator</th>
<th>Output stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH/Open</td>
<td>Operating</td>
<td>Operating</td>
</tr>
<tr>
<td>LOW</td>
<td>Disabled</td>
<td>Disabled (Hi-Z)</td>
</tr>
</tbody>
</table>

**Power Saving Pull-up Resistor**

The INHN terminal pull-up resistance switches between $R_{PU1}$ and $R_{PU2}$, depending on the input level (HIGH or LOW).

When the INHN terminal is held LOW, the built-in INHN terminal pull-up resistance increases ($R_{PU1}$), reducing the current consumed by the pull-up resistance when the outputs are disabled.

When the device is operating with the INHN terminal HIGH or open circuit, the pull-up resistance decreases ($R_{PU2}$), reducing internal susceptibility to the effects of external noise. The INHN terminal is held HIGH internally to prevent problems that might otherwise cause the outputs to stop abruptly.

**Oscillator Startup Detection Function**

An oscillator startup detection circuit is built-in. The circuit disables the OUT/OUTN outputs (high impedance) until the oscillator starts. This function prevents unstable oscillation and other problems, which can occur when power is applied, from appearing at the output.
MEASUREMENT CIRCUITS

These measurement circuits are used for the evaluation of the electrical and AC characteristics.

Notes

Connect the bypass capacitors, specified in the measurement circuits, between VDD-VSS and VT-VSS.
Connect the load resistors, specified in the measurement circuits, to the OUT and OUTN outputs.
Connect the bypass capacitors and load resistors with wiring pattern as short as possible (less than 3mm length). If the wiring pattern is too long, the desired characteristics cannot be obtained.
Note that if bypass capacitors and load resistors other than the specified values are connected, or if the components are not connected at all, the desired characteristics cannot be obtained.

* Capacitor and resistor values used by NPC
  Capacitors: 0.01μF GRM188B11H103K (Murata Manufacturing Co., Ltd.)
  Resistors: 49.9Ω RN732ATTD49R9B25 (KOA Corporation)

Measurement circuit 1
Measurement Parameter: $I_{DD}$, $I_{STB}$

![Measurement Circuit Diagram]
Measurement circuit 2
Measurement Parameter: $V_{IL}, V_{II}, R_{PU1}, R_{PU2}$

\[ R_{PU1} = \frac{(V_{DD} - V_{II})}{I_{IL}}, \quad V_{II} = 0V \]
\[ R_{PU2} = \frac{(V_{DD} - V_{II})}{I_{IL}}, \quad V_{II} = 0.7V_{DD} \]

INHN PIN
$V_{II}:V_{SS} \rightarrow V_{DD}$ voltage that changes output state
$V_{IL}:V_{DD} \rightarrow V_{SS}$ voltage that changes output state

Measurement circuit 3
Measurement Parameter: $I_Z$

\[ 0.01\mu F = \text{(Ceramic Chip Capacitor)} \]
Measurement circuit 4

Measurement Parameter: $R_f$

\[
V_{DO} = 0.5V
\]

\[
0.01\mu F \text{ (Ceramic Chip Capacitor)}
\]

\[
VDD \quad \text{XTN} \quad \text{OUT}
\]

\[
7051
\]

\[
\text{XT} \quad \text{OUTN}
\]

\[
\text{INHN} \quad \text{VSS}
\]

\[
R_f = \frac{V_{DO}}{I_{XT}}
\]

Measurement circuit 5

Measurement Parameter: Duty1, Duty2, $V_{OPP}$, $t_r$, $t_f$, $V_{OH}$, $V_{OL}$

\[
0.01\mu F \text{ (Ceramic Chip Capacitor)}
\]

\[
VDD \quad \text{XTN} \quad \text{OUT}
\]

\[
7051
\]

\[
\text{XT} \quad \text{OUTN}
\]

\[
\text{INHN} \quad \text{VSS}
\]

\[
0.01\mu F \text{ (Ceramic Chip Capacitor)}
\]

\[
V_{DD} - 2V
\]

Duty1 (Differential)

Duty2, $V_{OPP}$, $t_r$, $t_f$ (Single Ended), $V_{OH}$, $V_{OL}$
Measurement circuit 6
Measurement Parameter: $t_{OE}$, $t_{OD}$

$t_{OD}$: INHN = VDD to VSS
$t_{OE}$: INHN = VSS to VDD

0.01 $\mu$F (Ceramic Chip Capacitor)

49.9 $\Omega$

VDD
XTN
OUT
7051
XT
OUTN
INHN
VSS

0.01 $\mu$F (Ceramic Chip Capacitor)

$V_{DD} - 2V$

$V_T$

$V_{DD}$

$V_{SS}$
REFERENCE CHARACTERISTICS EXAMPLE (7051 Typical Characteristics)

The characters given below were measured using an NPC standards jig and standard crystal element, and do not represent a guarantee of device characteristics.

Note that the characteristics will vary due to measurement environment and the oscillator element used.

<table>
<thead>
<tr>
<th>Crystal used for evaluation</th>
<th>Parameter</th>
<th>Ax</th>
<th>B1</th>
<th>M1</th>
<th>N1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$f_0$ (MHz)</td>
<td>155.52MHz</td>
<td>245.76MHz</td>
<td>125MHz</td>
<td>155.52MHz</td>
</tr>
<tr>
<td></td>
<td>$C_0$ (pF)</td>
<td>1.7</td>
<td>1.4</td>
<td>2.3</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td>$R_1$ (Ω)</td>
<td>12</td>
<td>17</td>
<td>32</td>
<td>39</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phase Noise</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$f_0 = 155.52MHz$, $T_a = R.T.$ (Room Temperature)</td>
<td>$f_0 = 245.76MHz$, $T_a = R.T.$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_0 = 125MHz$, $T_a = R.T.$</td>
<td>$f_0 = 155.52MHz$, $T_a = R.T.$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[Measurement circuit diagram]
Negative Resistance

7051A1 \( V_{DD} = 3.3V, \ Ta = 25^\circ C \)

7051B1 \( V_{DD} = 3.3V, \ Ta = 25^\circ C \)

7051M1 \( V_{DD} = 3.3V, \ Ta = 25^\circ C \)

7051N1 \( V_{DD} = 3.3V, \ Ta = 25^\circ C \)

[Measurement circuit diagram]

Network-Analyzer (keysight 4396B)
S-Parameter Test Set (Keysight 85046A)

0.01\( \mu F \) (Ceramic Chip Capacitor)

Measurement results using 4396B Agilent analyzer on NPC test jig.
Measurements will vary with test jig and measurement environment.
Frequency Deviation with Voltage

7051A1 $f_0 = 155.52$MHz, $T_a=25^\circ$C

7051B1 $f_0 = 245.76$MHz, $T_a=25^\circ$C

7051M1 $f_0 = 125$MHz, $T_a=25^\circ$C

7051N1 $f_0 = 155.52$MHz, $T_a=25^\circ$C

[Measurement circuit diagram]

VDD
XTN
OUT
7051
XT
OUTN
INHN
VSS

VDD=2.0V
0.01μF (Ceramic Chip Capacitor)

0.01μF (Ceramic Chip Capacitor)

VSS= -1.3V

49.9Ω

Keysight 5052B
50Ω

0.01μF (Ceramic Chip Capacitor)
Output Waveform

7051A1 \( V_{DD} = 3.3V, \ f_0 = 155.52MHz, \ Ta=25^\circ C \)

7051B1 \( V_{DD}=3.3V, \ f_0=245.76MHz, \ Ta=25^\circ C \)

7051M1 \( V_{DD}=3.3V, \ f_0=125MHz, Ta=25^\circ C \)

7051N1 \( V_{DD}=3.3V, \ f_0=155.52MHz, Ta=25^\circ C \)

[Measurement circuit diagram]

Page 9 Measurement circuit 5

Measurement equipment : Oscilloscope  DSO80604B (keysight)
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