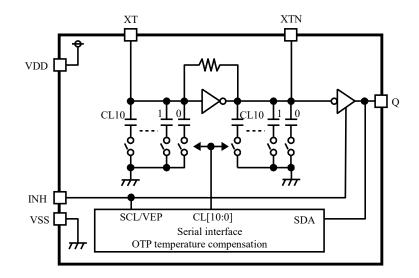
#### 1. OVERVIEW

The WF7290A is 32.768kHz output crystal oscillator module IC that has a digital temperature compensation function. The WF7290A has a Non-volatile memory (OTP) and can be adjusted the oscillation frequency after the modules implementation.

# 2. FEATURES

- Oscillation and output frequency : 32.768kHz
  - Operation voltage range : 1.3V to 3.63V (Oscillation output)
    - : 1.5 V to 3.63 V (Temperature compensation)
- Operating temperature of oscillation and output operation : -40°C to +105°C
- Operating temperature compensation :  $-40^{\circ}$ C to  $+105^{\circ}$ C
- Frequency accuracy :
- ±5.0 ppm Temperature compensation interval : select 2s / 0.5s / 0.25s / 0.125s / 0.0625s
- Low power current consumption
  - : 1.0µA typ.
    - (V<sub>DD</sub>=1.8V, C<sub>LOUT</sub>=0pF, temperature compensation interval 2s.)
- CMOS input/output
- Output drive capability
- :  $\pm 0.1 \text{mA} (V_{DD}=1.5 \text{V})$
- Output disable function
- 2-wire type serial interface

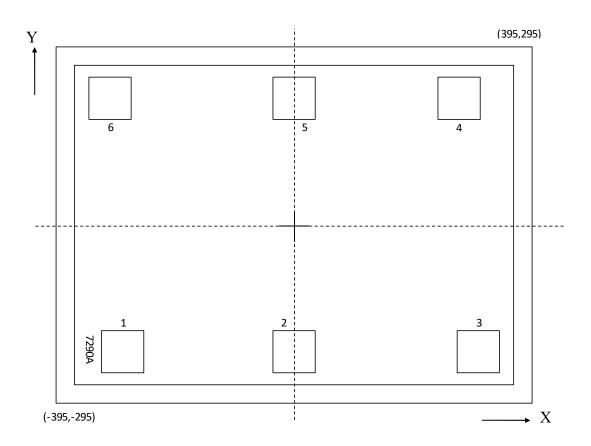
# 3. BLOCK DIAGRAM



3.1 block diagram

# 4. PAD DIMENSIONS

- (1) Chip size  $^{*1}$  : X = 0.79mm, Y = 0.59 mm
- (2) Wafer thickness :  $100 \pm 10 \mu m$
- (2) Rear surface :  $V_{SS}$  potential
- (3) Wafer size :  $\varphi 200 \text{ mm} \pm 0.5 \text{ mm}$
- (4) Pad aperture size :  $70 \ \mu m \times 70 \ \mu m$
- (5) Chip form and Pad dimensions
- \*1 : Chip size is the value between the scribe line centers.



			Unit: µm
PAD No.	Pad Name	Х	Y
1	VDD	-285	-210
2	XT	0	-210
3	VSS	306	-210
4	INH	274	210
5	XTN	0	210
6	Q	-306	210

# 5. PAD DESCRIPTION

Pad No.	Pad name	I/O <sup>*1</sup>	Description
1	VDD	_	(+) supply voltage
2	XT	Ι	Crystal input pin, C <sub>G</sub> built-in
3	VSS	—	(-) ground
4	INH (SCL)	I	Use in Open or "Low" usually. (in PUDN=0, QS[1:0]=00) It becomes serial interface mode if the high voltage is inputted. SCL (Clock input) pin in serial interface mode. Pull-up or pull-down resistors are selectable with built-in One Time Programmable memory (OTP). The polarity of INH is selectable with built-in One Time Programmable memory (OTP).
5	XTN	0	Crystal output connection pin, C <sub>D</sub> built-in
6	Q (SDA)	I/O	Oscillation output (32.768kHz), High-impedance output in standby mode (INH="L" level), SDA(Data input/output) pin in serial interface mode

\*1: I : Input pin, O : Output pin, I/O : Input / Output pin

			V <sub>SS</sub> =0V unless otherwise 1	noted
Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range <sup>*1</sup>	V <sub>DD</sub>	Between VDD and VSS	-0.3 to +4.5	V
Program input voltage range <sup>*1</sup>	V <sub>PP</sub>	Between INH and VSS	-0.3 to +6.75	V
Input voltage range *1,*2	V <sub>IN1</sub>	Input pins INH <sup>*3</sup>	-0.3 to $V_{DD}$ +0.3 <sup>*5</sup>	V
Input vonage range	V <sub>IN2</sub>	Input pins XT	-0.3 to 2.5	V
Output voltage range *1,*2	V <sub>OUT1</sub>	Output pins Q	-0.3 to $V_{DD}$ +0.3 <sup>*5</sup>	V
Output voltage lange	V <sub>OUT2</sub>	Output pins XTN	-0.3 to 2.5	V
Output current <sup>*2</sup>	I <sub>OUT</sub>	Q pin	$\pm 10$	mA
Junction temperature <sup>*2</sup>	Tj	_	+150	°C
Storage temperature range *4	T <sub>STG</sub>	Exclude EEPROM data retention	-55 to +150	°C

# 6. ABSOLUTE MAXIMUM RATINGS

\*1 : Absolute maximum ratings are the values that must never exceed even for a moment. This product may suffer breakdown if any one of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.

- \*2 : Do not exceed these values. If a rating is exceeded, there is a risk of decrease in reliability.
- \*3 : The value is in normal operation except program read/write operation.
- \*4 : When stored in nitrogen or vacuum atmosphere applied to IC itself only.
- \*5 :  $V_{DD}$  is a  $V_{DD}$  value of recommended operating conditions.

# 7. RECOMMENDED OPERATING CONDITIONS

			V SS	0 v unica	s other wi	se noteu
Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Unit
Operating supply voltage	V	Oscillation output	1.3	1.8	3.63	V
*1	V <sub>DD</sub>	Temperature compensation operation	1.5	1.8	3.63	V
Input voltage	V	INH	V <sub>SS</sub>	-	V <sub>DD</sub>	V
input voltage	$V_{IN}$	XT	V <sub>SS</sub>	-	2.0	V
Operating temperature	T <sub>a</sub>	Oscillation operation	-40	-	+105	°C
Program supply voltage	V <sub>pp</sub>	INH pin V <sub>DD</sub> =1.5V to 3.63V	6.35	6.5	6.75	V
OTP data retention	_	Ta=-40°C to $+105$ °C	10	-	-	years
Output load capacitance	C <sub>LOUT</sub>	Q pin	-	-	30	pF

\*1: For stable operation of this product, mount a ceramic chip capacitor that is more than 0.1 µF between VDD and VSS in close proximity to IC.

\* Since it may influence the reliability if it is used out of the recommended operating conditions range, this product should be used within this range.

V<sub>cc</sub>=0V unless otherwise noted

# 8. ELECTRICAL CHARACTERISTICS

#### 8.1. DC Characteristics

U.I. De characteris		0V, V <sub>DD</sub> =1.5V to 3.63V, Ta=-40°	C to +105	5°C unless	s otherwis	e noted
Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Unit
	I <sub>DD11</sub>	$V_{DD}$ =1.8V, $C_{LOUT}$ =0pF <sup>*1</sup> , Measurement circuit 2 Ta=-40°C to +85°C	-	1.0	2.0	μΑ
Current consumption in normal function (Select 2s for	I <sub>DD12</sub>	$V_{DD}$ =1.8V, $C_{LOUT}$ =0pF <sup>*1</sup> , Measurement circuit 2 Ta=-40°C to +105°C	-	1.0	3.0	μΑ
temperature compensation interval, SPXO=1)	I <sub>DD13</sub>	$V_{DD}$ =1.8V, $C_{LOUT}$ =30pF <sup>*1</sup> , Measurement circuit 2 Ta=-40°C to +85°C	-	2.8	3.8	μΑ
	I <sub>DD14</sub>	$V_{DD}$ =1.8V, $C_{LOUT}$ =30pF <sup>*1</sup> , Measurement circuit 2 Ta=-40°C to +105°C	-	2.8	4.8	μΑ
Current consumption in normal function	I <sub>DD21</sub>	$V_{DD}$ =1.8V, $C_{LOUT}$ =0pF <sup>*1</sup> , Measurement circuit 1 Ta=-40°C to +85°C	-	0.9	1.9	μΑ
(SPXO mode, SPXO=0)	I <sub>DD22</sub>	$V_{DD}$ =1.8V, $C_{LOUT}$ =0pF <sup>*1</sup> , Measurement circuit 1 Ta=-40°C to +105°C	-	0.9	2.9	μΑ
Current consumption in boot operation (SPXO mode, SPXO=0)	I <sub>boot</sub>	Boot <sup>*1</sup> , V <sub>DD</sub> =1.8V, C <sub>LOUT</sub> =0pF <sup>*1</sup> , Measurement circuit 1	-	-	3.3	μΑ
Current consumption in disable function	I <sub>DIS</sub>	Output disable, $V_{DD} = 1.8V$ , Measurement circuit 1,	-	-	2.0	μΑ

\*1: C<sub>LOUT</sub> is the load capacitor connected to Q pin outside.

\*2: In order to shorten the oscillation start up time, the oscillation circuit has a boot circuit that increases the drive ability. Boot function operates from oscillation start to 0.5s ( $t_{sta}$ + 0.5s) after applying power supply.

The contents of current consumption in normal function

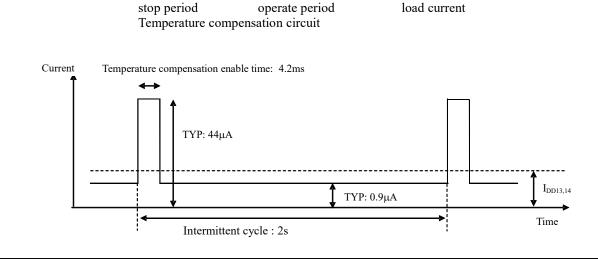
I<sub>DD13,14</sub> is the average value of the intermittent cycle (see below).

Example) temperature compensation interval =2s,  $V_{DD}$ =1.8V,  $C_{LOUT}$ =30pF

-

 $TYP: I_{DD13,14} = 0.9 \mu A \times (2s - 4.2ms) / 2s + 44 \mu A \times 4.2ms / 2s + 30 pF \times 32.768 kHz \times 1.8V = 2.8 \mu A \times 1.8 V = 2$ 

4



Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Unit
High-level input	N7	INH <sup>*1</sup> , Measurement circuit 3	0.8V <sub>DD</sub>	-	-	V
voltage	V <sub>IH1</sub>	Q <sup>*2</sup> , Measurement circuit 3,	0.8V <sub>DD</sub>	-	-	V
Low-level input voltage	V	INH <sup>*1</sup> , Measurement circuit 3	-	-	$0.2V_{DD}$	V
	$V_{IL1}$	Q <sup>*2</sup> , Measurement circuit 3,	-	-	0.2V <sub>DD</sub>	V
High-level output voltage	V <sub>OH1</sub>	Q <sup>*1</sup> , I <sub>OH</sub> =-0.1mA,V <sub>DD</sub> =1.5V Measurement circuit 4	0.9V <sub>DD</sub>	-	-	V
	V <sub>OH2</sub>	$Q^{*2}$ , $I_{OH}$ =-10µA, $V_{DD}$ =1.5V Measurement circuit 5	0.9V <sub>DD</sub>	-	-	V
Low-level output voltage	V <sub>OL1</sub>	Q <sup>*1</sup> , I <sub>OL</sub> =0.1mA,V <sub>DD</sub> =1.5V Measurement circuit 4	-	-	$0.1 V_{DD}$	V
	V <sub>OL2</sub>	$Q^{*2}$ , $I_{OL} = 10 \mu A$ , $V_{DD} = 1.5 V$ Measurement circuit 5	-	-	$0.1 V_{\text{DD}}$	V

 $V_{SS}$ =0V,  $V_{DD}$ =1.5V to 3.63V, Ta=-40°C to +105°C, unless otherwise noted

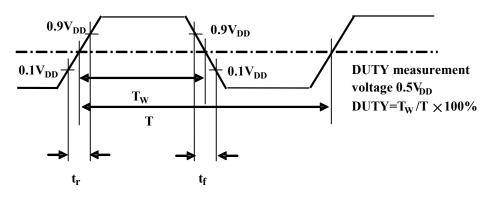
\*1 : It is the value in normal operation except temperature compensation control registers and OTP access.

\*2 : It is the value in access to temperature compensation control registers and OTP.

#### 8.2. AC Characteristics 1 (Q pin output characteristics) $V_{cc}=0V V_{DD}=1.5V \text{ to } 3.63V. \text{ Ta}=-40^{\circ}\text{C to } +105^{\circ}\text{C} \text{ unless otherwise noted}$

$V_{SS}=0.0, V_{DD}=1.3.0, 10, 3.03.0, 1a=-40^{\circ}C$ to +105°C unless otherwise not						
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output duty cycle	Duty	$C_{LOUT}$ =30pF, 0.5 $V_{DD}$ threshold, Measurement circuit 2	40	50	60	%
Output rise time	t <sub>r</sub>	$C_{LOUT}$ =30pF, 10% $\rightarrow$ 90% Measurement circuit 2	-	-	40	ns
Output fall time	$t_{\rm f}$	$C_{LOUT}$ =30pF, 90% $\rightarrow$ 10% Measurement circuit 2	-	-	40	ns

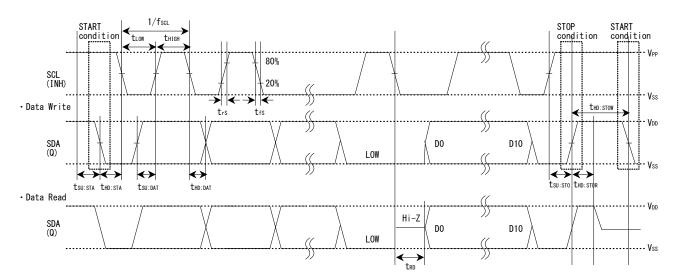
# **Timing Chart**



# 8.3. AC Characteristics 2 (2-wire type serial interface)

When accessing to the temperature compensating control register or OTP

	V <sub>SS</sub> =0V,	$V_{DD}$ =1.5V to 3.63V, Ta=-40°C to	+105°C	unless of	therwise	noted
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL clock frequency	f <sub>SCL</sub>	After start condition	20	-	500	kHz
Start condition setup time	t <sub>SU;STA</sub>	_	0.3	-	-	μs
Start condition hold time	t <sub>HD;STA</sub>	_	0.3	-	-	μs
Data setup time	t <sub>SU;DAT</sub>	_	0.3	-	-	μs
Data hold time	t <sub>HD;DAT</sub>	_	0.3	-	-	μs
Stop condition setup time	t <sub>SU;STO</sub>	—	0.3	-	-	μs
	t <sub>HD;STOW</sub>	Write the data to OTP	1.7	-	-	ms
Stop condition hold time	t <sub>HD;STOR</sub>	Read the data from OTP, Access the registers	0.2	-	-	μs
SCL "L" period	t <sub>LOW</sub>	_	1	-	-	μs
SCL "H" period	t <sub>HIGH</sub>	_	1	-	-	μs
SCL rise time	t <sub>rS</sub>	20%→80%	-	-	0.2	μs
SCL fall time	t <sub>fS</sub>	80%→20%	-	-	0.2	μs
Read data delay time	t <sub>RD</sub>	C <sub>LOUT</sub> =15pF	-	-	0.5	μs



# 8.4. Oscillation characteristics

WF7290A oscillation characteristics is in the below crystal parameters

Parameter	Symbol	Rating
Frequency	f0	32.768kHz
Frequency permission deviation	∕∫f	±20ppm(25°C)
Peak temperature	Ti	25°C±5°C
Parabolic coefficient	В	-0.04ppm/°C <sup>2</sup> min
Load capacitance	CL	9.0pF
Serial resistance	R1	$100 \mathrm{k}\Omega\mathrm{max}$

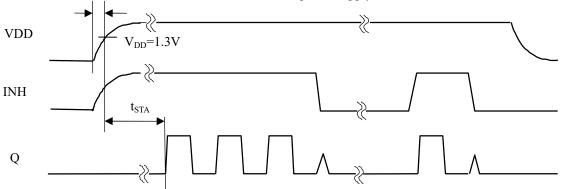
# $V_{SS}{=}0V,\,V_{DD}{=}1.3V$ to 3.63V, Ta=-40°C to +105°C, $C_{LOUT}{=}30pF$ unless otherwise noted

Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Unit
Oscillation frequency	fo	$Ta = +25^{\circ}C, V_{DD} = 1.3V$ to 5.5V	-	32.768	-	kHz
Oscillation start up voltage	V <sub>STR</sub>	V <sub>DD</sub> rises gradually. Measurement circuit 2	-	-	1.3	V
Oscillation stop voltage	V <sub>STO</sub>	V <sub>DD</sub> descends gradually. Measurement circuit 2	0.5	-	1.3	V
Frequency accuracy *2	$\Delta f / fo$	$V_{DD} = 1.8 V$	-	-	± 5.0	ppm
Oscillation start up time <sup>*3</sup>	t <sub>STA</sub>		-	-	0.5	S
Frequency-voltage characteristic	∐f/∠V	V <sub>DD</sub> ±10%	-1.0	-	+1.0	ppm

\*1: CL setting is built-in capacitance value for crystal oscillation ( $C_L$ ).

\*2: Frequency accuracy is the theoretical value.

# \*3: Timing Chart at power supply



# $t_{VDD}{<}10 \text{ms/V} \quad t_{VDD}{:}$ The rise time of the power supply from 0V to 1.3V

# 9. FUNCTIONAL DESCRIPTION

# 9.1. INH Function

Q outputs 32.768 kHz when INH goes "L" level or OPEN (in initial setting). When a high voltage is input to INH, INH becomes SCL, which is the input terminal to which the clock of the serial interface is input, and Q becomes SDA, which is the data of the serial interface, I/O terminal. The oscillator circuit don't stop the operation. Input the voltage of  $V_{IH1}$  or  $V_{IL1}$  to INH certainly. After power-on, the Q terminal outputs "L" level until the OTP data of QS bit is read. The polarity of the INH can be changed with OTP memory.

		Oscillator		
INH	$QS[1:0]=[00]^{*1}$	QS[1:0]=[01]	QS[1:0]=[10]	Oscillator
"H" level	Hi-Z	32.768kHz	32.768kHz	Operating
"L" level	32.768kHz	Hi-Z	32.768kHz	Operating
OPEN	32.768kHz <sup>*2</sup>	32.768kHz <sup>*2</sup>	32.768kHz	Operating

\*1: Initial value.

\*2: In the case of PUDN="0" (initial value).

		INH	
PUDN	QS[1:0]=[00]	QS[1:0]=[01]	QS[1:0]=[10]
0*1	Pull-down resistor	Pull-up resistor	Pull-down resistor
0	connected	connected	connected
1	Hi-Z	Hi-Z	Hi-Z

\*1: Initial value.

# **9.2.** SPXO Function

Temperature compensation operation is not performed by setting the SPXO bit to 0. (initial value) If OTP is not written, CL setting will be 400/H.

SPXO	Temperature compensation
	disable
$0^{*1}$	(Only the first temperature compensation operation after start-up is
	performed. The C <sub>L</sub> load capacitance setting value at that time is held.)
1	enable

\*1: Initial value.

# **9.3.** Temperature compensation function

Built-in capacitance for crystal oscillation is the capacitance array. This is controlled by CL registers to adjust frequency. The data of OTP which makes the A/D conversion output of an internal thermometer an address is periodically stored in CL registers. The adjustment data which makes the frequency constant to temperature is written in OTP. These data will be stored to CL registers at a temperature compensation interval and will change the value of built-in oscillator capacitance to adjust frequency. The temperature compensation interval is selected from 2s/0.5s/0.25s/0.125s/0.0625s.

	TSC[2:0] (T[9:7])		Temperature compensation interval					
TSC2 (T9)	TSC1 (T8)	TSC0 (T7)						
0	0	0	0.5s					
0	0	1	0.25s					
0	1	0	0.125s					
0	1	1	0.0625s					
1	1	1	2s					

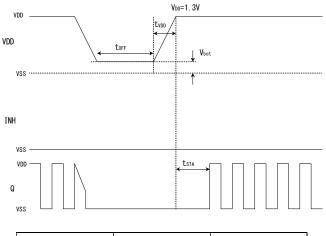
# 9.4. Power activation

It is the power-on clear circuit built-in. This circuit sets 300/H to CL registers at power activation. After starting oscillation, the first temperature compensation operates at 0.5s. After that, it operates at the selected temperature compensation interval.

The boot circuit operates to 0.5s after starting oscillation from power activation.

#### 9.5. Attention at the time of the power supply setup

The instability of IC inside circuit in the power supply start might cause malfunction. Therefore, built-in power-on clear circuit prevents it. Start up the power supply under the recommended conditions of  $t_{VDD}$ ,  $t_{OFF}$ ,  $V_{bot}$  in order to operate it certainly.



t <sub>VDD</sub>	t <sub>OFF</sub>	V <sub>bot</sub>
under 10ms/V	over 0.5ms	0V

# 10. TEMPERATURE COMPENSATION REGISTERS TABLE

D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A7~A0
Data										Address	
AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	00/h
STA	TCL	PTM1	PTM0	TOSC	-	-	TS3	TS2	TS1	TS0	01/h
VDT	TSC2	TSC1	TSC0	CRC	CR5	CR4	CR3	CR2	CR1	CR0	02/h
CL10	CL9	CL8	CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0	03/h
SPXO	QS1	QS0	PUDN	OSC2	OSC1	OSC0	OFS3	OFS2	OFS1	OFS0	04/h
T10	Т9	T8	T7	Т6	T5	Τ4	Т3	T2	T1	Т0	08/h
C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	10/h
											20/h
											-
		т			-l-+- ( <b>A</b> -l-l			0.01)			-
		Tem	perature co	mpensation	data (Add	ress IU/n t		0:0])			-
									E0/h		
										F0/h	
K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0	00/h

\*The double line indicates OTP field.

# 10.1. Serial Port Field Description

Field				description	Initial value						
<b>AD[10:0]</b> (R)	These ar only. * <sup>1</sup> Maximu Minimu	000 0000 0000*5									
STA (W)	this bit, a stopped from ser	This is the bit for A/D conversion start up. A/D conversion starts when 1 is written in this bit, and then it will be finished after 7.8ms. Normal intermittent operation is stopped by starting serial communication. And, A/D conversion starts to use the data from serial communication. Don't write and read from serial interface while A/D conversion operates.									
TCL (W)	For IC te	For IC test									
PTM[1:0]	For IC te	For IC test									
TOSC (W)	For IC te	est			0 For IC test <sup>*2</sup>						
<b>TS[3:0]</b> (W)	For IC te	est			0000 For IC test <sup>*2</sup>						
VDT (R)	For IC te	est			For IC test <sup>*2</sup>						
	T[9:7] d	This is the bit of the temperature compensation interval setup.T[9:7] data of OTP is written in here during a normal function.TSC2TSC1TSC0Temperature compensation interval									
<b>TSC[2:0]</b>	TSC2	$000^{*4}$									
(R/W)	0										
(T[9:7])	0	(000)									
	0	1	0	0.125s 0.0625s							
	1	1	1	2s							

32kHz output crystal oscillator IC with temperature compensation function

Field					descri	otion			Initial value			
		etting data										
CRC	Written	the trimm	ing data 🛛	Γ6 in nor	nal opera	tion.			$0^{*4}$			
(R/W)			1	( )					0			
		the below							(0)			
(T6)		mperature	-						(*)			
		• Temperature compensation ranges -40 to +105°C : 0										
	CR oscillation frequency adjustment bits Written the trimming data T[5:0] in normal operation.											
		CR oscill					nonou					
								ent CR data to T[5:0] in				
	OTP.	nging CK	[5.0] at 1	a 25 C	. And the	ii, write th	ie aujustine	In CR data to 1[5.0] II				
		mperature	compens	ation ran	pes -40 to	+85°C : 5	7.0kHz @	25°C				
CR[5:0]							51.8kHz @		$100000^{*4}$			
(R/W)	CR5	CR4	CR3	CR2	CR1	CR0		cillation frequency <sup>*3</sup>	100000			
	0	0	0	0	0	0	510 550	22.2kHz	(000000)			
(T[5:0])	0	0	0	0	0	1		23.1kHz	· · · · ·			
	0	0	0	0	1	0		23.9kHz				
	С	R oscillat	ion freque	ency adju	stment ste	ep <sup>*2</sup> 0.84	kHz(1.5% o	of 57.0kHz) 6bits				
	1	1	1	1	0	1		68.6kHz				
	1	1	1	1	1	0		69.3kHz				
	1	1	1	1	1	1		70.0kHz				
CL[10:0] (R/W)				-	_		crystal osc	illator	011 0000 0000*4			
		ature com	pensation		peration s ] : enable				$0^{*4}$			
SPXO	[0] : dis	Ũ										
(K[10])	When "0" is set, only the first temperature compensation operation after start-up is performed. The $C_L$ load capacitance setting value at that time is held.								(0)			
	Polarity	selection	$\frac{1000}{100}$ Car	H termin	setting va	ilue at that	t unie is nei	id.				
		the trimm				peration						
OCI1-AI				<b>1</b> [).0] III	normar of				$00^{*4}$			
QS[1:0]	QS1	QS0		VH="H"		Output sta INH=		INH="OPEN"	00			
(K[9:8])	0	0		<del>vп– п</del> Hi-Z		32.768		32.768kHz <sup>*6</sup>	(00)			
	0	1	30	2.768kHz				32.768kHz <sup>*6</sup>	(00)			
	1	0				32.768		32.768kHz				
	-		1					J2. / UONIIZ				
PUDN		pull-dow					bit		$0^{*4}$			
(K7)		the trimm	ing data I		-				(0)			
	[0] : cor	meet		L	1] : non-c	Jimeet			o.t*/			
OSC[2:0]	Oscillat	or current	adjustme	nt bits.	Write "10	00b"			011*4			
(K[6:4])			5						(000) $0000^{*4}$			
OFS[3:0]	Correcti	ion bits fo	r the calc	ulation re	sult of the	C <sub>L</sub> load c	capacitance	setting value	(0000)			
(K[3:0])								ial interface. The higher f				

\*1: A/D conversion of the temperature sensor is 11-bit and they are read in the serial interface. The higher 5 bits is actually used as the address of OTP. As a result of A/D conversion, when the lower 6 bits are not "0", compensation data is interpolated from the OTP data of the higher 5 bits address and the address added to it.

\*2: This bit is for IC test only. Write "0" to them.

\*3: designed value

\*4: Value just after power-up. The data written to OTP is stored in the register in the temperature compensation. All data of OTP are "0" in shipping this device.

\*5: Value just after power-up. The result of conversion is stored after A/D conversion.

\*6: Value in PUDN=0. INH is Hi-Z in PUDN=1. Input voltage according to the specification of the input voltage constantly.

# **10.2.** OTP data

D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A7~A0
Data											Address
T10	Т9	T8	T7	Т6	T5	T4	Т3	T2	T1	Т0	08/h
C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	10/h
									20/h		
											-
		Tam			data (Add			0.01)			-
		Tem	perature co	mpensation	I data (Add	ress 10/ n t		0:0])			-
											E0/h
											F0/h
K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0	00/h

• T[9:0] bits

These are the bits of the analog circuit compensation data. Write the adjustment CRC data and CR data in T[6:0].

T[9:7] is for the temperature compensation interval setup.

• C[10:0] bits

These are the bits of the set value of  $C_L$  load capacitance of crystal oscillator. Write the adjustment data for temperature compensation.

• K[10:0] bits (Address to control the INH function)

These are bits for SPXO setting, INH function selection and IC testing. Write temperature compensation operation control data to K[10]. Write to the data to select INH function in K[9:7]. K [6:4] are the oscillator current adjustment bits. Write "100b".K[3:0] are correction bits for the calculation result of the  $C_L$  load capacitance setting value.

\* About OTP data, write the data to all address and all bits under predetermined conditions

And it prohibited the accessing to the addresses except the above address.

Note that the data "0" are written to each address in shipping this device. (When read from outside, all 1 is returned but internal data is 0.)

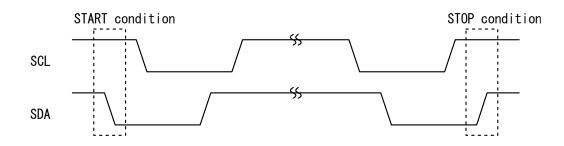
The  $C_L$  load capacitance is set to 400/H when it is used with all data (C[10:0] = 000/H) at the time of shipment from our company. When the OTP memory initial value 000/H is called into the register, the circuit is set to be around  $C_L = 6.5 pF$ .

Be careful when using with the default value of OTP memory.

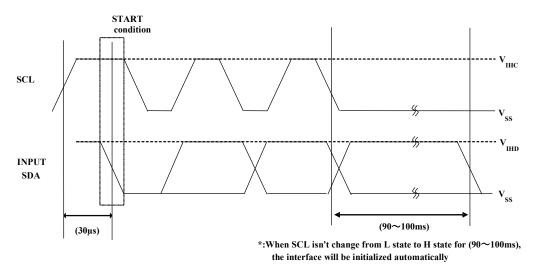
#### **10.3.** 2-WIRE TYPE SERIAL INTERFACE

WF7290A transmits and receives data by the 2-wire type serial interface of SCL (INH: clock line) and SDA (Q: data line). "H" level of SCL is  $V_{PP}$  and "H" level of SDA is  $V_{IH1}$ .

While serial interface is not performing data transfer, set SCL and SDA to "H" level. At this time, if SDA changed from "H" level to "L" level, the state will be in START condition. After detecting START condition, it is possible to start access and to perform data transmission. And, when SCL is "H" level, if SDA changed from "L" level to "H" level, the state will be in STOP condition. After detecting STOP condition, access is finished. These conditions are recognized on the way of data transfer too. Be sure to make these conditions at the data transfer start timing and end timing. About the data transfer format, refer to 10.4.



32.768kHz output of Q pin is disabled and becomes serial interface mode when SCL is inputted V<sub>PP</sub>. If there is no clock input of 90ms to 100ms or more in SCL on the way of communication, the interface is initialized and communication is finished.



Wait for 30us before changing SDA into "L" level from "H" level after making SCL "H" level when transmitting START condition in order to access the serial interface while the temperature compensation in normal operation.

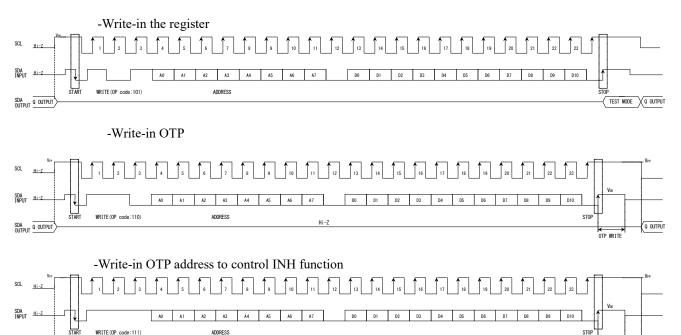
# NPC

# 10.4. Data transmission Format of Temperature Compensating Control Register and OTP

Data transmission format of temperature compensating control register and OTP is the below. Transmit from LSB data first.

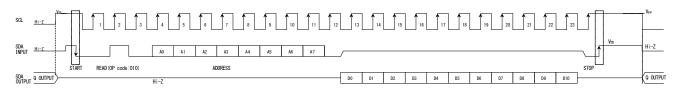
#### 10.4.1. Data Write-in Format

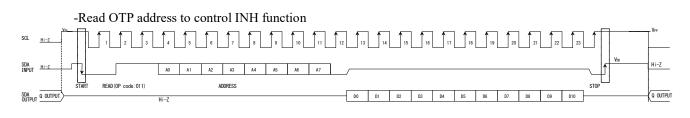
After start condition, the transmitter transmits 23 bits of WRITE opcode (101 in register, 110 in OTP, 111 in OTP address to control INH function), an address and a data. And then, it transmits STOP condition. The data of registers are written in synchronizing with the rising edge of  $23^{rd}$  SCL clock. OTP is written by OTP write-in circuit. OTP write-in circuit starts after detecting STOP condition and write-in time takes 1.7ms. Keep SCL and SDA of STOP condition (SCL=V<sub>PP</sub>, SDA=V<sub>IH1</sub>) for 1.7ms. And, to finish serial communication and return to the normal operation, it needs to release SDA (Hi-Z) by set "L" (V<sub>IL1</sub>) to SCL after STOP condition.



#### 10.4.2. Data Read-out Format

After start condition, the transmitter transmits 11 bits of READ opcode (010 in registers and OTP, 011 in OTP address to control INH function), and an address. The 12<sup>th</sup> bit transfers "L" level. And, it releases SDA(Hi-Z) at the falling edge of 12<sup>th</sup> SCL clock. The receiver sends out the read data in synchronizing with the falling edge of 12<sup>th</sup> SCL clock. To finish serial communication, it needs to execute the same procedure as 10.4.1.



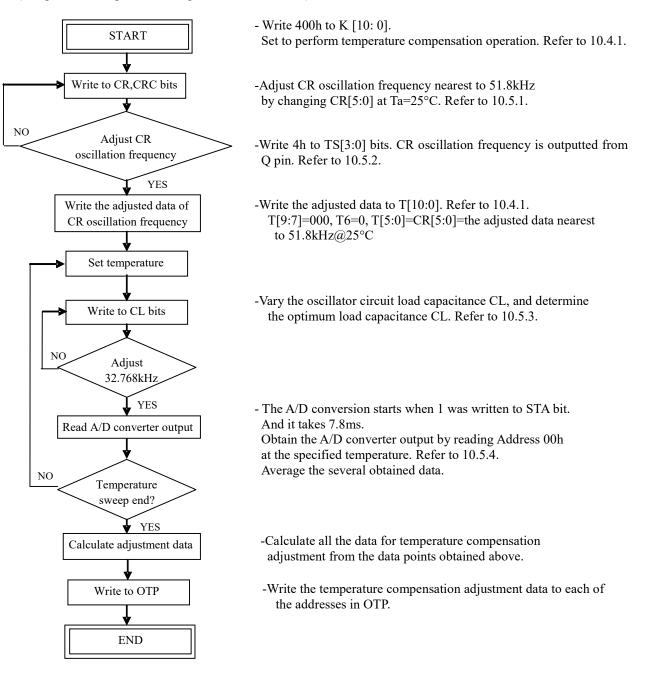


Q OUTPU

OTP WRITE

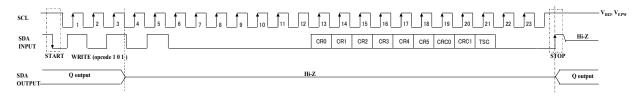
# 10.5. Temperature Compensation Adjustment Flow Chart

(Temperature compensation range  $-40^{\circ}C \sim +105^{\circ}C$ )

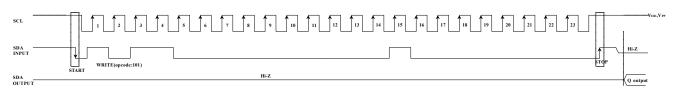


#### 10.5.1. Data Write-in Format to adjust CR oscillation frequency

Write CR[5:0] and CRC to address 02h to adjust CR oscillation frequency. Refer to 10.1.3 in adjusting CR oscillation frequency. After writing data, carry out 10.5.2 with holding INH=H.

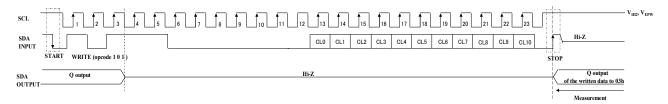


#### **10.5.2.** Data Write-in Format to output CR oscillation frequency at Q pin (Test mode) Write 004h to address 01h to confirm CR oscillation frequency at Q pin. INH=L makes this mode cancel.



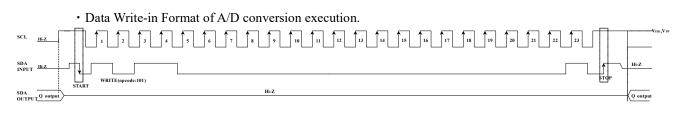
#### 10.5.3. Data Write-in Format to adjust CL[10:0] bits (CL adjustment emulation mode)

Write  $C_L$  load capacitance data to address 03h in order to obtain the optimum  $C_L$  load capacitance data. After recognized STOP condition, Q outputs crystal oscillation frequency with  $C_L$  load capacitance data of address 03h. Keep INH=H while measurement. INH=L makes this mode cancel. Determine the optimum  $C_L$  load capacitance by changing the data of address 03h.

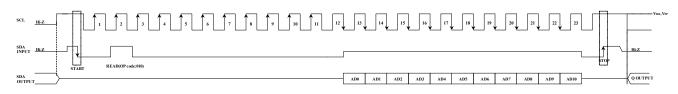


#### **10.5.4.** Data Read-out Format of A/D conversion results

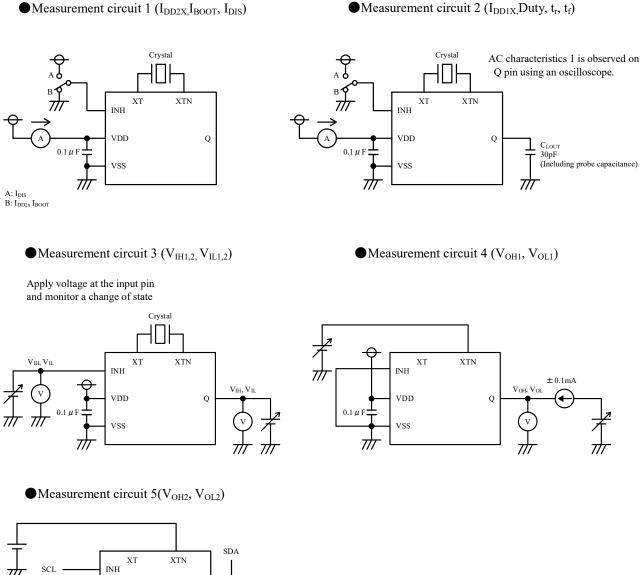
Execute A/D conversion with writing the data of 400h(STA=1) to address 01h in order to obtain the results of A/D conversion. After that, read the data of address 00h.

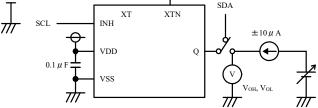


#### · Data Read-out Format of A/D conversion result.



# **11. MEASUREMENT CIRCUIT**

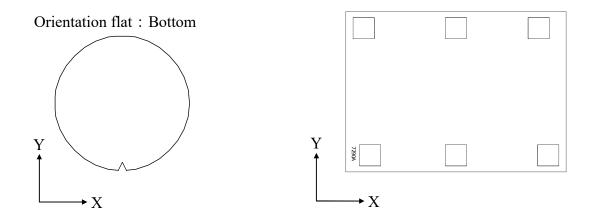


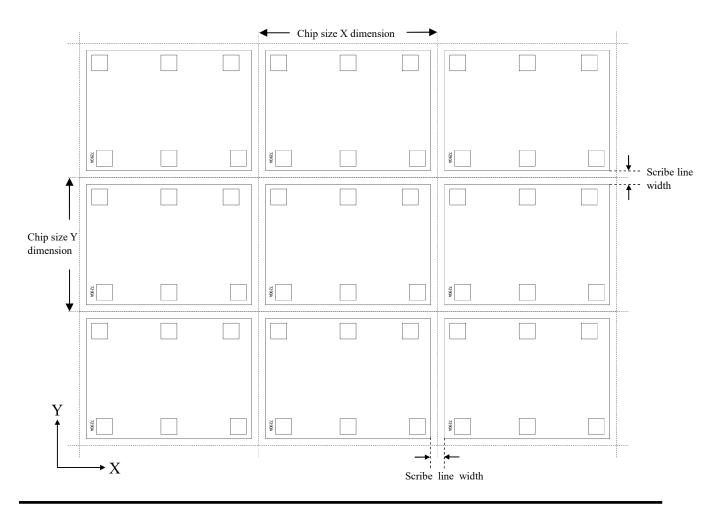


# WF7290A-5-Z1

# 12. WAFER SURFACE ALIGNMENT DIAGRAM

Wafer size : 200mm±0.5mm Scribe line width : 64um (CAD data scribe area 60µm)



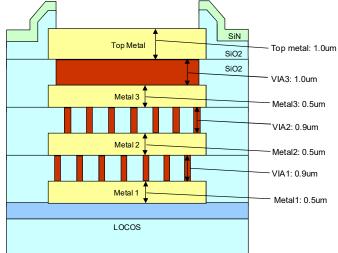


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# 13. CROSS SECTION STRUCTURE

# **13.1.** PAD Cross Section Structure

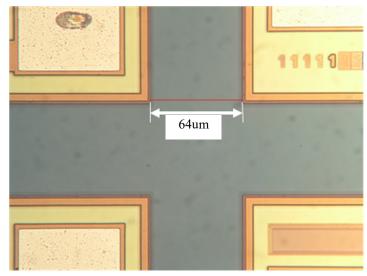


The film thicknesses described above are design values, not actual measurements on the chip.

# 13.2. Seal Ring and Scribe Line Cross Section Structure

	10um	60um	10um	at least 5um	
		2um	-		pad
	<b>**</b>				
chip area	die seal area	scribe line area	die seal area	chip area	

The scribe line width " $64\mu$ m" is the length of the flat area to be seen through a microscope as shown in the photo.



# <Notes on UBM formation>

In UBM (Under Bump Metal) formation to the mounting pad electrode by electroless plating, UBM is similarly formed on the scribe line TEG and the metal exposed part of the accessory. So mask process covering the scribe line is required to prevent these effects.

#### 14. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.

If you wish to use this product in equipment requiring extremely high level of reliability, please contact our sales department or representative in advance.

In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

Please pay your attention to the following points at time of using the products shown in this document.

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If you wish to use the Products in that apparatus, please contact our sales section in advance.

In the event that the Products are used in such apparatus without our prior approval, we assume no responsibility whatsoever for any damages resulting from the use of that apparatus.

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