OVERVIEW

The SM8578BV is a serial interface, real-time clock IC that uses a 32.768kHz crystal oscillator for its reference timing. It comprises second-counter to year-counter clock and calendar circuits that feature automatic leap-year adjustment, alarm and timer interrupt functions, as well as oscillator stop, timer reloading, and other detection functions. Data is transferred to and from an external controller using a 3-wire serial interface. It is available in compact 8-pin VSOP packages, making it ideal for use in all types of portable, hand-held equipment.

FEATURES

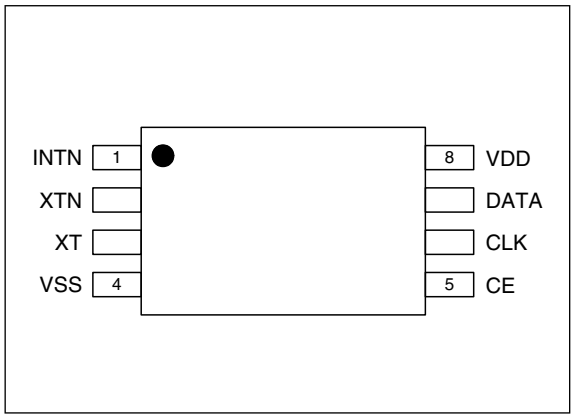
- 1.6 to 5.5V wide operating voltage range
- 0.5µA (typ.) current consumption (V_{DD} = 3.0V, CE = Low)
- 3-wire serial interface control
- Day, day-of-week, hour, and minute alarm interrupt function
- 1/4096 seconds to 255 minutes presettable interval timer interrupt function
- Time update detection function
- Abnormal oscillation detection function
- Automatic leap-year adjustment function (Western and Japanese calendars)
- Oscillator capacitor C_D built-in
- Molybdenum-gate CMOS process
- Miniature 8-pin VSOP package

ORDERING INFORMATION,

Device	Package
SM8578BV	8-pin VSOP

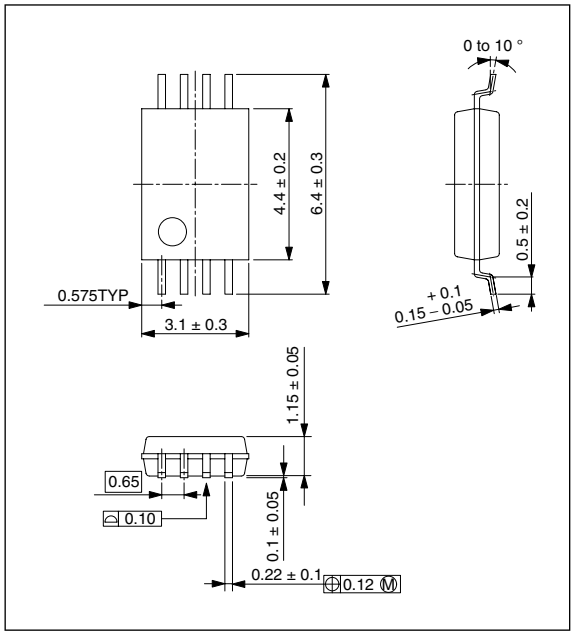
PINOUT

(Top view)

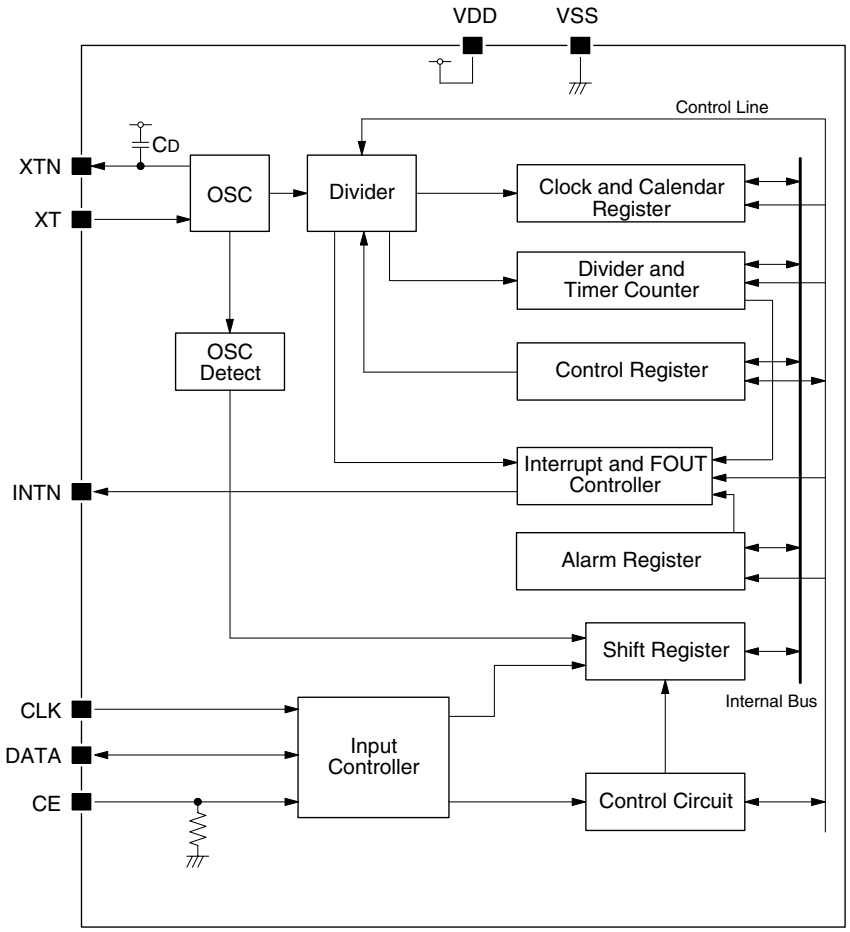


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function
1	INTN	O	Timer interrupt/alarm interrupt output, determined by internal mode setting, or frequency output, with frequency value given in the frequency set register (N-channel open-drain output)
2	XTN	O	Oscillator output. Oscillator capacitor C_D built-in.
3	XT	I	Oscillator input
4	VSS	–	Negative supply voltage connection
5	CE	I	Chip enable input with pull-down resistance built-in. Internal registers can be accessed when CE is HIGH.
6	CLK	I	Serial data transfer clock input. In write mode, data is read in from DATA on the rising edge of CLK. In read mode, data is read out from DATA on the rising edge of CLK.
7	DATA	I/O	Serial data transfer data input/output. When CE goes HIGH, the first four bits of write data determine the operating mode (read mode/write mode).
8	VDD	–	Positive supply voltage connection. A 0.1µF bypass capacitor should be connected between VDD and VSS.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.3 to +7.0	V
Input voltage range	V_{IN}	Input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage range 1	V_{OUT1}	INTN	V_{SS} – 0.3 to +8.0	V
Output voltage range 2	V_{OUT2}	DATA	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D		150	mW
Storage temperature range	T_{STG}		–55 to +125	°C

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		1.6 to 5.5	V
Operating temperature range	T_{opr}		–40 to +85	°C

DC Characteristics

V_{SS} = 0V, V_{DD} = 1.6 to 5.5V, C_G = 10pF, Ta = –40 to +85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Current consumption 1	I_{DD1}	V_{DD} = 5V	CE = V_{SS}, DATA, INTN = V_{DD}	–	1.0	2.0	µA
Current consumption 2	I_{DD2}	V_{DD} = 3V		–	0.5	1.0	µA
HIGH-level input voltage	V_{IH}	CE, CLK, DATA pins		0.8V_{DD}	–	V_{DD}	V
LOW-level input voltage	V_{IL}			0	–	0.2V_{DD}	V
Input leakage current	I_{LEAK}	V_{IN} = V_{DD} or V_{SS}, CE, CLK pins		–0.5	–	0.5	µA
Input resistance 1	R_{DWN1}	V_{DD} = 5V	V_{IN} = V_{DD}, CE pin	75	150	300	kΩ
Input resistance 2	R_{DWN2}	V_{DD} = 3V		150	300	600	kΩ
Output voltage 1	V_{OH1}	V_{DD} = 5V	I_{OH} = –1mA, DATA pin	4.5	–	5.0	V
	V_{OH2}	V_{DD} = 3V		2.0	–	3.0	V
	V_{OL1}	V_{DD} = 5V	I_{OL} = 1mA, DATA pin	–	–	V_{SS} + 0.5	V
	V_{OL2}	V_{DD} = 3V		–	–	V_{SS} + 0.8	V
Output voltage 2	V_{OL3}	V_{DD} = 5V	I_{OL} = 1mA, INTN pin	–	–	V_{SS} + 0.25	V
	V_{OL4}	V_{DD} = 3V		–	–	V_{SS} + 0.4	V
Output leakage current	I_{OZ}	V_{OUT} = V_{DD} or V_{SS}, DATA, INTN pins		–0.5	–	0.5	µA

Oscillator Characteristics

Ta = 25°C, C_G = 10pF, X'tal = NPC reference crystal (C_I = 30kΩ, C_L = 6pF) unless otherwise noted.

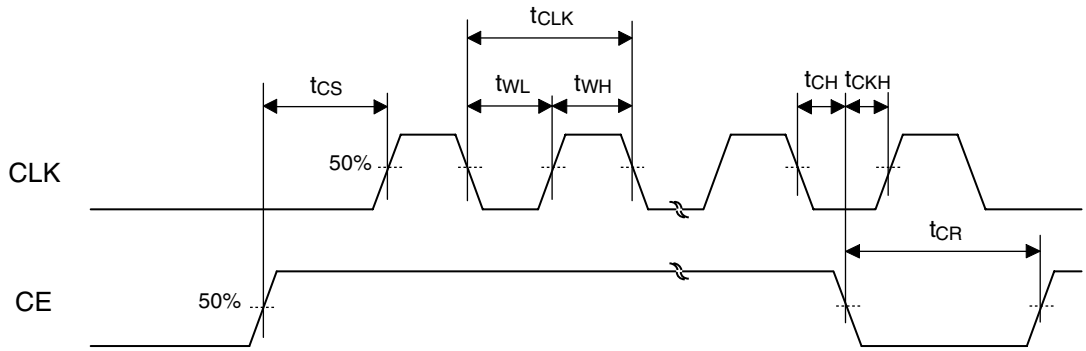
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator startup time	T_{STA}	V_{DD} = 1.6V	–	–	5.0	s
Oscillator stop voltage	V_{STO}		–	–	1.5	V
Frequency voltage characteristic	f/V	V_{DD} = 1.6 to 5.5V	–2	–	2	ppm/V
Frequency accuracy	ε_{IC}	V_{DD} = 5.0V	–10	–	10	ppm
Output capacitance	C_D	V_{DD} = 5.0V	–	15	–	pF

AC Characteristics

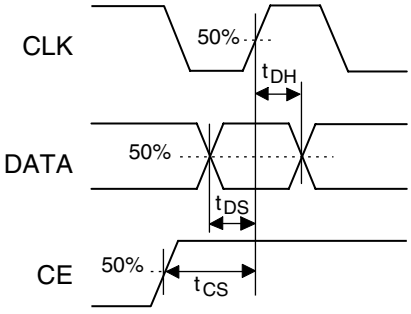
V_{SS} = 0V, Ta = –40 to +85°C unless otherwise noted.

Parameter	Symbol	Condition	V_{DD} = 5.0V ± 10%			V_{DD} = 3.0V ± 10%			Unit
			min	typ	max	min	typ	max	
CLK clock cycle	t_{CLK}		600	–	–	1200	–	–	ns
CLK HIGH-level pulsewidth	t_{WH}		300	–	–	600	–	–	ns
CLK LOW-level pulsewidth	t_{WL}		300	–	–	600	–	–	ns
CE setup time	t_{CS}		150	–	–	300	–	–	ns
CE hold time	t_{CH}		200	–	–	400	–	–	ns
CE recovery time	t_{CR}		300	–	–	600	–	–	ns
CLK hold time	t_{CKH}		50	–	–	100	–	–	ns
Write data setup time	t_{DS}		50	–	–	100	–	–	ns
Write data hold time	t_{DH}		50	–	–	100	–	–	ns
Read data output delay time	t_{RD}	C_L = 50pF	–	–	200	–	–	400	ns
Output disable delay time	t_{RZ}	C_L = 50pF R_L = 10kΩ	–	–	100	–	–	200	ns
Input rise and fall time	t_{RF}		–	–	20	–	–	40	ns
Abnormal oscillation detection time	t_{OSC}		10	–	–	10	–	–	ms

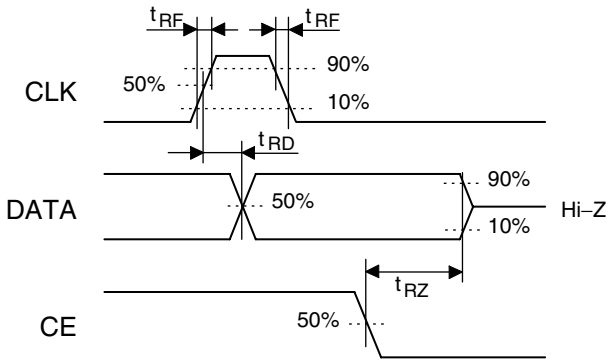
Timing Diagrams



Data write



Data read



FUNCTIONAL DESCRIPTION

Register Table

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Read	Write
0	Second	FOS	40	20	10	8	4	2	1	Yes	Yes
1	Minute	fr	40	20	10	8	4	2	1	Yes	Excl. bit 7
2	Hour	fr	*	20	10	8	4	2	1	Yes	Excl. bit 7
3	Day-of-week	fr	6	5	4	3	2	1	0	Yes	Excl. bit 7
4	Day	fr	*	20	10	8	4	2	1	Yes	Excl. bit 7
5	Month	fr	*	*	10	8	4	2	1	Yes	Excl. bit 7
6	Year	80	40	20	10	8	4	2	1	Yes	Yes
7	Minute alarm	AE	40	20	10	8	4	2	1	Yes	Yes
8	Hour alarm	AE	*	20	10	8	4	2	1	Yes	Yes
9	Day-of-week alarm	AE	6	5	4	3	2	1	0	Yes	Yes
A	Day alarm	AE	*	20	10	8	4	2	1	Yes	Yes
B	Frequency	FE	*	FD4	FD3	*	FD2	FD1	FD0	Yes	Yes
C	Fixed cycle	TE	*	TD1	TD0	*	*	*	*	Yes	Yes
D	Fixed-cycle counter	128	64	32	16	8	4	2	1	Yes	Yes
E	Control 1	*	*	*	TI/TP	AF	TF	AIE	TIE	Yes	Yes*1
F	Control 2	*	TEST	*	RESET	HOLD	*	*	*	Yes	Yes

*1. The AF and TF bits have “0” only valid write data values.

Note 1. When power is applied, all register values are undefined, hence they must be initialized.
Note 2. When Register D is read, the previously preset data value written to the register is read.

Clock and Calendar Registers (Registers 0 to 6)

- Data is in BCD format. For example, register 0 data "0101 1001" represents the value 59 seconds. Also, "*"-entries in the register table represent read/write locations that can be used as RAM.
- Clock timing is in 24-hour mode.
- Year register and leap year:
  The year register represents years as 2 digits, with 00 following year 99.
  Leap years are automatically identified for years up to 2099.
- Day-of-week register:
  The day-of-week register is a 7-bit register (bits 0 to 6) with valid values shown in the following table.
  Note that a register setting with a multiple number of "1" bits is invalid.

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Day-of-week
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

- FOS (Abnormal Oscillation Detection Bit)
  This flag reports oscillation abnormalities during normal operation, such as may occur when the supply voltage falls too low, for example. It is set to "1" to indicate abnormal oscillation, and maintains this value until a "0" bit is written. It is not affected by the function of any other bits.
- fr (Read Flags)
  When CE is HIGH, these flags are set to "1" when the 1s seconds digit is incremented. They are set to "0" when CE goes LOW. This makes it possible to determine whether the 1s seconds digit has been incremented during a clock register read-out operation (when CE is HIGH). If the fr bits are set to "1", all the clock timing registers should be read again.
  The seconds and year registers do not have fr flags. Instead, bits 6 and 5 in the seconds register and bits 7 and 6 in the year register are logically-Ored with data "1" (example: year register 00101001 → 11101001). When CE goes LOW, the register values are restored (example: year register 11101001 → 00101001).

Alarm Registers (Registers 7 to A)

- These registers contain the alarm interrupt time setting. When the alarm matches the clock registers, the INTN output goes LOW (if the alarm interrupt enable AIE bit is set to 1).
- The alarm can be set for day-of-week, day, hour and minute.
  Bit 7 of each of the alarm registers is an enable alarm AE bit. These bits can be used to implement repetitive alarms, such as for every hour or every day.
- The day-of-week alarm can optionally be set for multiple alarms.
  Correct alarm output may not occur if the only alarm setting is a day-of-week alarm.
- When the AE bit is set to 0, the alarm registers are compared with the corresponding clock registers. When set to "1", the data is ignored as don't care bits and is always deemed to match.
- When the AIE bit in register E is set to "0", output on pin INTN is disabled. The TIE and FE bits must be set to "1" and the AIE bit must be set to "0" to enable alarm interrupts.
- Day-of-week alarm bit relationship.

Bit	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Day-of-week	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

Timer Registers (Registers C to E)

- These registers control the 8-bit presettable down-counters used for timer interrupts. The counter source clock is assigned by register C, and the counter frequency divider is assigned by register D.
- When the timer count register counts down to zero, with source clock cycle timing, the INTN output goes LOW (if the timer interrupt enable TIE bit is set to "1").
  When the TI/TP bit is set to "1", the fixed-cycle counter register data is reloaded and the count down starts again. Accordingly, this bit can be used to implement an interval timer (periodic mode).
- When the TIE bit in register E is set to "0", output on INTN is disabled.
  The TI/TP, FE, AIE, and TIE bits must be set for normal timer operation (with the FE and AIE bits set to "0").
- When data is written to register D, the presettable down counters are updated. The data written to register D is maintained until a subsequent data write is performed, hence this register can be used as RAM, similar to the "*"- entries in the register table, when timer interrupt mode is not used (when TIE is "0").
- When the TE bit is set to "0", the counter loads the fixed-cycle counter contents and the count stops. When the TE bit is set to "1", the count starts.
- Note that when the TE bit is set to "0", fixed-cycle interrupts from output INTN are not generated even when the fixed-cycle counter (register D) is loaded with zero data.

TD1	TD0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

Frequency Setting Register (Register B)

- This register contains the arbitrary frequency setting for output on INTN.
  The FD4 and FD3 bits set the frequency divider source clock, and the FD2 to FD0 bits set the frequency divider ratio of the source clock (output frequency = source clock frequency × frequency divider ratio).
  The FE bit must be set to "1" to enable frequency output on INTN, with frequency given by the frequency set register (with the AIE and TIE bits set to "0").
- When the FE bit is set to "0", the output is disabled and is high impedance (Hi-Z).

FD4	FD3	Source clock
0	0	32768Hz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

FD2	FD1	FD0	Frequency divider ratio
0	0	0	1/1
0	0	1	1/2
0	1	0	1/3
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/15
1	1	1	1/30

Control Register 1 (Register E)

This register controls alarm interrupts and timer interrupts.

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E	*	*	*	TI/TP	AF	TF	AIE	TIE

- TI/TP bit: Interrupt Signal Output Mode Select. Interrupt/Periodic
  This selects the timer interrupt signal output mode (with the FE and AIE bits set to "0").

TI/TP	0	1
Mode	<Level interrupt mode> INTN goes LOW immediately when a timer interrupt occurs. INTN remains LOW until the TF bit is set to "0" (with TIE = "1").	<Periodic interrupt mode (interval interrupt)> INTN goes LOW immediately when a timer interrupt occurs (with TIE = "1"), the TF bit is set to "1", and then INTN becomes high impedance until "0" data is written to the TF bit.

- AF, TF bits: Alarm Flag, Timer Flag
  The AF bit is set to "1" when an alarm occurs, and the TF bit is set to "1" when the timer is zero.
  The data bits are maintained until "0" data is written to both bits.
  Note that "1" data cannot be written to both bits.
- AIE, TIE bits: Alarm, Timer Interrupt Enable
  These bits determine the output on INTN when alarm or timer interrupt events occur.
  AIE is the alarm interrupt enable flag, and TIE is the timer interrupt enable flag.
  The alarm or timer interrupt is enabled when the corresponding enable bit is set to "1" (both interrupts are output if both bits are set to "1", so setting both bits to "1" should be avoided).

Control Register 2 (Register F)

This register controls the clock timing frequency divider.

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
F	*	TEST	*	RESET	HOLD	*	*	*

- TEST bit: NPC Test Bit
  This bit should be set to "0" when power is applied and when writing to register F.
- RESET bit
  When this bit is set to "1", the 2kHz to 1Hz frequency divider counters are reset and clock timing stops. After "1" data is written, test mode is cancelled by writing "0" data or by setting the CE input LOW.
  It is not affected by the state of any other bits.
- HOLD bit
  When this bit is set to "1", the seconds digit increment operation is disabled.
  However, if an increment operation occurs when this bit is "1" and the bit is subsequently set to "0" within 1 second, the automatic correction function forces a 1-second correction.
  Therefore, it is recommended that the HOLD bit should be used for less than 1 second.
- Functional operation table
  The function of the RESET and HOLD bits is shown in the following table.

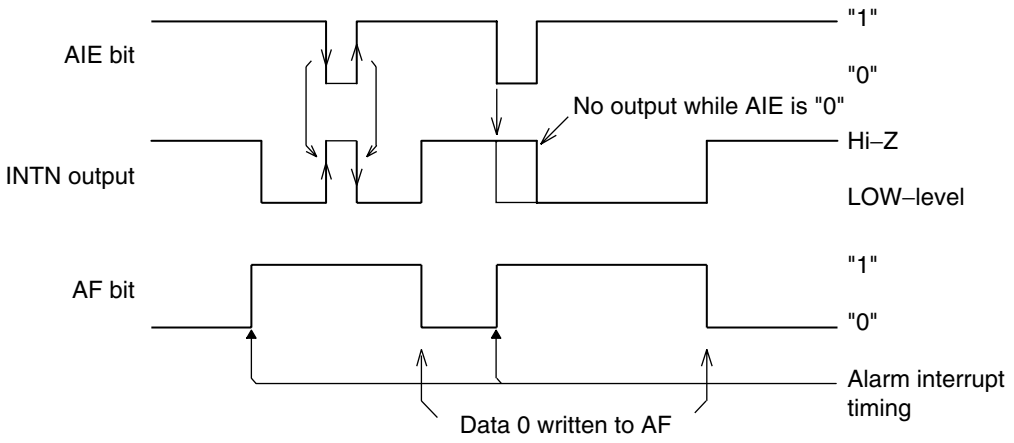
Bit		Function			
RESET	HOLD	Clock timing	Timer interrupt output	Alarm interrupt output	Arbitrary frequency output
0	0	Operating	Operating	Operating	Operating
0	1	*1	*2	Stopped	Operating
1	0	Stopped	*3	Stopped	*4
1	1	Stopped	*3	Stopped	*4

*1. The automatic correction function operates if the HOLD bit is set for less than 1 second.
*2. Normal operation for source clocks other than 1/60Hz (1 minute).
*3. Normal operation for 4096Hz source clock only.
*4. Normal operation for 32768Hz source clock only.

INTERRUPT HANDLING

Alarm Interrupt

- If AIE = 1 when the alarm occurs, output INTN goes LOW. If AIE = 0, INTN is in high impedance state.
- The alarm interrupt is output when the 10s seconds digit carries over to the minutes digit.

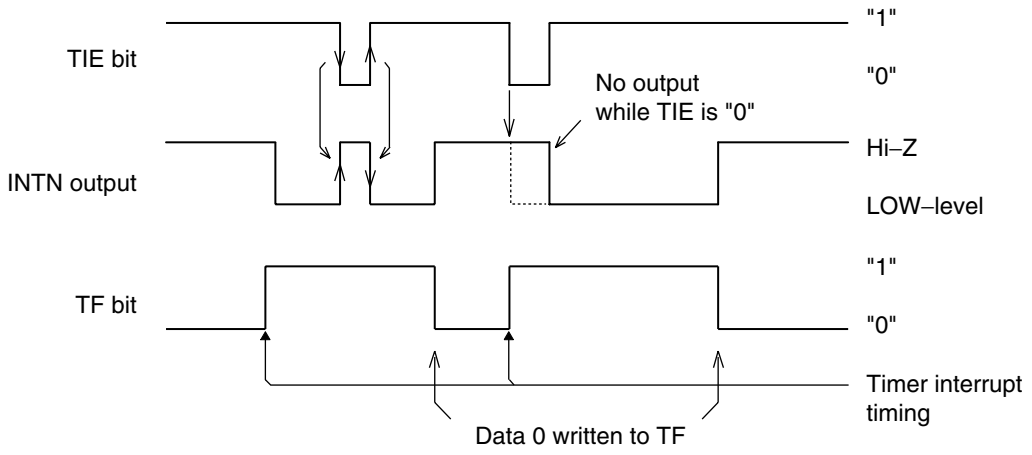


Timer Interrupt

- The TI/TP bit setting selects either level interrupt mode or periodic interrupt mode output (with the AIE and FE bits set to “0”).

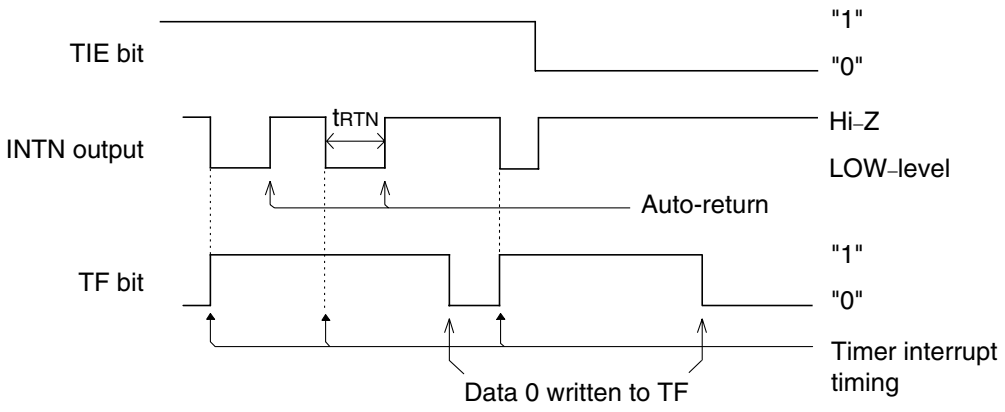
(1) Level interrupt mode (TI/TP = “0”)

- If TIE = “1” when the interrupt occurs, output INTN goes LOW. If TIE = “0”, INTN is in high impedance state.



(2) Periodic mode (TI/TP = “1”)

- If TIE = “1” when the interrupt occurs, output INTN goes LOW.
- If TIE = “0” when the interrupt occurs, output INTN stays high impedance and the TF bit is set to “1”, and this condition is maintained.



* Auto-return: The auto-return time (t_{RTN}) is determined by the source clock set by register C.

Source clock	Auto-return time (t_{RTN})
4096Hz	0.122ms
64Hz	7.81ms
1Hz	0.5s
1/60Hz	0.122ms

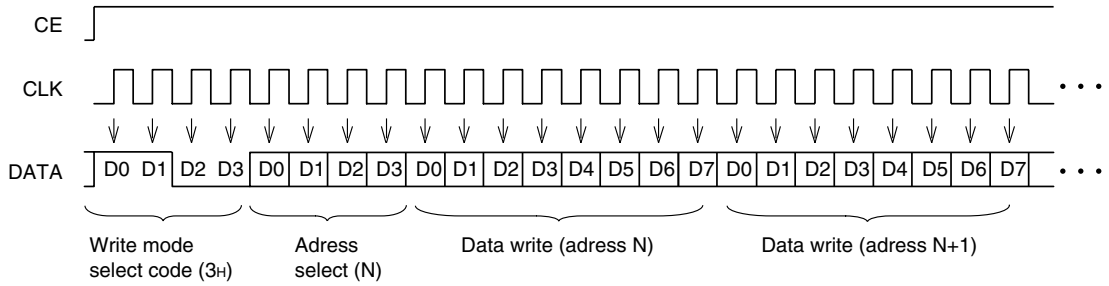
USAGE NOTES

Data Read/Write

- For both writing and reading data, the first 4 bits after CE goes HIGH are mode select bits, the next 4 bits assign the address, and subsequent bits are read/write data in 8-bit units.
- When writing data, the data must be input in 8-bit units.
- If CE goes LOW before an 8-bit unit data word is input, the 8-bit data being written when CE goes LOW will not be written correctly.
- Write data and read data are in LSB-first format.

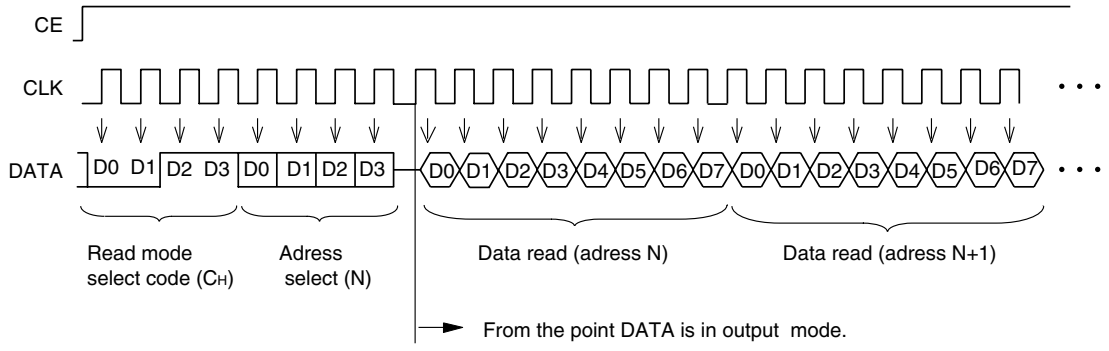
[Write mode]

1) If the first 4 bits after CE goes HIGH have value "3", write mode is selected. The next 4 bits determine the write address.
2) The next 8-bit data unit is written to the write address, and subsequent 8-bit data units are written to consecutive locations addressed using an automatic address increment function.
3) The address automatic increment function is cyclical, with address 0 following after address F.



[Read mode]

1) If the first 4 bits after CE goes HIGH have value "C", read mode is selected. The next 4 bits determine the read address.
2) The next 8-bit data unit is read from the read address, and subsequent 8-bit data units are read from consecutive locations addressed using an automatic address increment function.
3) The address automatic increment function is cyclical, with address 0 following after address F.



Note. If the mode set code is neither "C" nor "3", all subsequent data is ignored and the DATA pin input state is maintained.

Alarm Interrupt

Alarms can be set for day, day-of-week, hour, and minute. Also, multiple day-of-week alarms can be set.
It is recommended that the AF bit and AIE bit be initialized to "0" to avoid unexpected hardware interrupts during the alarm setting procedure. Subsequent alarm data can be set and then the AF flag can be reset to zero for reliable initialization. Then the AIE bit should be set to "1". If hardware interrupts are never used, the AIE should be set to "0" and the AF bit should be monitored using software as necessary.

Example 1) Alarm output for 6pm tomorrow:

- Write "0" to AIE bit, and "0" to AF bit.
- Write "1" to day alarm AE bit.
- Write register 3's current day-of-week data left-shifted by 1 bit into the day-of-week alarm register. If bit 6 in register 3 is "1", left shift into the fr bit is not allowed. Instead, write "01h" (Sunday).
- Write "18h" to the hour alarm register.
- Write "00h" to the minute alarm register.
- Reset the AF bit to zero.
- Write "1" to the AIE bit.

Example 2) Alarm output for 6am every day excluding Saturday and Sunday:

- Write "0" to AIE bit, and "0" to AF bit.
- Write "1" to day alarm AE bit.
- Write "3Eh" to the day-of-week alarm register.
- Write "06h" to the hour alarm register.
- Write "00h" to the minute alarm register.
- Reset the AF bit to zero.
- Write "1" to the AIE bit.

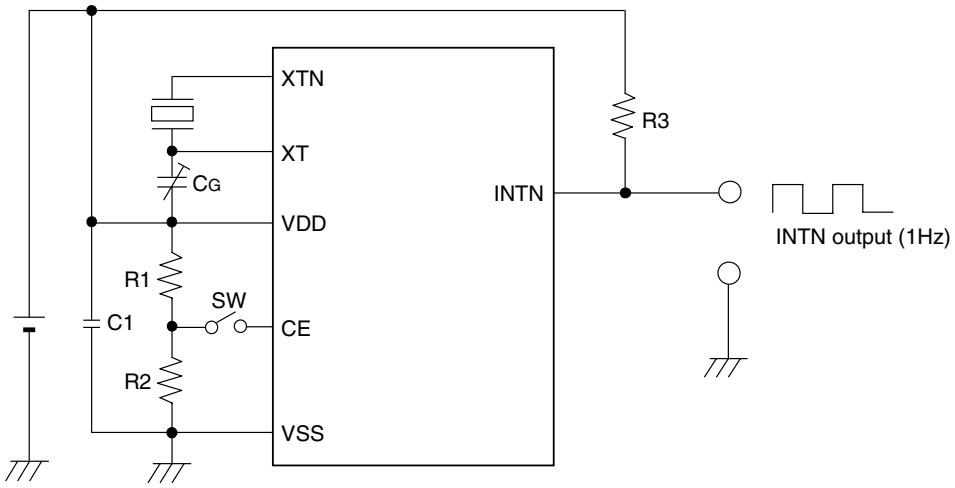
Interrupt Output (INTN)

- The INTN output mode can be selected, by internal mode setting, for timer interrupt output, alarm interrupt output, or arbitrary frequency output.
- The output mode setting is set by the TIE, AIE, and FE bits as shown in the following table. Note that multiple "1" bits are invalid.

Mode	Bit		
	TIE	AIE	FE
Timer interrupt output	1	0	0
Alarm interrupt output	0	1	0
Arbitrary frequency output	0	0	1
Output disabled	0	0	0

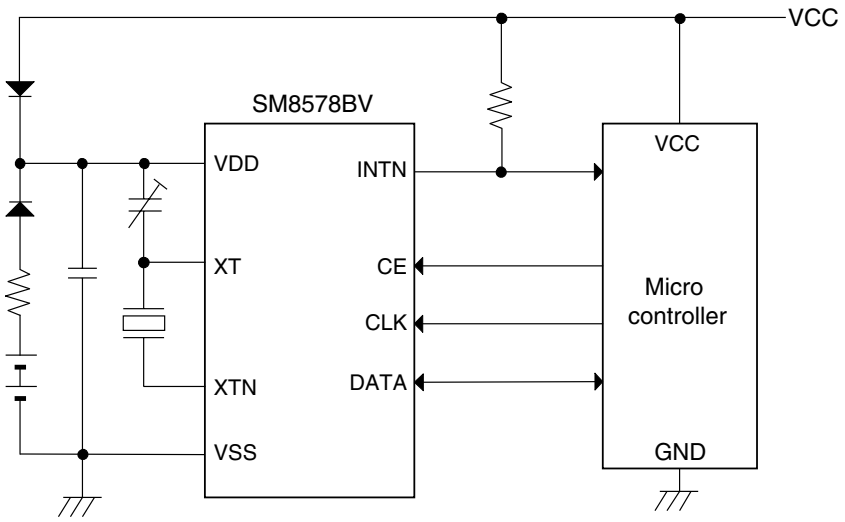
Monitoring Oscillator Frequency

A 1Hz signal is output from INTN when input CE is biased to $1/2V_{DD}$.
By monitoring this output, the oscillator frequency can be adjusted by tuning an external capacitor (C_G).



R1 = R2 (≈ 10kΩ)
R3 ≈ 10kΩ
C1 ≈ 0.1µF

TYPICAL APPLICATION CIRCUIT



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NC9619EE 2006.04