SM6451B

Audio Variable Volume IC

OVERVIEW

The SM6451B is a 3-wire serial-controlled electronic variable volume IC for audio applications. It provides electronic volume control for a stereo system (left and right channels), and independent channel attenuation and muting, with greatly enhanced digital zip noise suppression. The chip address function allows up to four SM6451B devices to be connected and individually controlled over the 3-wire control interface from a single CPU. It is available in 16-pin TSSOP packages.

FEATURES

- Stereo inputs and outputs
- Attenuation function
  - 2-channel independent control
  - 1.0dB/step over 80 steps
  - 0 to −80dB range
- Mute function
- 3-wire serial data control (MDT, MCK, MLEN)
- Chip addressing (up to 4 devices can be connected in parallel)
- Low noise
  - 0.003% THD + noise
  - 12μVrms residual noise
- 2.5 to 3.6V single power supply
- Silicon-gate CMOS process
- Package: 16-pin TSSOP (Pb free)

APPLICATIONS

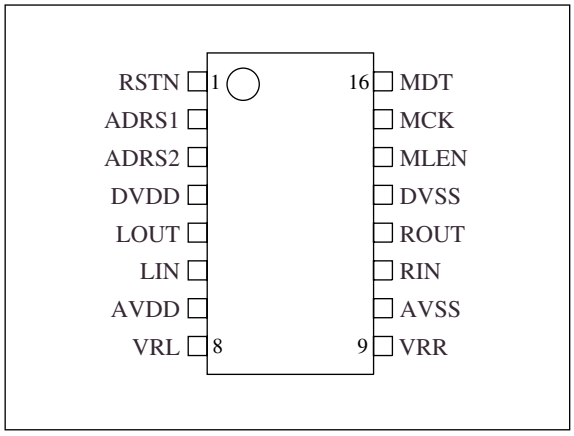
- Audio equipment

ORDERING INFORMATION

Device	Package
SM6451BT	16-pin TSSOP

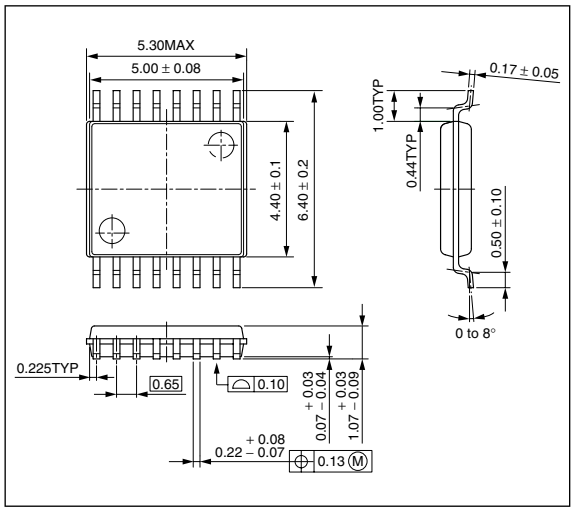
PINOUT

(Top view)

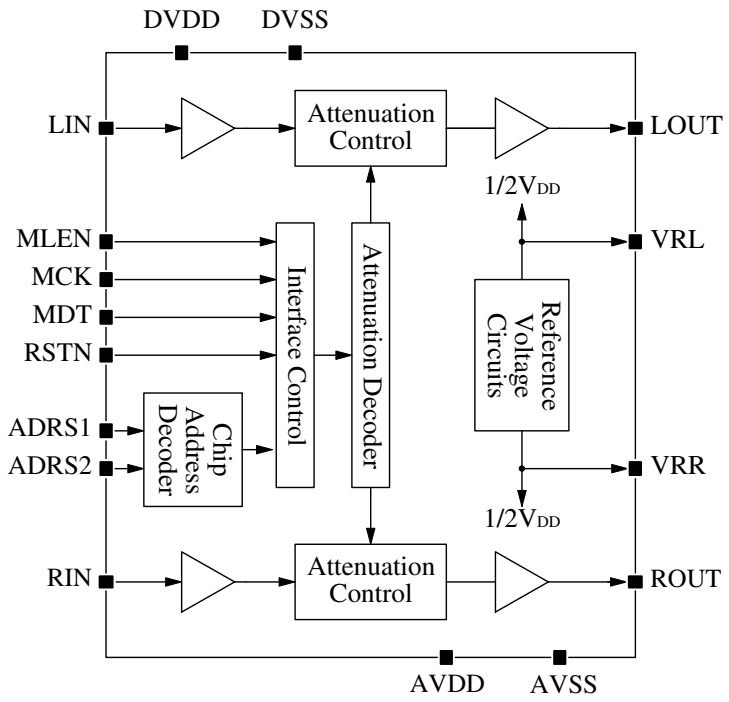


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O[1]	A/D[1]	Description
1	RSTN	Ip	D	System reset input (LOW-level reset)
2	ADRS1	Ip	D	Chip address set 1
3	ADRS2	Ip	D	Chip address set 2
4	DVDD	–	D	Digital supply
5	LOUT	O	A	Left-channel audio output
6	LIN	I	A	Left-channel audio input
7	AVDD	–	A	Analog supply
8	VRL	O	A	Left-channel reference voltage ($0.5V_{DD}$). Connect a 10µF capacitor between VRL and AVSS.
9	VRR	O	A	Right-channel reference voltage ($0.5V_{DD}$). Connect a 10µF capacitor between VRR and AVSS.
10	AVSS	–	A	Analog ground
11	RIN	I	A	Right-channel audio input
12	ROUT	O	A	Right-channel audio output
13	DVSS	–	D	Digital ground
14	MLEN	Ip	D	Microcontroller latch enable input
15	MCK	Ip	D	Microcontroller clock input
16	MDT	Ip	D	Microcontroller data input

1. Ip = input pin with pull-up, A = analog, D= digital

SPECIFICATIONS

Absolute Maximum Ratings

DVSS = AVSS = 0V, DVDD = AVDD = V_{DD}

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	150	mW
Storage temperature	T_{stg}	–55 to 125	°C

Note. Rating applies at power-ON and power-OFF.

Recommended Operating Conditions

DVSS = AVSS = 0V, DVDD = AVDD = V_{DD}

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	2.5 to 3.6	V
Supply voltage deviation	$DV_{DD} – AV_{DD}$, $DV_{SS} – AV_{SS}$	±0.1	V
Operating temperature	T_{opr}	–40 to 85	°C

DC Characteristics

DVDD = AVDD = V_{DD} = 2.5 to 3.6V, V_{SS} = 0V, Ta = –40 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD Current consumption	I_{DDD1}	Data transfer stopped, MDT, MCK, MLEN, RSTN, ADRS1, ADRS2 = V_{DD}	–	0.2	1.0	µA
	I_{DDD2}	ADRS1 = ADRS2 = 0V, 0.8Vrms analog input, ATT = 0dB, data transfer active	–	0.4	1.0	mA
AVDD Current consumption	I_{DDA}		–	1.9	5.5	mA
HIGH-level input voltage[1]	V_{IH}		$0.7V_{DD}$	–	–	V
LOW-level input voltage[1]	V_{IL}		–	–	$0.3V_{DD}$	V
Input current[1]	I_{IL}	V_{IN} = 0V	–	70	150	µA
Input leakage current[1]	I_{IH}	$V_{IN} = V_{DD}$	–	–	1.0	µA

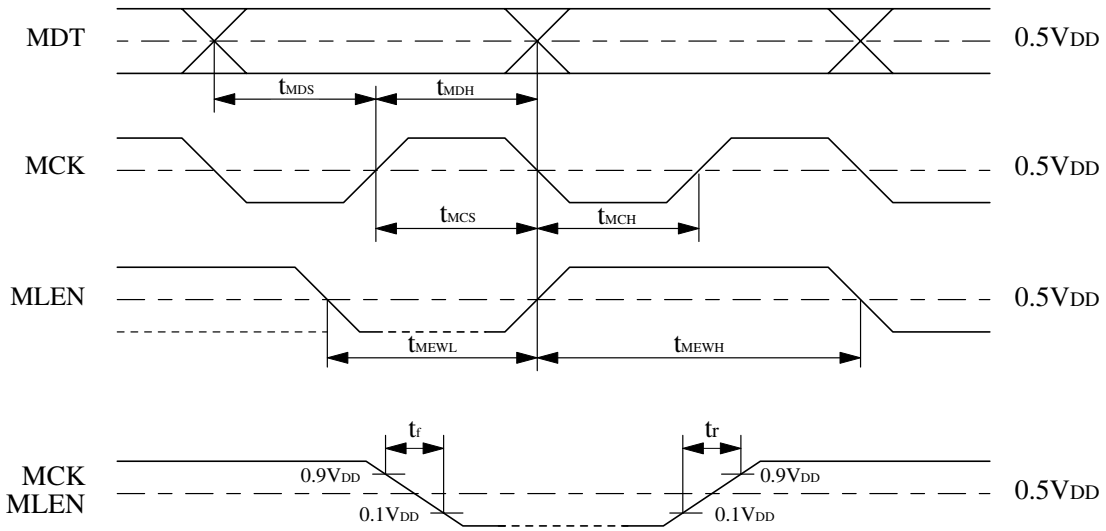
1. MDT, MCK, MLEN, RSTN, ADRS1, ADRS2

AC Digital Characteristics

DVDD = AVDD = V_{DD} = 2.5 to 3.6V, V_{SS} = 0V, Ta = –40 to 85°C

Serial inputs (MDT, MCK, MLEN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
MCK, MLEN rise time	t_r	–	–	100	ns
MCK, MLEN fall time	t_f	–	–	100	ns
MCK pulse cycle	t_{MCK}	100	–	10000	ns
MDT setup time	t_{MDS}	50	–	–	ns
MDT hold time	t_{MDH}	50	–	–	ns
MLEN setup time	t_{MCS}	50	–	–	ns
MLEN hold time	t_{MCH}	50	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	16	–	–	t_{MCK}
MLEN HIGH-level pulsewidth	t_{MEWH}	50	–	5000	ns



Reset input (RSTN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	100	–	–	ns

AC Analog Characteristics

V_{DD} = 3.0V, 0.8Vrms amplitude, 1kHz input frequency, 100kΩ output load resistance, Ta = 25°C, AC-coupled inputs

Analog inputs (LIN, RIN)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference input amplitude	V_{AI}		–	0.8	–	Vrms
Input resistance	R_{IN}		40	50	60	kΩ
Input clipping voltage	V_{CLP}	THD + N = 1%, ATT = 0dB	–	1.1	–	Vrms

Analog outputs (LOUT, ROUT)

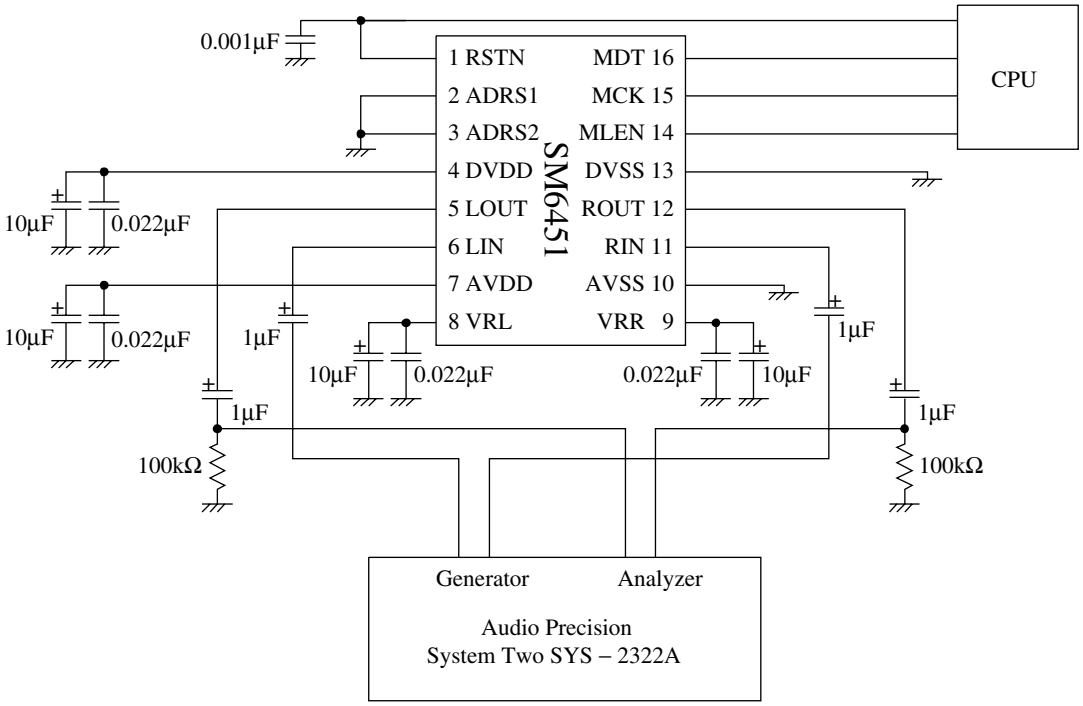
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Residual noise voltage	V_{NS}	Input signal: 0Vrms, A-weight filter, 0dBr = 0.8Vrms, ATT = 0dB	–	12	20	μVrms
Signal-to-noise ratio	SNR		92	96	–	dBr
Total harmonic distortion + noise	THD + N	ATT = 0dB, 20kHz lowpass filter	–	0.0025	0.005	%
Gain control range	R_{CNT}		– 80	–	0	dB
Step size	Step		0.8	1.0	1.8	dB
Attenuation error (1k to 20kHz)	ERR_1	0 to –60dB	– 2	–	1	dB
	ERR_2	–61 to –80dB	– 6	–	0	dB
Absolute attenuation (1kHz)	AT_0	ATT = 0dB	–	– 0.0	–	dB
	AT_2	ATT = –20dB	–	– 20.0	–	dB
	AT_4	ATT = –40dB	–	– 40.0	–	dB
	AT_6	ATT = –60dB	–	– 60.4	–	dB
	AT_8	ATT = –80dB	–	– 84.2	–	dB
Mute attenuation (1kHz)	Mute	ATT = Mute	– 85.0	– 88.0	–	dB
Channel crosstalk	CT	ATT = 0dB	– 103	– 105	–	dB
Frequency response	FR	ATT = 0dB, f = 200kHz	– 10	– 8	–	dB
Quiescent output zip noise voltage (while ATT value adjusting)	N_J	0Vrms input	–	–	3	mV
Minimum driver load resistance	R_{ML}	ATT = 0dB, THD + N = 1%	–	8	12	kΩ

Reference voltage (VRL, VRR)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference voltage output	V_{REF}		$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V

MEASUREMENT CIRCUIT

Chip address: ADRS1 = LOW, ADRS2 = LOW



MICROCONTROLLER INTERFACE

The SM6451B uses a 3-wire serial interface comprising MDT (data), MCK (clock) and MLEN (latch enable) to select channels and attenuation levels for the addressed device.

Input Timing

The microcontroller data input timing is shown in figure 1.

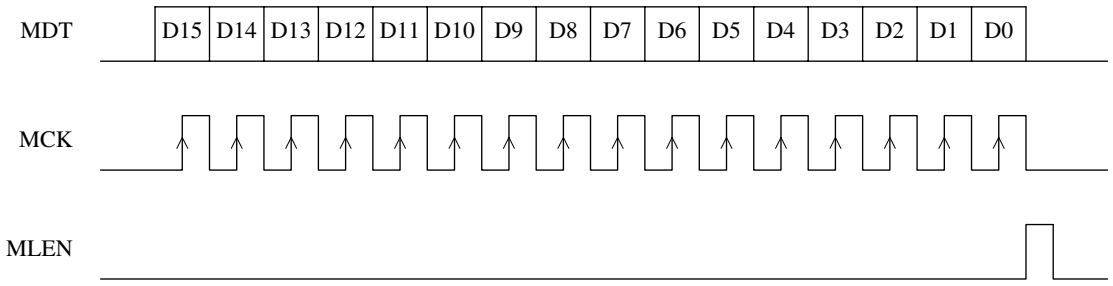


Figure 1. Microcontroller data input timing

Data is shifted into the internal shift register on the rising edge of MCK, and the attenuation value is updated on the rising edge of MLEN. Accordingly, data on MDT should be changed on the falling edge of MCK.

Note, however, a minimum of 16 MCK input pulses are required.

Data Format

The format of microcontroller input data is shown in figure 2.

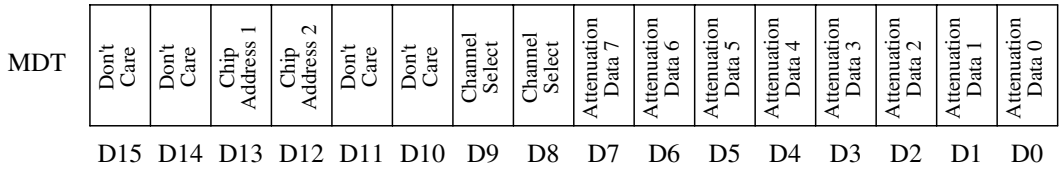


Figure 2. Microcontroller data format

D15, D14

Don’t care.

D13, D12

Chip address bits. D13 corresponds to ADRS1 and D12 corresponds to ADRS2. The device is addressed only when ADRS1:ADRS2 matches D13:D12.

Example 1: If D13 = LOW, D12 = HIGH and ADRS1 = LOW, ADRS2 = LOW, then the device is not addressed since ADRS2 and D12 do not match.

Example 2: If D13/D12 = LOW and ADRS1/ADRS2 = LOW, then the device is addressed and all input data is read and the attenuation settings updated.

D11, D10

Don’t care.

D9, D8

Channel select bits. The selected channel(s) are shown in table 1.

Table 1. Channel select

D9	D8	Selected channel
LOW	LOW	Both left and right channels
LOW	HIGH	Left channel
HIGH	LOW	Right channel
HIGH	HIGH	No change

D7 to D0

Attenuation register (ATT) set bits.

Table 2. Attenuation setting

Attenuation	ATT_H	D7	D6	D5	D4	D3	D2	D1	D0
0 dB	00	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
−1 dB	01	LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH
−2 dB	02	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	LOW
:	:	:	:	:	:	:	:	:	:
−15 dB	0F	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	HIGH
−16 dB	10	LOW	LOW	LOW	HIGH	LOW	LOW	LOW	LOW
−17 dB	11	LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH
:	:	:	:	:	:	:	:	:	:
−63 dB	3F	LOW	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
−64 dB	40	LOW	HIGH	LOW	LOW	LOW	LOW	LOW	LOW
−65 dB	41	LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH
:	:	:	:	:	:	:	:	:	:
−79 dB	4F	LOW	HIGH	LOW	LOW	HIGH	HIGH	HIGH	HIGH
−80 dB	50	LOW	HIGH	LOW	HIGH	LOW	LOW	LOW	LOW
Mute	51	LOW	HIGH	LOW	HIGH	LOW	LOW	LOW	HIGH
Mute	52	LOW	HIGH	LOW	HIGH	LOW	LOW	HIGH	LOW
:	:	:	:	:	:	:	:	:	:
Mute	FE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW
Mute	FF	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

Note. Outputs are muted after system reset.
Attenuation error is changed dependent on the supply voltage when attenuation level is under – 60dB. In the case of the supply voltage being under 2.6V, mute level inverses up to the same level of – 80dB setting or more. (see Figure 6)

ANALOG PERFORMANCE CHARACTERISTICS

DVDD = AVDD = 3.0V, 100kΩ output load resistance, Ta = 25°C

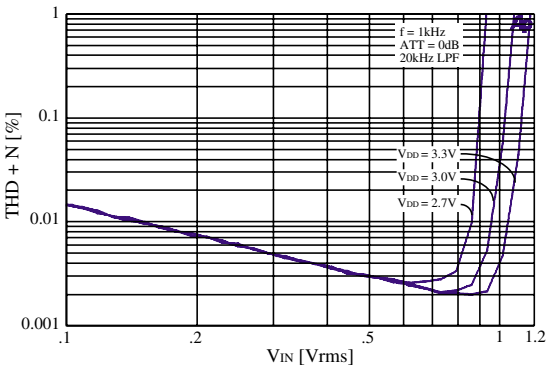


Figure 3. THD + N vs. input amplitude

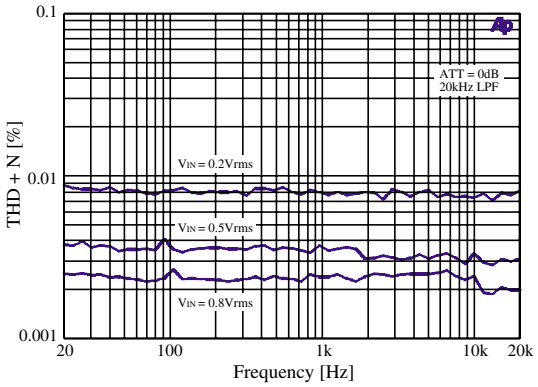


Figure 4. THD + N vs. input frequency

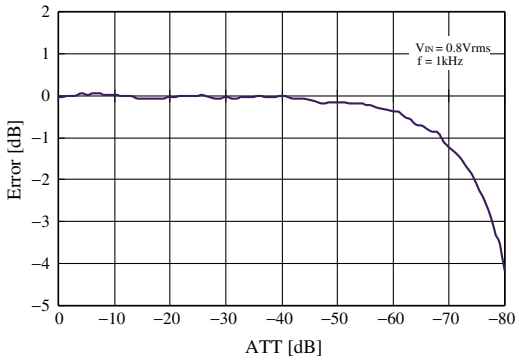


Figure 5. Attenuation error

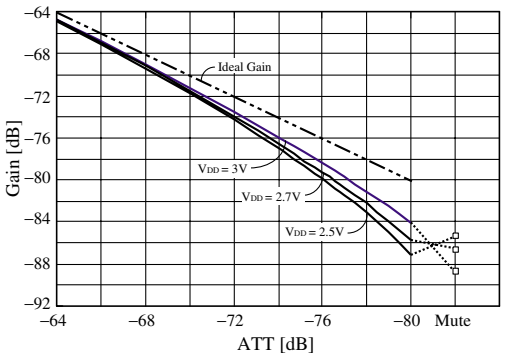


Figure 6. Attenuation characteristic (– 64dB to MUTE)

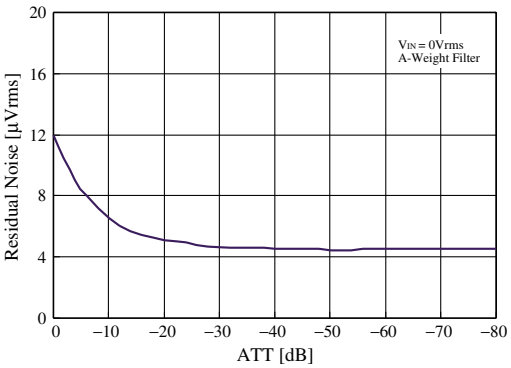


Figure 7. Residual noise vs. ATT

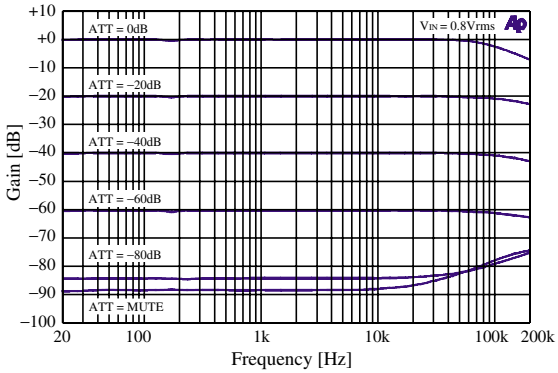


Figure 8. Frequency response

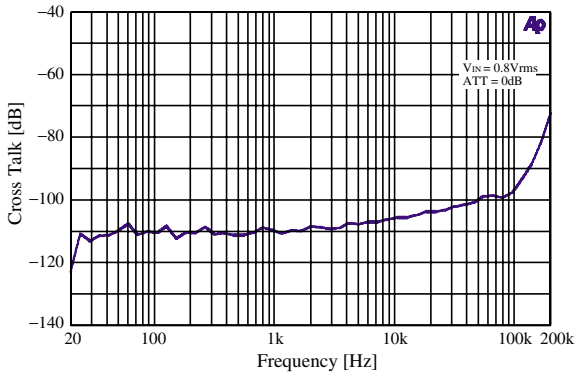


Figure 9. Crosstalk frequency response

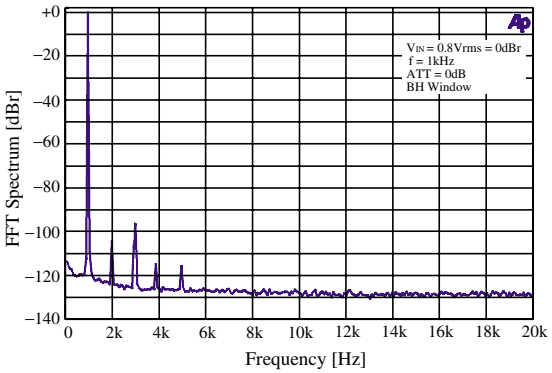


Figure 10. FFT spectrum

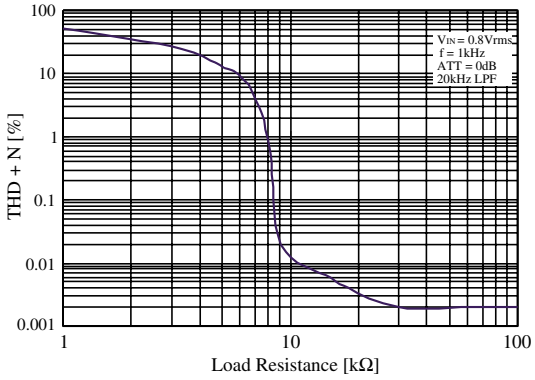


Figure 11. THD + N vs. load resistance

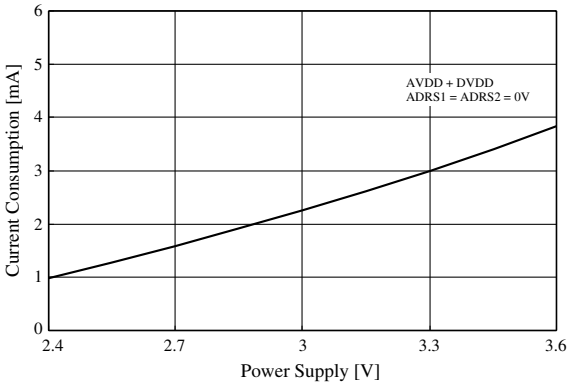


Figure 12. Current consumption vs. supply voltage

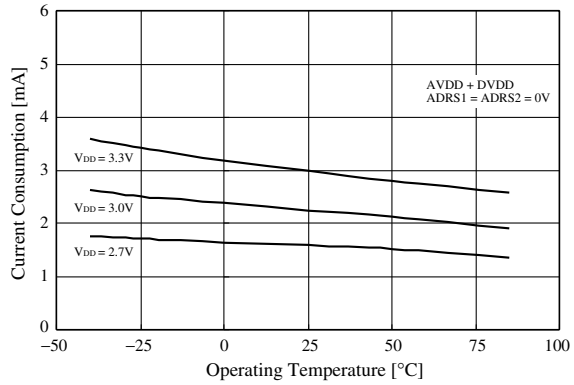


Figure 13. Current consumption vs. operating temperature

TYPICAL APPLICATIONS

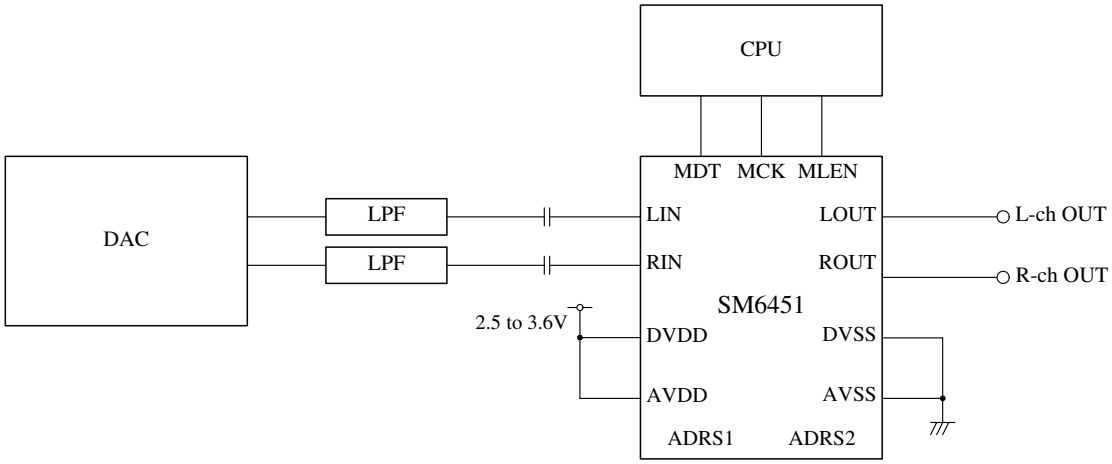
Connection Guidelines

Decoupling capacitors of approximately 10µF should be connected from AVDD, VRL, VRR to AVSS, and from DVDD to DVSS.

In addition, approximately 0.01µF capacitors should also be connected from AVDD, VRL, VRR to AVSS, and from DVDD to DVSS to suppress digital switch noise.

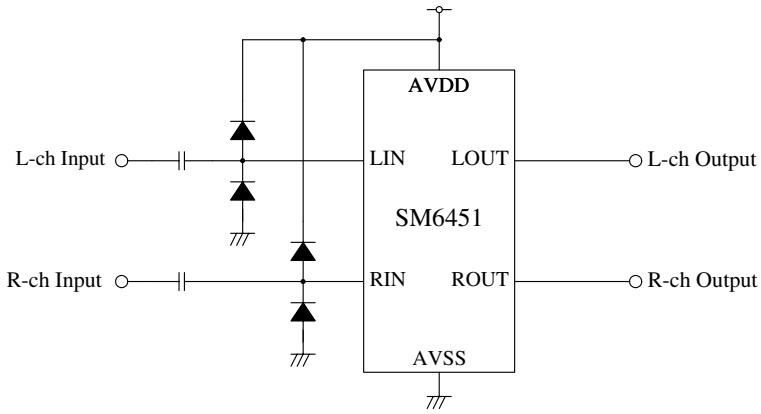
An approximately 0.001µF capacitor connected from RSTN to DVSS will force a system reset when power is applied.

Connection 1 (to DAC)



Connection 2

When there is a possibility that the input peak-to-peak amplitude will exceed the supply voltage, input protection diodes should be connected to prevent device breakdown.



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