OVERVIEW

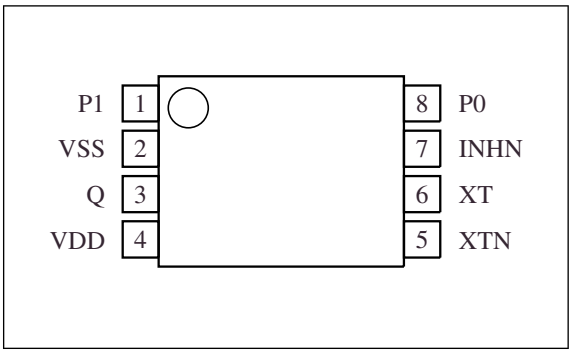
The SM5050A is a single-output clock generator IC that generates standard high-frequency clocks derived from a 20 to 40MHz crystal oscillator master clock. The high-frequency output stage uses optimized PLL circuits for low jitter output. The oscillator capacitors C_G and C_D are built-in, realizing a high-frequency output oscillator by just the connection of a crystal. Two program inputs allows selection from 4 frequency multipliers, making the SM5050A able to generate multi-standard frequency clock outputs.

FEATURES

- 2.7 to 3.6V operating supply voltage
- 20 to 40MHz master clock frequency (fundamental)
- Output frequency ranges
  - 100 to 166.6MHz (V_{DD} = V_{DDQ} = 3.0 to 3.6V)
  - 100 to 125MHz (V_{DD} = V_{DDQ} = 2.7 to 3.6V)
- 8mA output drive capability
- Oscillator capacitors (C_G, C_D) and feedback resistor (R_f) built-in
- 100ps (typ) low jitter output (peak-to-peak)
- 2 program inputs for 4 selectable multiplier ratios
- Standby function
- Packaging
  - Chip form (CF5050A)
  - 8-pin VSOP package (SM5050AV)

PINOUT

(Top view)

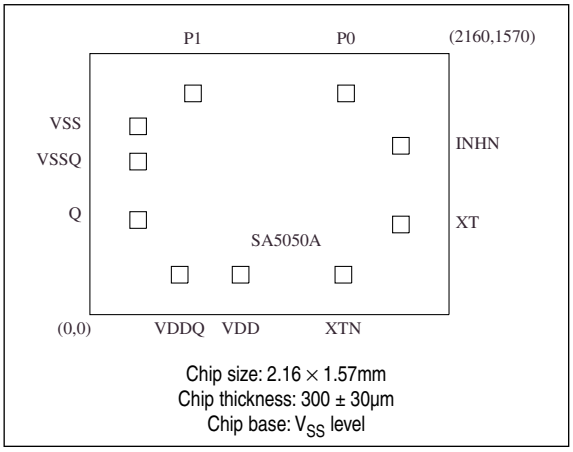


ORDERING INFORMATION

Device	Package
CF5050A–1	Chip form
SM5050AV	8-pin VSOP

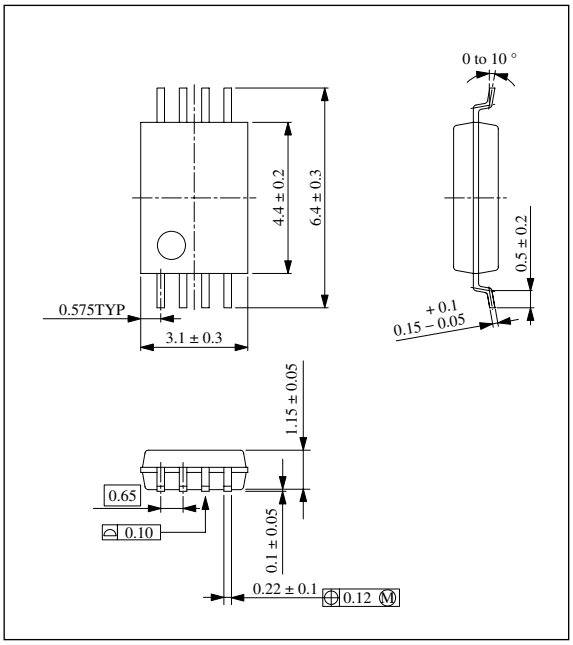
PAD DIMENSIONS

(Unit: µm)

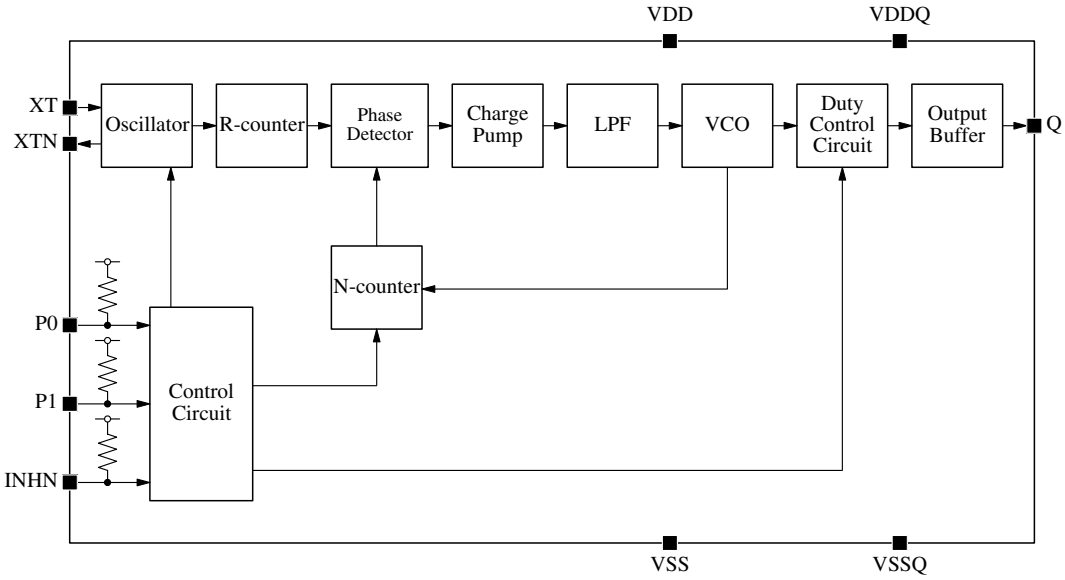


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

SM5050AV		CF5050A			I/O[1]	Description
Number	Name	Name	Pad dimensions [µm]			
			X	Y		
1	P1	P1	620	1330	Ip	Program input 1. Selects the output frequency multiplier ratio.
2	VSS	VSS	290	1132	–	Ground
		VSSQ	290	920	–	Output circuit ground
3	Q	Q	290	569	O	Output (CMOS)
4	VDD	VDDQ	540	240	–	Output circuit supply
		VDD	906	240	–	Supply
5	XTN	XTN	1524	240	O	Crystal oscillator connection pins. Crystal connected between XT and XTN.
6	XT	XT	1870	542	I	
7	INHN	INHN	1870	1015	Ip	Operating state control (inhibit). When INHN is LOW, output is high impedance and PLL circuits stop.
8	P0	P0	1540	1330	Ip	Program input 0. Selects the output frequency multiplier ratio.

1. Ip = input with built-in pull-up resistor.

OUTPUT FREQUENCY SETTINGS

Program inputs		Multiplier ratio	Master clock frequency [MHz]	Output frequency [MHz]	Supply voltage [V]
P0	P1				
LOW	LOW	× 4	25.00	100	2.7 to 3.6
LOW	HIGH	× 4.25	25.00	106.25	
HIGH	LOW	× 5	25.00	125	
			26.66	133.3	3.0 to 3.6
HIGH	HIGH	× 6.25	24.8832	155.52	
			26.66	166.6	

Note: The output frequency range is 100 to 166.6MHz. The master clock frequency can be adjusted to any value within the range 20 to 40MHz, so the master clock frequency and multiplier should be selected such that the output frequency is within the output frequency range.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.5 to 6.0	V
Input voltage range	V_{IN}		–0.5 to V_{DD} + 0.5	V
Output voltage range	V_{OUT}		–0.5 to V_{DD} + 0.5	V
Storage temperature range	T_{stg}	CF5050A	–65 to 150	°C
		SM5050AV	–55 to 125	°C
Operating temperature range	T_{opr}		–40 to 85	°C
Output current	I_{OUT}		25	mA
Power dissipation	P_D	SM5050AV	150	mW

Recommended Operating Conditions

V_{SS} = 0V, f_{OUT} = 100 to 166.6MHz, C_L = 15pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Operating supply voltage	V_{DD}	$f_{OUT} \leq$ 125MHz	2.7	–	3.6	V
		$f_{OUT} \leq$ 166.6MHz	3.0	–	3.6	
Input voltage	V_{IN}		V_{SS}	–	V_{DD}	V
Operating temperature	T_{opr}		–20	–	80	°C

DC Characteristics

V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Q HIGH-level output voltage	V_{OH}	V_{DD} = 2.7V, I_{OH} = 8mA		2.2	–	–	V
Q LOW-level output voltage	V_{OL}	V_{DD} = 2.7V, I_{OL} = 8mA		–	–	0.4	V
Q output leakage current	I_Z	Measurement circuit 4, INHN = V_{SS}	V_{OH} = V_{DD}	–	–	10	µA
			V_{OL} = V_{SS}	–	–	10	
INHN HIGH-level input voltage	V_{IH1}			0.7V_{DD}	–	–	V
P0, P1 HIGH-level input voltage	V_{IH2}			0.9V_{DD}	–	–	V
INHN LOW-level input voltage	V_{IL1}			–	–	0.3V_{DD}	V
P0, P1 LOW-level input voltage	V_{IL2}			–	–	0.1V_{DD}	V
Current consumption	I_{DD}	25MHz crystal, measurement circuit 1, load circuit 1, INHN = open, C_L = 15pF, P0 = HIGH, P1 = LOW, V_{DD} = 3.0V		–	23	–	mA
		25MHz crystal, measurement circuit 1, load circuit 1, INHN = open, C_L = 15pF, P0 = HIGH, P1 = LOW		–	–	42	
Standby current	I_{ST}	INHN = V_{SS}, measurement circuit 1		–	–	40	µA
INHN, P0, P1 input pull-up resistance	R_{UP1}	V_{DD} = 3V, measurement circuit 2		0.3	–	6	MΩ
	R_{UP2}			10	–	200	kΩ
Negative resistance	$–R_L$	V_{DD} = 3V, Ta = 25°C, f = 30MHz		–	–240	–	Ω
Feedback resistance	R_f	Measurement circuit 3		100	300	900	kΩ
Internal capacitance	C_G	Design values		15.98	18.44	20.90	pF
	C_D			15.98	18.44	20.90	pF

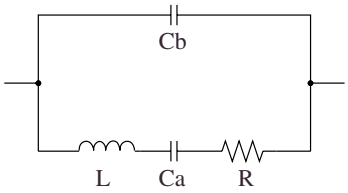
Switching Characteristics

V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_r	$0.2V_{DD} \rightarrow 0.8V_{DD}$, measurement circuit 1, load circuit 1, C_L = 15pF		–	1	2.5	ns
Output fall time	t_f	$0.8V_{DD} \rightarrow 0.2V_{DD}$, measurement circuit 1, load circuit 1, C_L = 15pF		–	1	2.5	ns
Output duty cycle	Duty	V_{DD} = 3V, Ta = 25°C, measurement circuit 1, load circuit 1, C_L = 15pF, f ≤ 166.6MHz		40	–	60	%
Output disable delay time[1]	t_{PLZ}	V_{DD} = 3V, Ta = 25°C, measurement circuit 1, load circuit 1, C_L = 15pF		–	–	100	ns
Startup time[2,3]	t_{SZL}	V_{DD} = 3V, Ta = 25°C, measurement circuit 1, load circuit 1, C_L = 15pF		–	1	–	ms
Oscillator frequency	f	Measurement circuit 1		20	–	40	MHz
Output frequency	f_{OUT}	Measurement circuit 1	V_{DD} = 2.7V	100	–	125	MHz
			V_{DD} = 3.0V	100	–	166.6	
Output clock jitter[3]	Jitter	V_{DD} = 3V, Ta = 25°C, 25MHz crystal, P0 = HIGH, P1 = LOW, measurement circuit 1, load circuit 1,C_L = 15pF, peak-to-peak		–	100	–	ps

1. Time from when INHN goes LOW until Q output goes high impedance.
2. Time from when either INHN goes LOW to HIGH or supply voltage V_{DD} = 3.0V until normal signal output.
3. Measured values using NPC characteristics standard evaluation board and standard crystal.

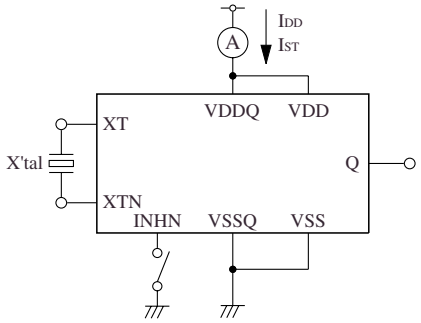
NPC STANDARD CRYSTAL DATA



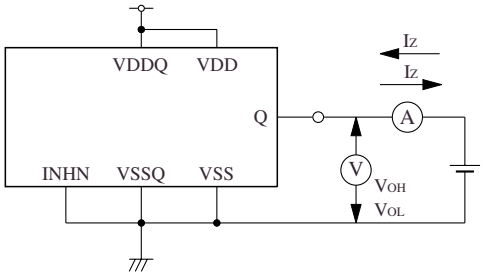
f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
25	4.368	1.885	21.52	4.793
27	7.421	2.402	14.48	4.097

MEASUREMENT CIRCUITS

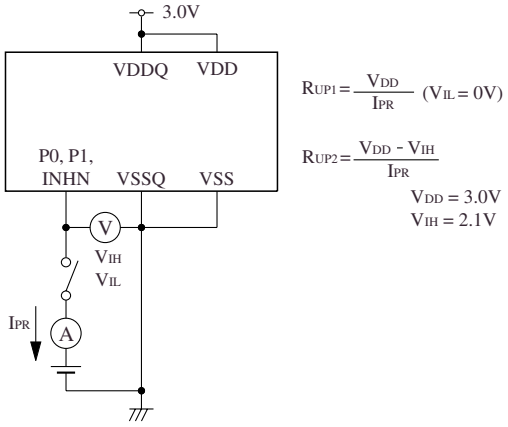
Measurement Circuit 1



Measurement Circuit 4



Measurement Circuit 2



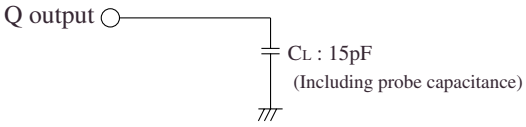
$$R_{UP1} = \frac{V_{DD}}{I_{PR}} \quad (V_{IL} = 0V)$$

$$R_{UP2} = \frac{V_{DD} - V_{IH}}{I_{PR}}$$

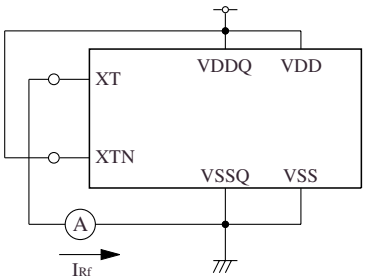
$V_{DD} = 3.0V$

$V_{IH} = 2.1V$

Load Circuit 1



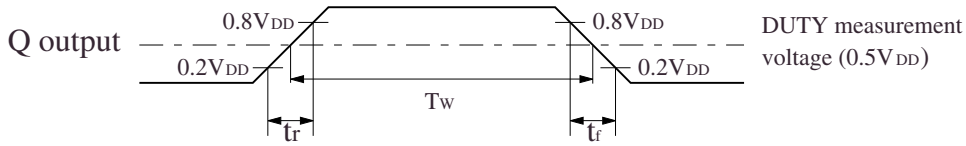
Measurement Circuit 3



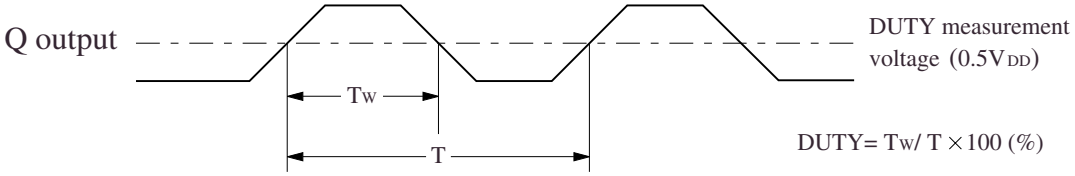
$$R_f = \frac{V_{DD}}{I_{Rf}}$$

Switching Time Measurement Waveforms

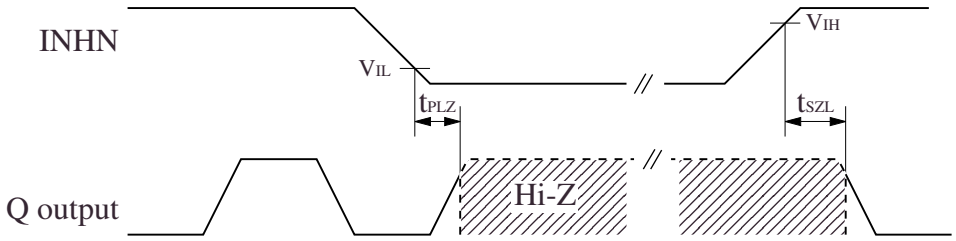
Output duty level



Output duty cycle time



Output Disable Delay Time/Startup Time



INHN input waveform $t_r = t_f \leq 10ns$

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