

1. OVERVIEW

The SM3414 is a reflective absolute linear optical encoder IC. The absolute code pattern on the scale is read optically and then output via a serial interface.

An analog incremental signal can also be output.

The device incorporates various adjustment circuits controlled via the serial interface, including adjustments for the absolute code binarization threshold voltage and the incremental signal I/V conversion gain.

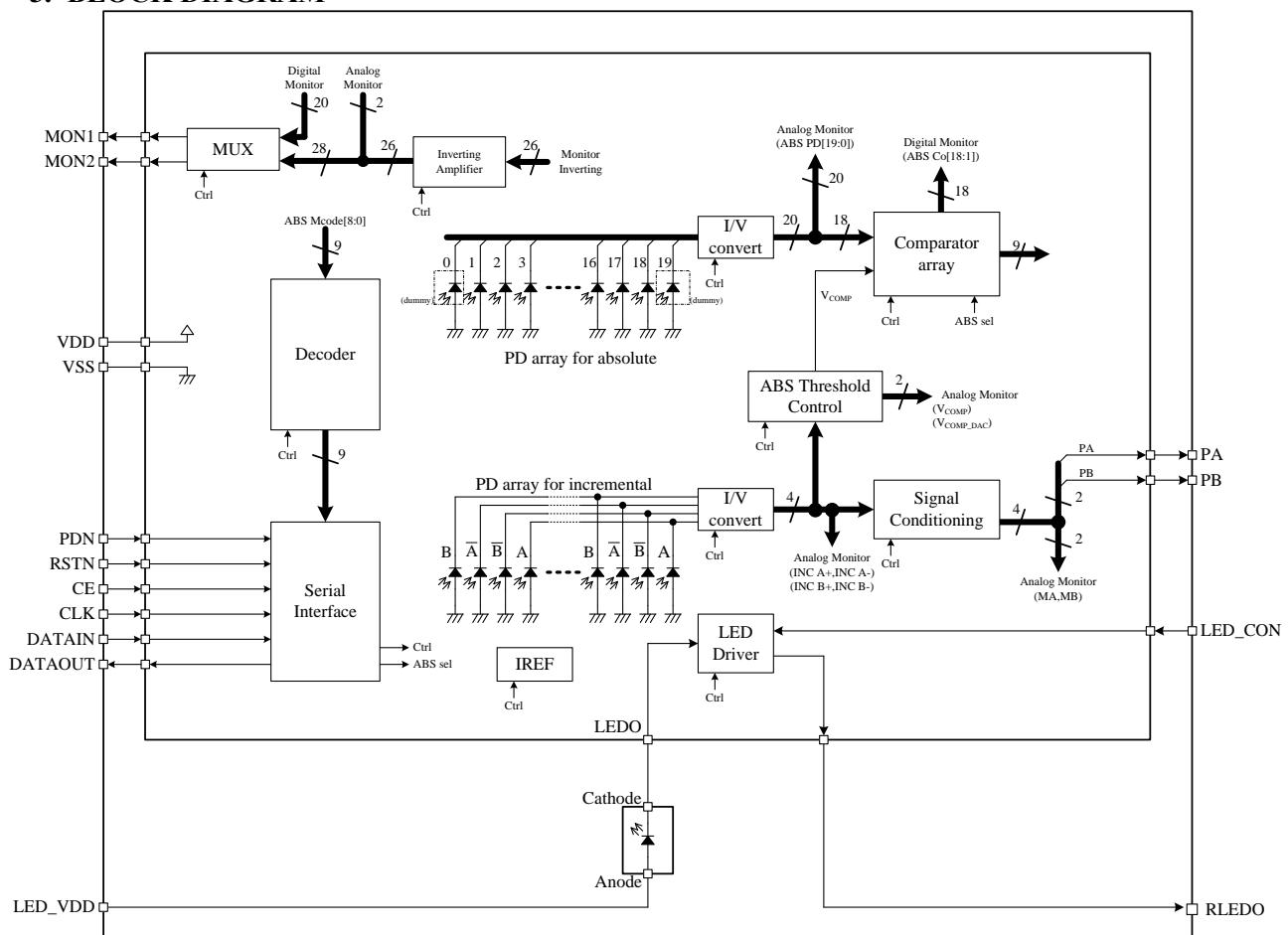
* The following abbreviations are used in this document.

Absolute: ABS, Incremental: INC, Photodiode: PD, Serial interface: SIF

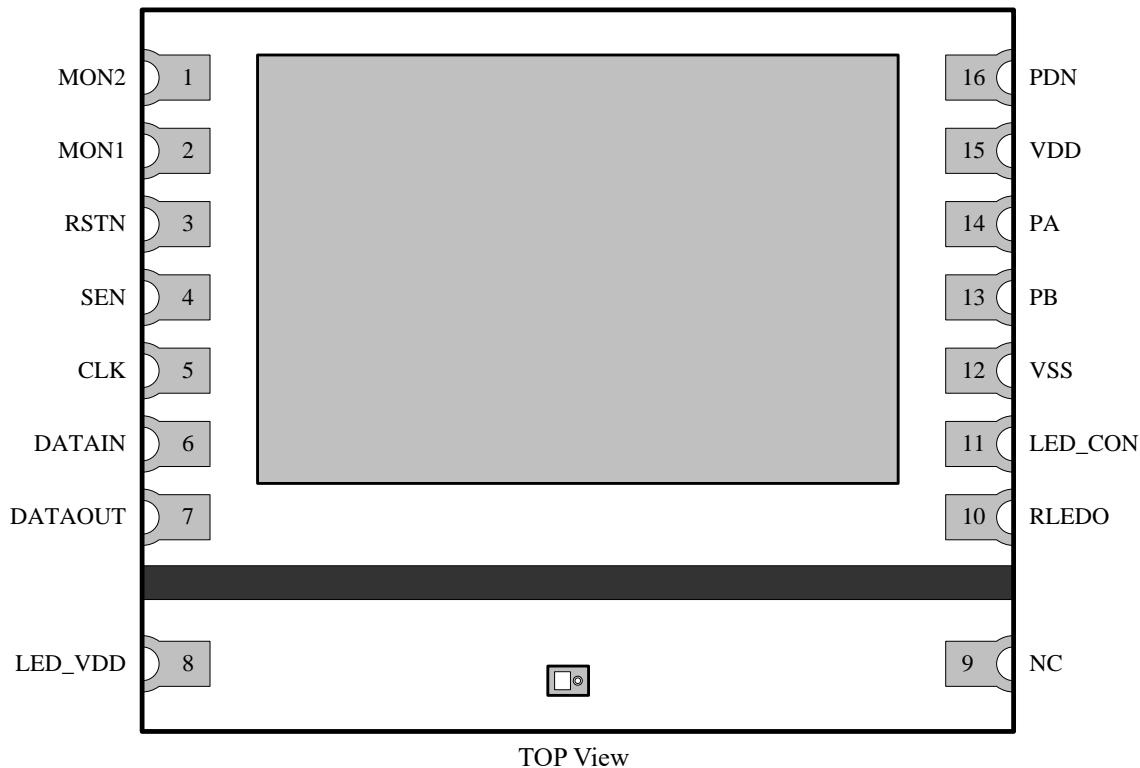
2. FEATURES

- Supply voltage : 2.7 to 3.3V
- Current consumption : 8mA (including 5mA LED current, typ. conditions)
- Operating temperature range : -30 to +70°C
- Absolute output : 51.2mm scale length, 100μm resolution (9-bit serial output), built-in decoder
- Incremental outputs : Analog phase A and phase B
- Built-in adjustment circuits : Absolute binarization voltage adjustment, Incremental signal gain adjustment
- LED wavelength : 850nm (typ.)
- Logic input 3.6V input-tolerant function
- Low-crosstalk dedicated process
- Photodiode with built-in antireflection film

3. BLOCK DIAGRAM



4. PIN LAYOUT



TOP View

5. PIN DESCRIPTION

Pin No.	Name	Type	Description
1	MON2	O	Internal signal monitor output pin 2
2	MON1	O	Internal signal monitor output pin 1
3	RSTN	I	Register reset and power-down pin (Pull-down pin, Active-Low)
4	SEN	I	Serial interface enable signal (Pull-up pin, Active-Low)
5	CLK	I	Serial interface clock signal input pin
6	DATAIN	I	Serial interface data input pin
7	DATAOUT	O	Serial interface data output pin
8	LED_VDD	S	LED power supply pin
9	NC	-	No connection
10	RLEDO	O	LED current control resistor connection pin
11	LED_CON	I	LED current adjustment pin
12	VSS	S	Ground pin
13	PB	O	Incremental signal phase B output pin
14	PA	O	Incremental signal phase A output pin
15	VDD	S	Power supply pin
16	PDN	I	Absolute function power-down pin (Pull-down pin, Active-Low)

[Type] I: Input pin, O: Output pin, S: Power supply pin

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit	Note
Supply voltage	V _{DD}	VDD, LED_VDD pins	-0.3 to 5.0	V	*1
Input voltage	V _{IN_D}	SEN, CLK, DATAIN, RSTN, PDN pins	-0.3 to 5.0	V	*1
	V _{IN_A}	LED_CON pin	-0.3 to V _{DD} +0.3	V	*1,*2
Output voltage	V _{OUT}	PA, PB, MON1, MON2, RLEDO, DATAOUT pins	-0.3 to V _{DD} +0.3	V	*1,*2
LED forward current	I _{LED}	LED_VDD pin	30	mA	
Junction temperature	T _J		125	°C	*3
Storage temperature	T _{STG}		-40 to 85	°C	*4

*1: Parameters must not exceed ratings, not even momentarily. If a rating is exceeded, there is a risk of adverse effect on electrical characteristics and reliability.

*2: "V_{DD}" in absolute maximum ratings refers to the recommended operating conditions supply voltage value (V_{DD}).

*3: Use within the rated range. If a rating is exceeded, there is a risk of deterioration in characteristics and decrease in reliability.

*4: Stored separately in Nitrogen (N₂) atmosphere or vacuum.

7. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V _{DD}	Between VDD and VSS pins	2.7	3.0	3.3	V
LED supply voltage	V _{LVDD}	Between LED_VDD and VSS pins	2.7	3.0	3.6	V
Logic input voltage	V _{IN_D}	SEN, CLK, DATAIN, RSTN, PDN pins	V _{SS}	-	3.6	V
Analog input voltage	V _{IN_A}	LED_CON pin	V _{SS}	-	V _{DD}	V
LED current	I _{LED}		-	5	20	mA
Operating temperature	T _a		-30	-	70	°C

* Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

8. ELECTRICAL CHARACTERISTICS

8.1. DC Characteristics

$V_{DD}=V_{LVDD}=3.0V$, $V_{SS}=0V$, $T_a=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Current consumption 1	I_{DD1}	No output load, RSTN=PDN=SEN= V_{DD} , CLK=DATAIN= V_{SS} , $V_{LVDD}=V_{SS}$ *INC/ABS operation, when not accessing SIF	-	3.0	8.5	mA
Current consumption 2	I_{DD2}	No output load, RSTN=SEN= V_{DD} , CLK=DATAIN=PDN= V_{SS} , $V_{LVDD}=V_{SS}$ *INC operation, ABS stopped, when not accessing SIF	-	2.5	7.0	mA
Standby-mode current consumption	I_{NOP}	No output load, CLK=DATAIN=RSTN=PDN= V_{SS} , SEN= V_{DD} $V_{LVDD}=V_{SS}$	-	-	5.0	μA
High-level logic input voltage	V_{IH}	RSTN, SEN, CLK, DATAIN, PDN pins	$V_{DD}-0.7$	-	3.6	V
Low-level logic input voltage	V_{IL}		0	-	0.3	V
High-level logic input current	I_{IH1}	$V_{IN}=3.6V$, SEN pin	-	6	50	μA
	I_{IH2}	$V_{IN}=3.6V$, CLK, DATAIN pins	-	-	1	μA
	I_{IH3}	$V_{IN}=3.6V$, RSTN, PDN pins	-	15	100	μA
Low-level logic input current	I_{IL1}	$V_{IN}=V_{SS}$, RSTN, PDN, CLK, DATAIN pins	-1	-	-	μA
	I_{IL2}	$V_{IN}=V_{SS}$, SEN pin	-100	-30	-	μA
High-level logic output voltage	V_{OH}	DATAOUT pin, $I_{OUT}=1mA$	$V_{DD}-0.5$	-	V_{DD}	V
Low-level logic output voltage	V_{OL}	DATAOUT, $I_{OUT}=-1mA$	0	-	0.5	V

8.2. Analog Circuit Electrical Characteristics

$V_{DD}=V_{LVDD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, using NPC reference scale, unless otherwise stated

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Incremental signal output frequency range	f_{OUT}	PA, PB pins, 50pF load capacitance, 100μm incremental signal cycle time	-	-	10	kHz
Incremental signal output signal amplitude	V_{APP}	PA, PB pins, 100kΩ load resistance (R), I_{LED} : 5mA ($R_{LED}=100\Omega$, $V_{LED_CON}=0.5V$) I/V conversion gain: 1 (register GA,GB[2:0]=0h *1), $D_{YAW}=0$, $D_{PTCH}=0$, $D_{ROL}=0$, $D_{CNTR}=0$, $D_{GAP}=0$	0.18	0.35	0.70	V_{P-P}

*1: See “9.12.7. Incremental Phase A/Phase B I/V conversion gain setting register (GAB[2:0]).”

8.3. Mounting Tolerance^{*2}

$V_{DD}=V_{LVDD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, using NPC reference scale, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Azimuth offset (Yaw)	D_{YAW}	Excluding dynamic fluctuations	-1.0	0	1.0	deg
		Dynamic fluctuations only	-0.15	0	0.15	deg
Pitch offset	D_{PTCH}		-1.0	0	1.0	deg
Roll offset	D_{ROL}		-1.0	0	1.0	deg
Center offset	D_{CNTR}	Including dynamic fluctuations	-0.2	0	0.2	mm
Gap offset	D_{GAP}	Gap=2.13mm (reference) ^{*3} , Excluding dynamic fluctuations	-0.1	0	0.6	mm
		Initial position (reference), dynamic fluctuations only	-0.25	0	0.25	mm

*2: These parameters are guaranteed by design. Not tested prior to shipping.

*3: The gap is the distance between the package surface and the scale.

For the definition of tolerance, see “14.1. Mounting Tolerance Definition.”

9. FUNCTIONAL DESCRIPTION

9.1. Absolute Signal Output Function

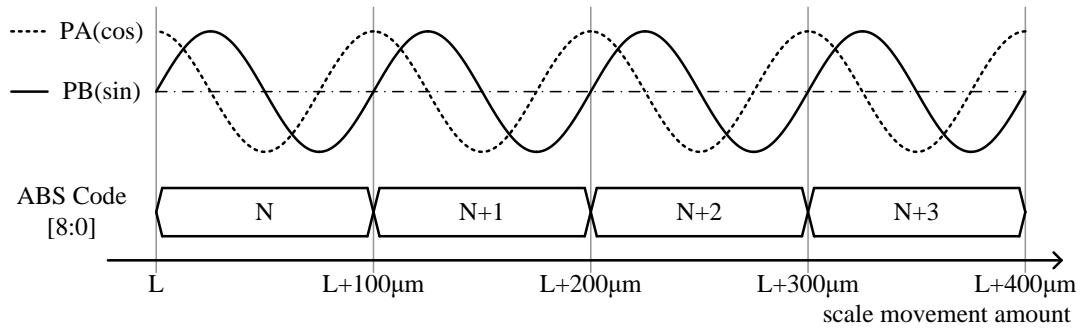
The SM3414 optically reads the reflection/non-reflection pattern from an absolute code on an external scale, decodes the M code to a binary code, and then digitally outputs the absolute signal as 9-bit data over a serial interface. The 9-bit output code can also be output as raw M code without decoding.

The absolute code has a single code assigned to each scale deviation of 100μm, which results in a maximum amount of displacement that can be measured of 51.2mm.

9.2. Incremental Signal Output Function

The SM3414 optically reads the reflection/non-reflection pattern for an incremental signal pattern from an external scale, and outputs a two-phase analog signal with a phase difference of 90 degrees from the PA and PB pins. The output sine waves are output with 0.5V_{DD} DC bias and an amplitude that varies with the detected light level.

One cycle of the incremental signal corresponds to a displacement of 100μm on the scale.

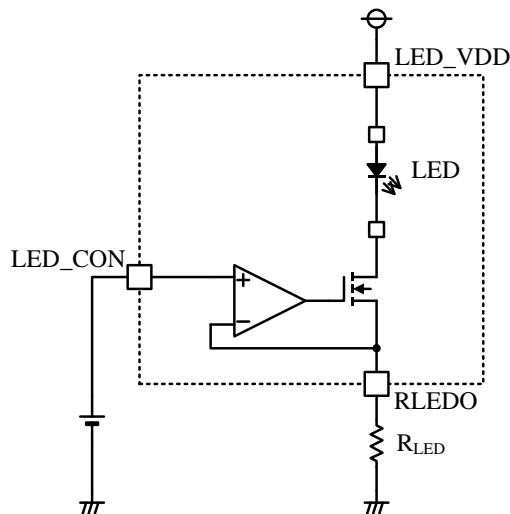


9.3. LED Current Adjustment Function

The SM3414 has a built-in LED element and LED driver, and the LED current can be adjusted by varying the voltage applied to the LED_CON pin and the resistance connected to the RLEDO pin.

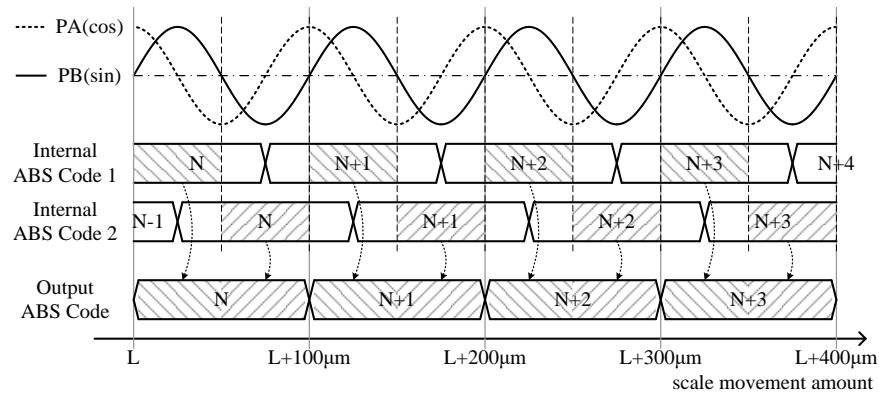
In addition, the LED_VDD supply voltage is provided separately from the VDD pin. If the LED was driven from only the V_{DD} voltage, the LED current control range is reduced by the forward voltage V_F across the LED. However, a voltage higher than V_{DD} can be applied to the LED_VDD pin to alleviate this problem.

$$\text{LED current } [A] = \frac{\text{LED_CON voltage } [V]}{\text{RLED } [\Omega]}$$



9.4. Absolute Signal, Phase Select Function

The SM3414 receives the reflected light of 1-bit absolute code as an “internal ABS code 1” and “internal ABS code 2” using two 0.5-bit wide photodiodes. By selecting either “internal ABS code 1” or “internal ABS code 2” in realtime depending on the state of the incremental signal, it is possible to obtain a stable output by avoiding the region where the photodiode output is unstable while it is transitioning to the next code.



ABS code selection

To read ABS codes:

- Select internal ABS code 1 when PB is High.
- Select internal ABS code 2 when PB is Low.

“Internal ABS code 1” is a code in which 1-bit wide light of ABS code reflected from the scale is detected by a 0.5-bit wide photodiode on the LSB side, and “internal ABS code 2” is a code in which 1-bit wide light of ABS code reflected from the scale is detected by a 0.5-bit wide photodiode on the MSB side.

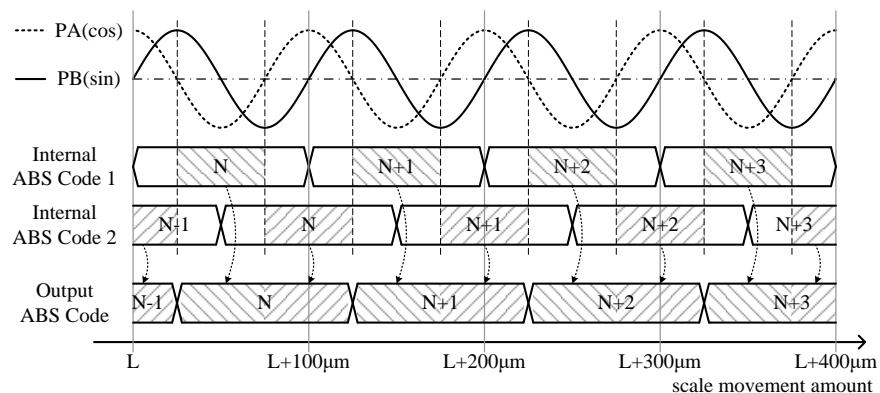
Stable output can be obtained by selecting and reading “Internal ABS code 1” when the PB component of the incremental signal is higher than the midpoint potential, and “Internal ABS code 2” when the PB component is lower than the midpoint potential.

In the arrangement above, if the phase relationship between the absolute signal and incremental signal is offset due to a physical offset in the mounting positions of the SM3414 and the scale (an offset of $\pm 90^\circ$ or more for an incremental cycle of 360° in the figure above^{*1}), only the unstable range will be output instead of the intended function.

To avoid this, it is necessary to select and read the internal ABS codes according to the offset, considering the phase information of the incremental signal.

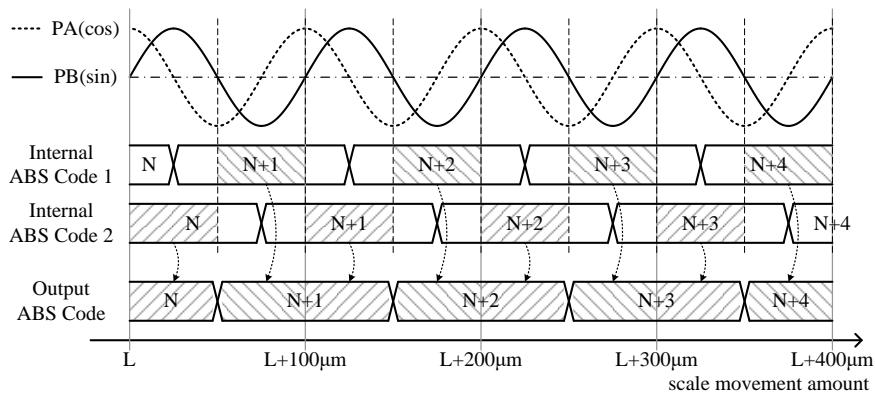
The phases in the following diagram are represented as PA=+cos and PB=+sin, and 0° is defined as the point at which PA is a maximum voltage and the PB voltage is $0.5V_{DD}$.

*1 The center distance between the absolute photodiode (ABS PD) and the incremental photodiode (INC PD) is 2700μm. When the azimuth (D_{YAW}) is 1° , the offset in the vertical direction between ABS PD and INC PD is approximately 47.1 μm ($2700 \times \tan 1^\circ \approx 47.1 \mu\text{m}$). Since one INC PD cycle displacement is 200μm, the phase offset between the ABS signal and INC signal becomes approximately 90° .

ABS code selection when the phase offset is 90°

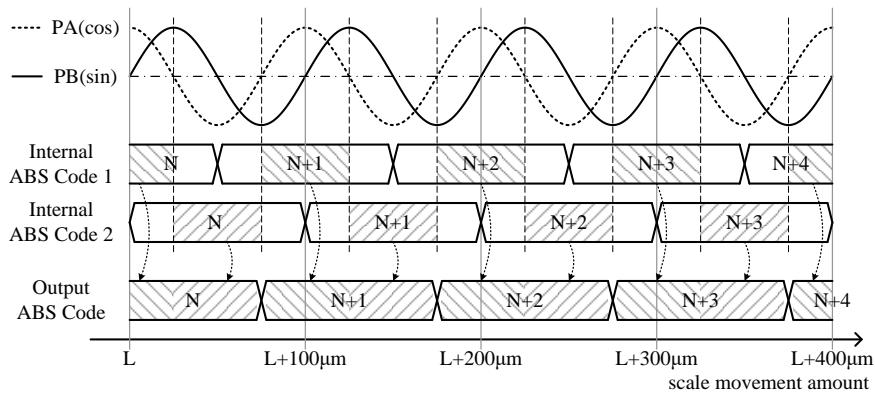
To read ABS codes:

- Select internal ABS code 1 when PA is Low.
- Select internal ABS code 2 when PA is High.

ABS code selection when the phase offset is -180°

To read ABS codes:

- Select internal ABS code 1 when PB is Low.
- Select internal ABS code 2 when PB is High.

ABS code selection when the phase offset is -90°

To read ABS codes:

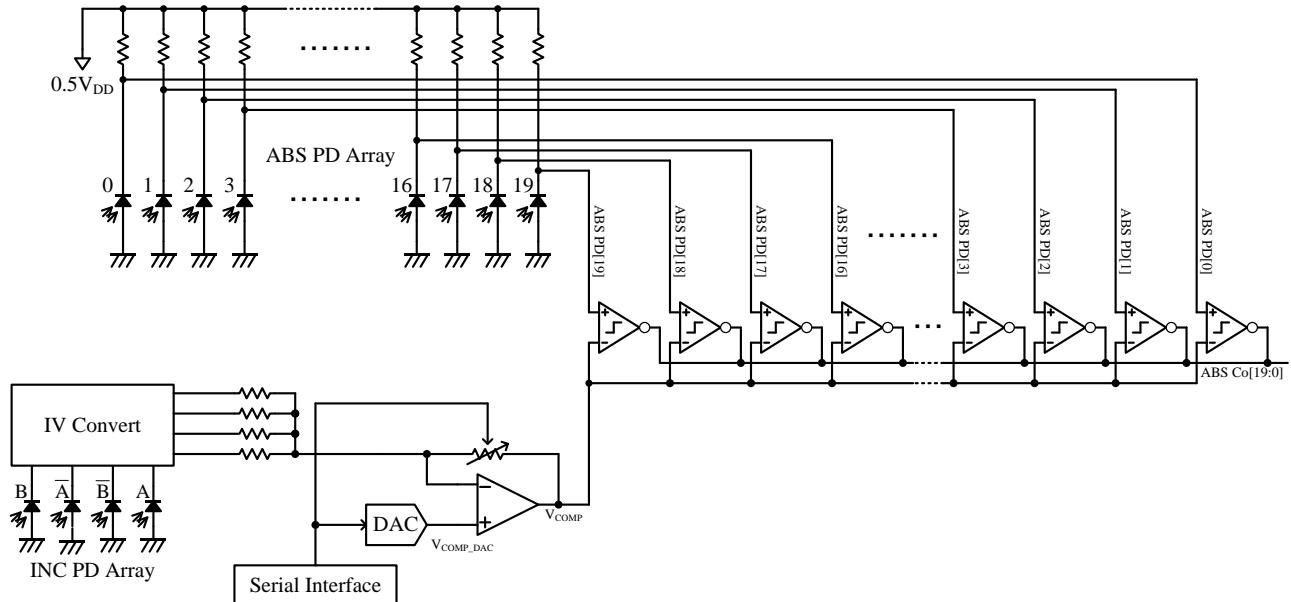
- Select internal ABS code 1 when PA is High.
- Select internal ABS code 2 when PA is Low.

9.5. Absolute Binarization Voltage Adjustment Function

The SM3414 has a built-in function that tracks the amount of light received by the photodiode by converting the analog absolute signal to binary using a threshold voltage in order to read the absolute code in a stable manner.

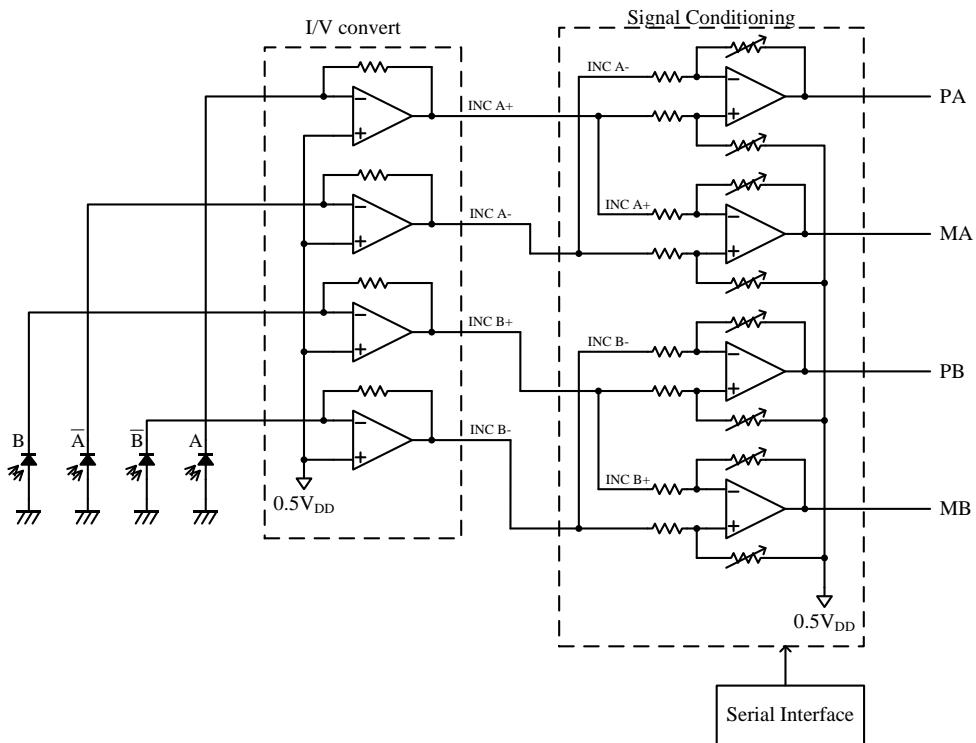
The photodiode for the incremental signal is used to detect the amount of light.

The gain setting (which determines the change in the binarization threshold voltage corresponding to changes in the amount of light) and the DC offset voltage (which serves as the reference for changes in the binarization threshold voltage) are adjusted using the serial interface.



9.6. Incremental Output, I/V Conversion Gain Adjustment Function

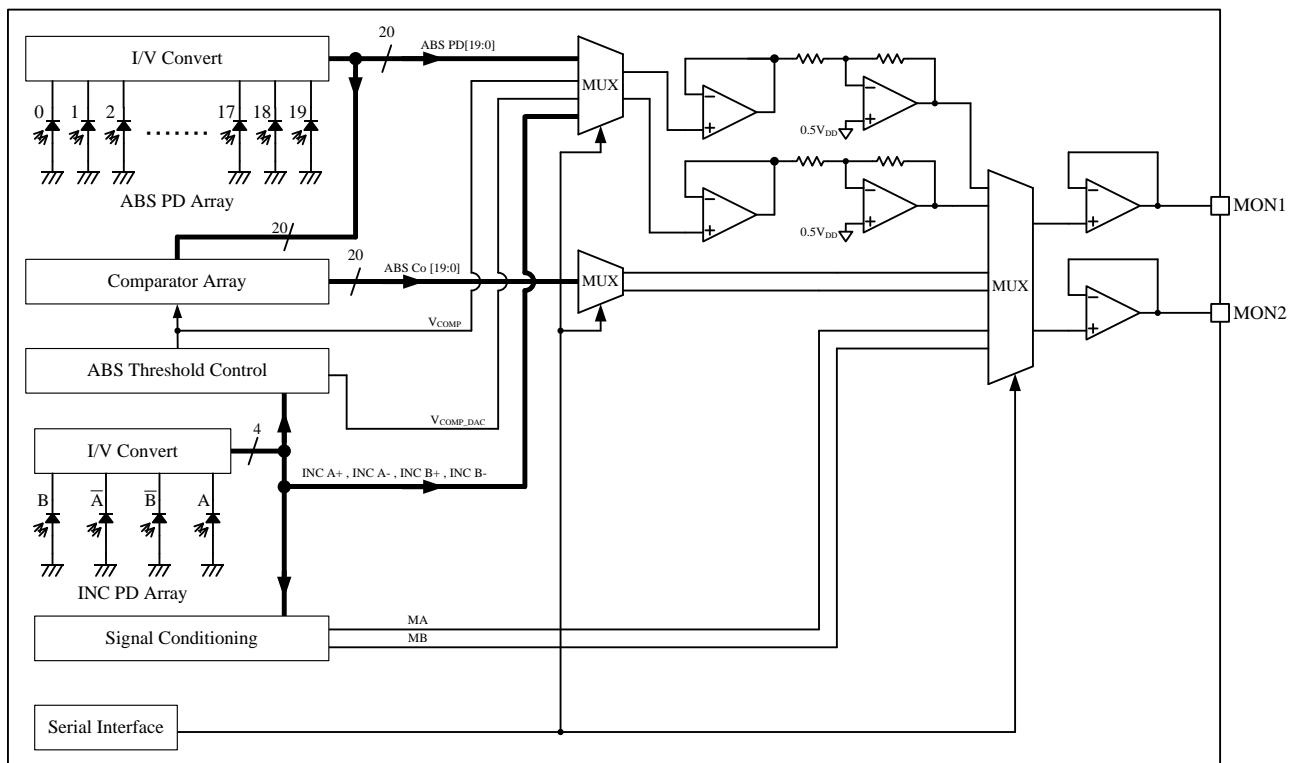
The SM3414 can adjust the I/V conversion gain of the incremental signal. The gain adjustment value is adjusted using the serial interface. The adjustment value can be set individually for phase A and phase B.



9.7. Internal Signal Monitor Function

The SM3414 has a built-in function for monitoring various internal signals in order to check the signals inside the IC. Signals that can be monitored include the analog signal prior to binarization of each bit of the absolute signal, the binarization threshold voltage, and the internal signals after I/V conversion of the incremental signal.

The signals to monitor are set using the serial interface, and are output from the MON1 and MON2 pins. For details about the signals to monitor and the output pins, see “9.12.8. Monitor target signal setting register (MON_SEL[3:0]” and “9.12.9. Monitor target signal setting register 2 (OUT_SEL1[4:0], OUT_SEL2[4:0].”



9.8. Reset Function

You can reset all the SM3414 shift register contents in the serial interface to “0” by setting the RSTN pin to Low level. During normal operation, set the RSTN pin to High level.

9.9. Absolute Circuit Power-Down Function

When the PDN pin is set to Low level, the circuit functionality for the absolute signal stops, and only the circuit for the incremental signal is in the operating state, enabling the current consumption to be reduced.

9.10. Standby Function

When both the PDN pin and RSTN pin are set to Low level, the device switches to standby mode and all circuits stop, including the LED driver. In standby mode, the current consumption is reduced to an extremely low value.

9.11. M Code Conversion Function

The SM3414 uses a built-in decoder to convert M codes to binary data.

[M-code conversion table]

Binary	M Code						
0	0	48	84	96	19	144	476
1	1	49	168	97	38	145	440
2	2	50	337	98	76	146	368
3	4	51	163	99	153	147	225
4	8	52	326	100	307	148	450
5	17	53	141	101	103	149	389
6	34	54	283	102	206	150	267
7	68	55	54	103	413	151	22
8	136	56	108	104	314	152	44
9	273	57	217	105	116	153	89
10	35	58	435	106	232	154	179
11	70	59	359	107	465	155	358
12	140	60	207	108	419	156	205
13	281	61	415	109	327	157	411
14	50	62	318	110	143	158	310
15	100	63	124	111	287	159	109
16	200	64	249	112	62	160	219
17	401	65	499	113	125	161	439
18	291	66	487	114	251	162	367
19	71	67	463	115	503	163	222
20	142	68	414	116	495	164	445
21	285	69	316	117	478	165	378
22	58	70	120	118	444	166	244
23	117	71	241	119	376	167	488
24	234	72	482	120	240	168	464
25	469	73	453	121	480	169	417
26	427	74	395	122	449	170	323
27	342	75	278	123	387	171	135
28	173	76	45	124	263	172	270
29	347	77	91	125	15	173	28
30	182	78	183	126	31	174	57
31	364	79	366	127	63	175	115
32	216	80	220	128	127	176	230
33	433	81	441	129	255	177	460
34	355	82	370	130	511	178	408
35	199	83	229	131	510	179	304
36	398	84	458	132	508	180	97
37	284	85	404	133	504	181	194
38	56	86	297	134	496	182	388
39	113	87	82	135	481	183	265
40	226	88	164	136	451	184	18
41	452	89	328	137	391	185	36
42	393	90	144	138	271	186	72
43	274	91	288	139	30	187	145
44	37	92	65	140	61	188	290
45	74	93	130	141	123	189	69
46	149	94	260	142	247	190	138
47	298	95	9	143	494	191	277

Binary	M Code						
192	43	234	467	276	416	318	60
193	87	235	423	277	321	319	121
194	174	236	335	278	131	320	243
195	349	237	158	279	262	321	486
196	186	238	317	280	13	322	461
197	373	239	122	281	27	323	410
198	235	240	245	282	55	324	308
199	471	241	490	283	110	325	105
200	431	242	468	284	221	326	211
201	350	243	425	285	443	327	422
202	188	244	338	286	374	328	333
203	377	245	165	287	237	329	154
204	242	246	330	288	475	330	309
205	484	247	148	289	438	331	107
206	457	248	296	290	365	332	215
207	402	249	80	291	218	333	430
208	293	250	160	292	437	334	348
209	75	251	320	293	363	335	184
210	151	252	129	294	214	336	369
211	302	253	258	295	428	337	227
212	92	254	5	296	344	338	454
213	185	255	10	297	176	339	397
214	371	256	21	298	352	340	282
215	231	257	42	299	193	341	52
216	462	258	85	300	386	342	104
217	412	259	170	301	261	343	209
218	312	260	341	302	11	344	418
219	112	261	171	303	23	345	325
220	224	262	343	304	46	346	139
221	448	263	175	305	93	347	279
222	385	264	351	306	187	348	47
223	259	265	190	307	375	349	95
224	7	266	381	308	239	350	191
225	14	267	250	309	479	351	383
226	29	268	501	310	446	352	254
227	59	269	491	311	380	353	509
228	119	270	470	312	248	354	506
229	238	271	429	313	497	355	500
230	477	272	346	314	483	356	489
231	442	273	180	315	455	357	466
232	372	274	360	316	399	358	421
233	233	275	208	317	286	359	331

Binary	M Code						
360	150	398	345	436	301	474	195
361	300	399	178	437	90	475	390
362	88	400	356	438	181	476	269
363	177	401	201	439	362	477	26
364	354	402	403	440	212	478	53
365	197	403	295	441	424	479	106
366	394	404	79	442	336	480	213
367	276	405	159	443	161	481	426
368	41	406	319	444	322	482	340
369	83	407	126	445	133	483	169
370	166	408	253	446	266	484	339
371	332	409	507	447	20	485	167
372	152	410	502	448	40	486	334
373	305	411	493	449	81	487	156
374	99	412	474	450	162	488	313
375	198	413	436	451	324	489	114
376	396	414	361	452	137	490	228
377	280	415	210	453	275	491	456
378	48	416	420	454	39	492	400
379	96	417	329	455	78	493	289
380	192	418	146	456	157	494	67
381	384	419	292	457	315	495	134
382	257	420	73	458	118	496	268
383	3	421	147	459	236	497	24
384	6	422	294	460	473	498	49
385	12	423	77	461	434	499	98
386	25	424	155	462	357	500	196
387	51	425	311	463	203	501	392
388	102	426	111	464	407	502	272
389	204	427	223	465	303	503	33
390	409	428	447	466	94	504	66
391	306	429	382	467	189	505	132
392	101	430	252	468	379	506	264
393	202	431	505	469	246	507	16
394	405	432	498	470	492	508	32
395	299	433	485	471	472	509	64
396	86	434	459	472	432	510	128
397	172	435	406	473	353	511	256

9.12. Serial Interface Function

The SM3414 employs a built-in serial interface for reading and writing registers for saving constant settings and parameters of each circuit.

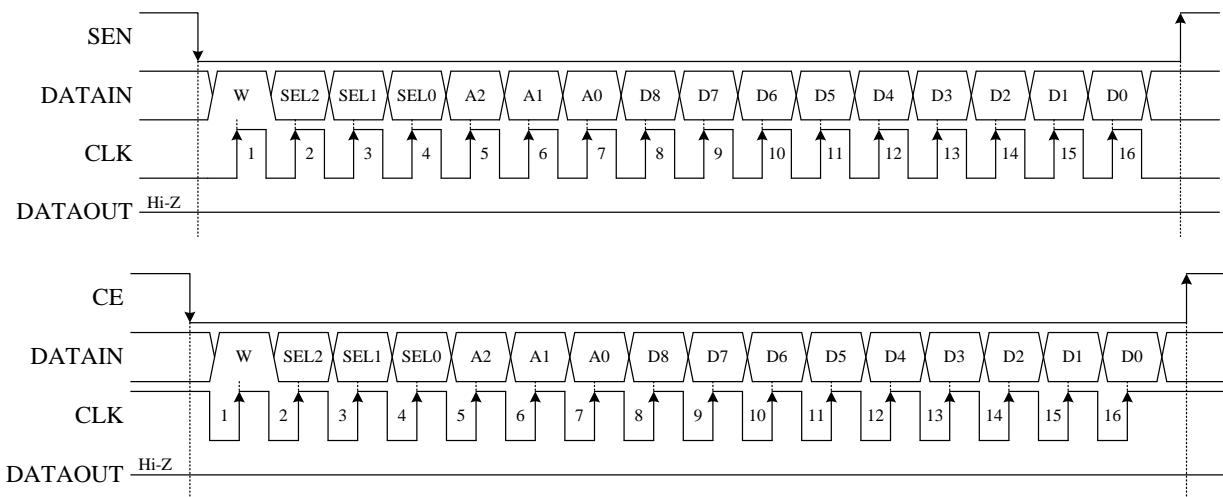
When the SEN pin input is set to Low level, serial interface operation starts. The SM3414 serial interface supports SPI mode 0 and mode 3.

9.12.1. Writing register data

When the SEN pin input is set to Low level, serial interface operation starts.

Send a 1-bit R/W mode setting bit (High level for write mode), a 3-bit absolute PD assignment, and a 3-bit write address assignment to the DATAIN pin, followed by 9-bit write data with the MSB first. On the 16th falling edge on the CLK pin, the write data is loaded into the device and the data becomes active.

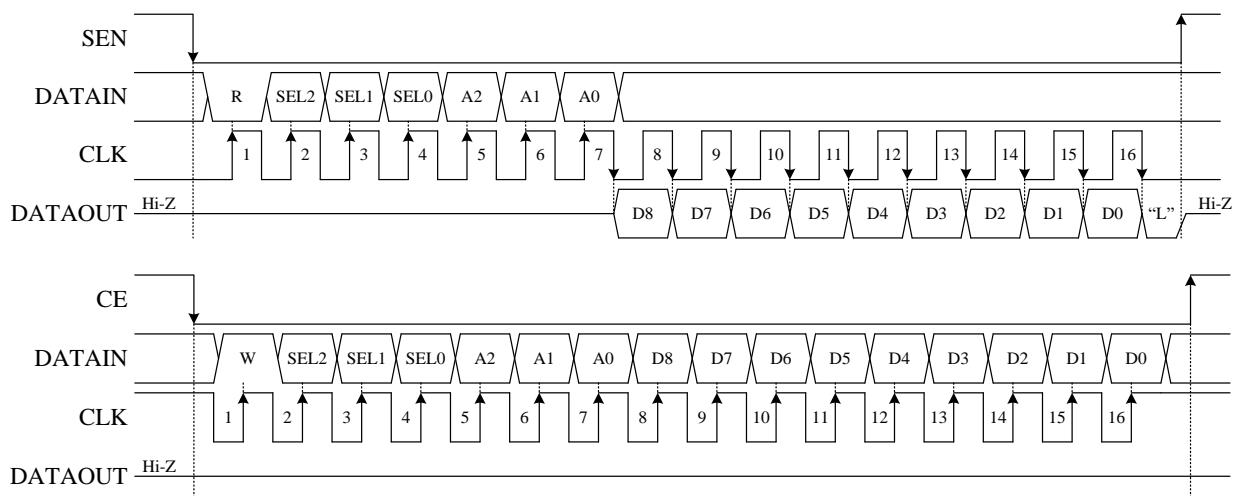
Note that when writing to the registers, do not apply any number of clock cycles other than 16 to the CLK pin. If a different number of cycles is input, it may cause an error in writing.



9.12.2. Reading register data

When the SEN pin input is set to Low level, serial interface operation starts.

Send a 1-bit R/W mode setting bit (Low level for read mode), a 3-bit absolute PD assignment, and a 3-bit read address assignment to the DATAIN pin, and then read the 9-bit data output from the DATAOUT pin with the MSB first starting from the 7th falling edge on the CLK pin. After the 16th falling edge on the CLK pin, the output goes Low level, and serial interface operation ends when a rising edge occurs on the SEN pin.



9.12.3. Internal register map

Definition	R/W	SEL [2:0]	Address [2:0]	D[8:0]								Default value			
				D8	D7	D6	D5	D4	D3	D2	D1	D0			
ABS output data	R	*00	000	ABS_DATA[8:0] (Even-numbered PD select, decode output)								-			
		*01		ABS_DATA[8:0] (Even-numbered PD select, M code output)								-			
		*10		ABS_DATA[8:0] (Odd-numbered PD select, decode output)								-			
		*11		ABS_DATA[8:0] (Odd-numbered PD select, M code output)								-			
ABS adjust 1	R/W	***	001	*2	*1		R	ABS_COMPG[3:0]				100h			
ABS adjust 2	R/W	***	010	ABS_COMPO[8:0]									000h		
INC adjust	R/W	***	011	*1		GA[2:0]		GB[2:0]					000h		
Monitor signal select 1	R/W	***	100	MON_SEL[3:0]				OUTSEL1[4:0]					000h		
Monitor signal select 2	R/W	***	111	*1				OUTSEL2[4:0]					000h		

SEL[2:0] entries with “*” are don’t care values.

*1: Reserved. Set to 0 for normal operation.

*2: Version identification register with default value of 1 (Reserved). Set to 1 for write commands.

9.12.4. Absolute I/V converter resistance adjustment register (R)

The R register (address: 001b) sets the I/V converter resistance for the absolute signal. The I/V converter resistance can be set to 2.95MΩ or 5.90MΩ. Changing the value of the I/V converter resistance enables the amplitude of the absolute signal to be increased without changing the LED current.

R	I/V converter resistance
0	2.95MΩ
1	5.90MΩ

9.12.5. Absolute binarization voltage gain adjustment register (ABS_COMPG[3:0])

The ABS_COMPG[3:0] register (address: 001b) sets the gain relative to the light level when determining the threshold voltage for binarizing the absolute signal.

For an overview of the setting, see “9.5. Absolute Binarization Voltage Adjustment Function.”

ABS_COMPG				Gain (typ.)
[3]	[2]	[1]	[0]	
1	0	0	0	0.096
1	0	0	1	0.138
1	0	1	0	0.180
1	0	1	1	0.222
1	1	0	0	0.264
1	1	0	1	0.306
1	1	1	0	0.347
1	1	1	1	0.389
0	0	0	0	0.431
0	0	0	1	0.473
0	0	1	0	0.515
0	0	1	1	0.557
0	1	0	0	0.599
0	1	0	1	0.640
0	1	1	0	0.682
0	1	1	1	0.721

V_{COMP} can be calculated by the following formula.

$$V_{COMP} = V_{COMP_DAC} - G_{VCOMP} \times (INC\ PD - V_{COMP_DAC})$$

G_{VCOMP} : Gain value (Set the ABS_COMPG[3:0] register)

V_{COMP_DAC} : Offset voltage (Set the ABS_COMPO[8:0] register)

$INC\ PD$: Average value of the incremental signal(INC A+, INC A-, INC B+, INC B-)

9.12.6. Absolute binarization voltage offset adjustment register (ABS_COMPO[8:0])

The ABS_COMPO[8:0] register (address: 010b) sets the threshold voltage offset for binarizing the absolute signal.

For an overview of the setting, see “9.5. Absolute Binarization Voltage Adjustment Function.”

ABS_COMPO										Offset voltage* (V _{DD} =3.0V)
[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
1	0	0	0	0	0	0	0	0	1.1265V	.
1	0	0	0	0	0	0	0	1	1.1279V	.
1	0	0	0	0	0	0	1	0	1.1294V	.
1	0	0	0	0	0	0	1	1	1.1309V	.
1	1	1	1	1	1	1	0	1	1.4971V	.
1	1	1	1	1	1	1	1	0	1.4984V	.
1	1	1	1	1	1	1	1	1	1.5000V	.
0	0	0	0	0	0	0	0	0	1.5015V	.
0	0	0	0	0	0	0	0	1	1.5029V	.
0	0	0	0	0	0	0	1	0	1.5044V	.
0	0	0	0	0	0	0	1	1	1.5059V	.
0	1	1	1	1	1	1	0	0	1.8706V	.
0	1	1	1	1	1	1	0	1	1.8721V	.
0	1	1	1	1	1	1	1	0	1.8735V	.
0	1	1	1	1	1	1	1	1	1.8750V	.

* The offset voltage adjustment value (V_{COMP_DAC}) depends on the V_{DD} voltage.

$$V_{COMP_DAC} = \frac{V_{DD}}{2} + \frac{V_{DD}}{4} \cdot \frac{\text{ABS_COMPO [8:0]} + 1}{2^9}$$

(ABS_COMPO[8:0] is -256 to 255 in 2's complement representation)

9.12.7. Incremental Phase A/Phase B I/V conversion gain setting register (GAB[2:0])

The GAB[2:0] register (address: 011b) sets the I/V conversion gain of the incremental phase A signal and incremental phase B signal. The gain of the phase A signal and phase B signal can be adjusted independently.

For an overview of the setting, see “9.6. Incremental Output, I/V Conversion Gain Adjustment Function.”

GA[2:0] GB[2:0]			I/V conversion gain [dB]	(Magnification notation)
[2]	[1]	[0]		
0	0	0	±0dB	1.00×
0	0	1	+3dB	1.41×
0	1	0	+6dB	2.00×
0	1	1	+9dB	2.82×
1	0	0	+12dB	3.98×
1	0	1	+15dB	5.62×
1	1	0	+18dB	7.94×
1	1	1	+21dB	11.22×

9.12.8. Monitor target signal setting register (MON_SEL[3:0])

The MON_SEL[3:0] register (address: 100b) specifies the internal signals to output on the monitor pins. For details about each internal signal, see “9.7. Internal Signal Monitor Function.”

MON_SEL				MON1 pin	MON2 pin
[3]	[2]	[1]	[0]		
0	0	0	0	Hi-Z	Hi-Z
0	0	0	1	MA	MB
0	0	1	0	ABS PD *1	ABS PD *1
0	0	1	1	ABS PD *1	ABS Co *1
0	1	0	0	ABS Co *1	ABS Co *1
0	1	0	1	V _{COMP}	V _{COMP_DAC}
0	1	1	0	V _{COMP}	ABS PD *1
0	1	1	1	V _{COMP}	ABS Co *1
1	0	0	0	INC A+	INC A-
1	0	0	1	INC B+	INC B-
1	0	1	0	INC A+	INC B+
1	0	1	1	INC A-	INC B-
1	1	0	0	V _{COMP}	INC A+
1	1	0	1	V _{COMP}	INC B+
1	1	1	0	V _{COMP}	INC A-
1	1	1	1	V _{COMP}	INC B-

*1: The output of internal signals can be configured using the OUTSEL1[4:0] and OUTSEL2[4:0] settings.

9.12.9. Monitor target signal setting register 2 (OUT_SEL1[4:0], OUT_SEL2[4:0])

The OUTSEL1[4:0] register (address: 100b) and OUTSEL2[4:0] register (address: 111b) specify the numbers of the internal signals to output on the monitor pins when ABS PD and ABS Co settings are configured (MON_SEL[3:0]=2h, 3h, 5h, 6h). OUTSEL1[4:0] specifies the internal signal to output on the MON1 pin, and OUTSEL2[4:0] specifies the internal signal to output on the MON2 pin.

When the MON_SEL[3:0] register is set to a value that does not select an ABS PD or ABS Co (MON_SEL[3:0]=0h, 1h, 4h, 7h, 8h, 9h, Ah, Bh, Ch, Dh, Eh, Fh), the OUTSEL1[4:0] and OUTSEL2[4:0] settings are ignored.

For details about each internal signal, see “9.7. Internal Signal Monitor Function.”

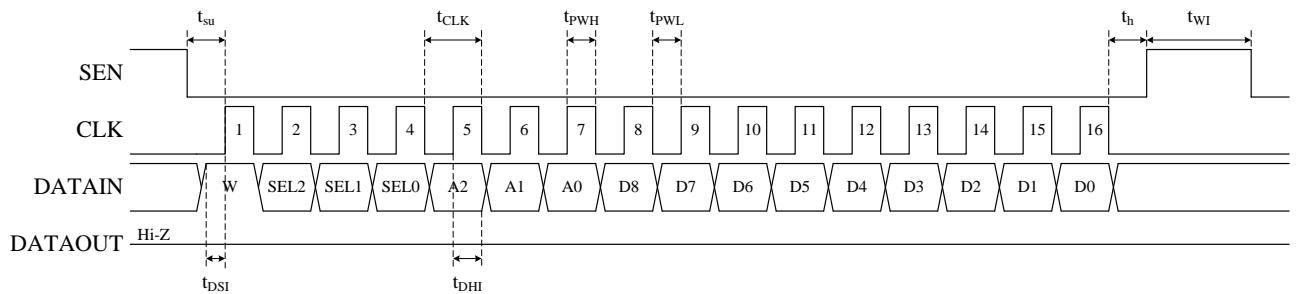
OUTSEL1, OUTSEL2					Selected ABS PD	Selected ABS Co
[4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	ABS PD0	ABS Co0
0	0	0	0	1	ABS PD1	ABS Co1
0	0	0	1	0	ABS PD2	ABS Co2
0	0	0	1	1	ABS PD3	ABS Co3
0	0	1	0	0	ABS PD4	ABS Co4
0	0	1	0	1	ABS PD5	ABS Co5
0	0	1	1	0	ABS PD6	ABS Co6
0	0	1	1	1	ABS PD7	ABS Co7
0	1	0	0	0	ABS PD8	ABS Co8
0	1	0	0	1	ABS PD9	ABS Co9
0	1	0	1	0	ABS PD10	ABS Co10
0	1	0	1	1	ABS PD11	ABS Co11
0	1	1	0	0	ABS PD12	ABS Co12
0	1	1	0	1	ABS PD13	ABS Co13
0	1	1	1	0	ABS PD14	ABS Co14
0	1	1	1	1	ABS PD15	ABS Co15
1	0	0	0	0	ABS PD16	ABS Co16
1	0	0	0	1	ABS PD17	ABS Co17
1	0	0	1	0	ABS PD18	ABS Co18
1	0	0	1	1	ABS PD19	ABS Co19
1	0	1	0	0	Hi-Z	Hi-Z
1	0	1	0	1	Hi-Z	Hi-Z
1	0	1	1	0	Hi-Z	Hi-Z
1	0	1	1	1	Hi-Z	Hi-Z
1	1	0	0	0	Hi-Z	Hi-Z
1	1	0	0	1	Hi-Z	Hi-Z
1	1	0	1	0	Hi-Z	Hi-Z
1	1	0	1	1	Hi-Z	Hi-Z
1	1	1	0	0	Hi-Z	Hi-Z
1	1	1	0	1	Hi-Z	Hi-Z
1	1	1	1	0	Hi-Z	Hi-Z
1	1	1	1	1	Hi-Z	Hi-Z

10. TIMING DIAGRAMS

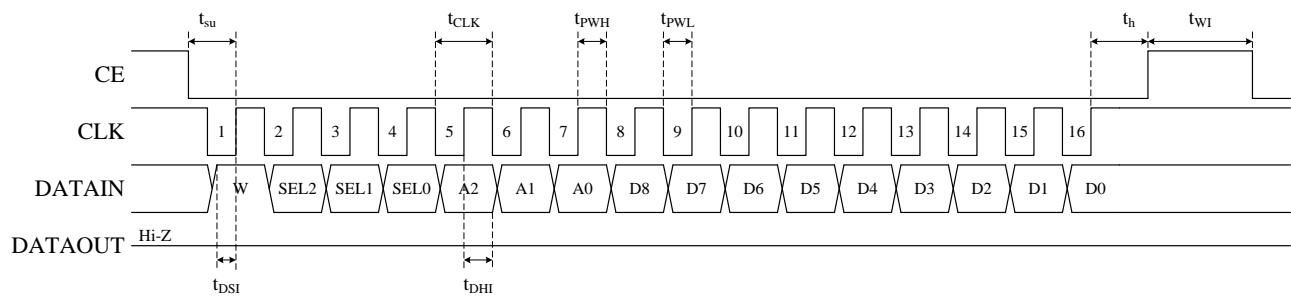
10.1. Serial Interface

[Write timing]

SPI MODE0

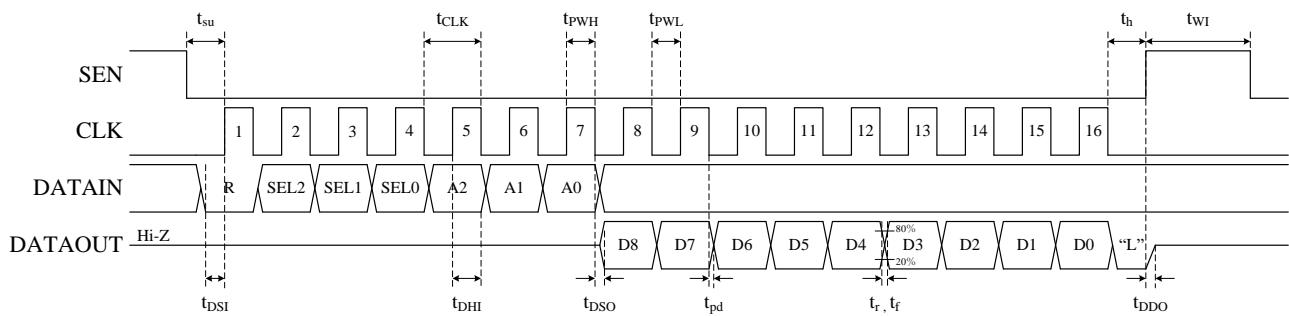


SPI MODE3

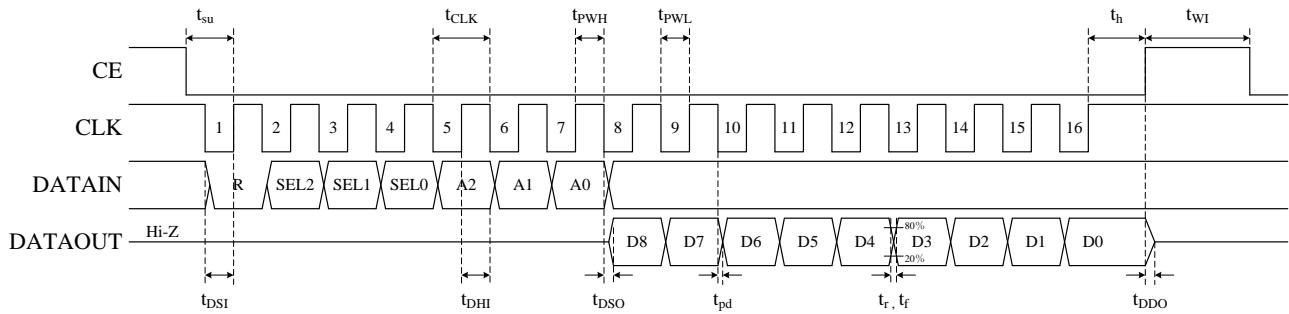


[Read timing]

SPI MODE0



SPI MODE3



V_{DD}=3.0V, V_{SS}=0V, T_a=25°C, C_L=15pF unless otherwise noted

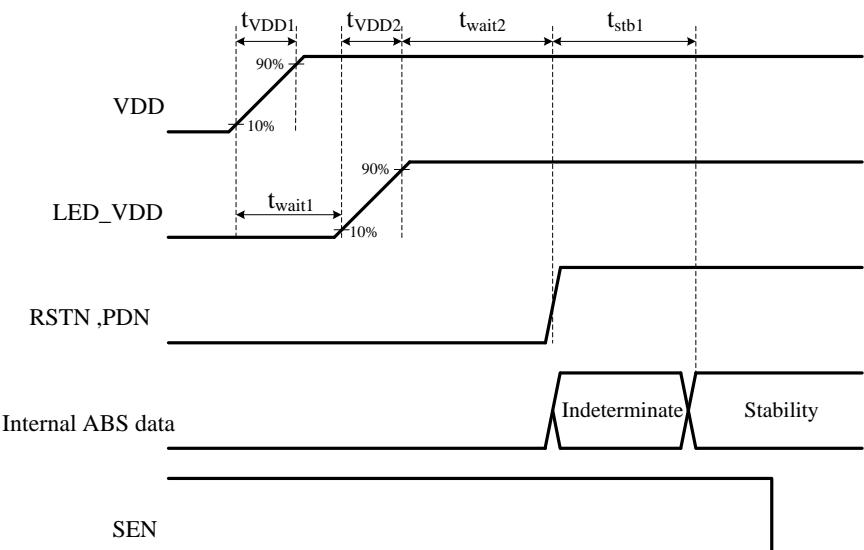
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High-level pulse width	t _{PWH}		90	-	-	ns
Low-level pulse width	t _{PWL}		90	-	-	ns
Pulse cycle time	t _{CLK}		200	-	-	ns
Setup time	t _{SU}		30	-	-	ns
Hold time	t _H		60	-	-	ns
Interface wait time	t _{WI}		300	-	-	ns
Input data setup time	t _{DSI}		20	-	-	ns
Input data hold time	t _{DHI}		90	-	-	ns
Output data setup time	t _{DSO}		-	-	50	ns
Output data disable time	t _{DDO}		-	-	50	ns
Propagation delay time	t _{PD}		-	-	50	ns
Output rise time	t _R		-	-	8	ns
Output fall time	t _F		-	-	8	ns

10.2. Power-Up Procedure

Do not apply the LED_VDD voltage before the VDD voltage ($t_{wait1}>0$).

There are no specified power-on rise time ratings (t_{VDD1} , t_{VDD2}). However, before the power is turned on, set the RSTN and PDN pins to the same potential as VSS (standby state).

The startup stabilization time referred to here is the time required to recover from the absolute circuit power-down state (from standby mode). The ABS output data is stable after 1ms has elapsed since releasing the absolute circuit power-down state (from standby mode).

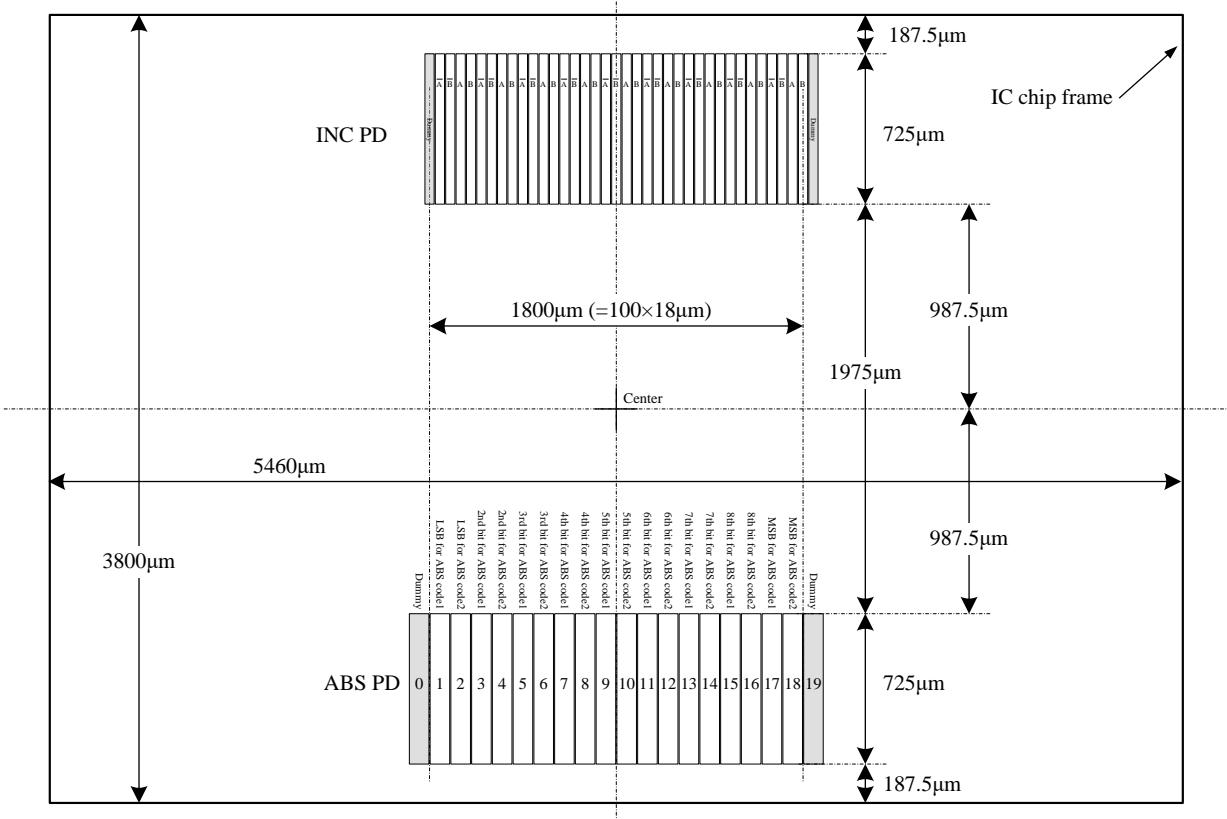


$V_{DD}=V_{LVDD}=3.0V$, $V_{SS}=0V$, $T_a=25^{\circ}C$ unless otherwise noted

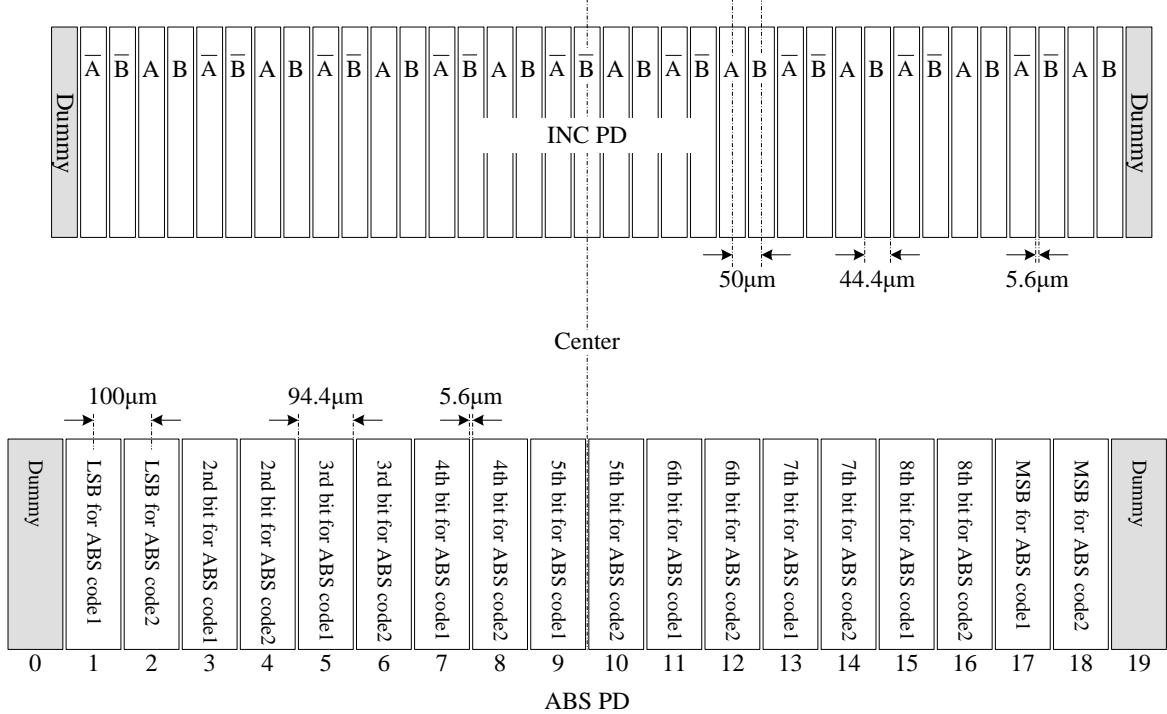
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Standby release wait time	t_{wait2}		1	-	-	ms
Startup stabilization time	t_{stbl}		-	-	1	ms

11. PD LAYOUT and DIMENSIONS

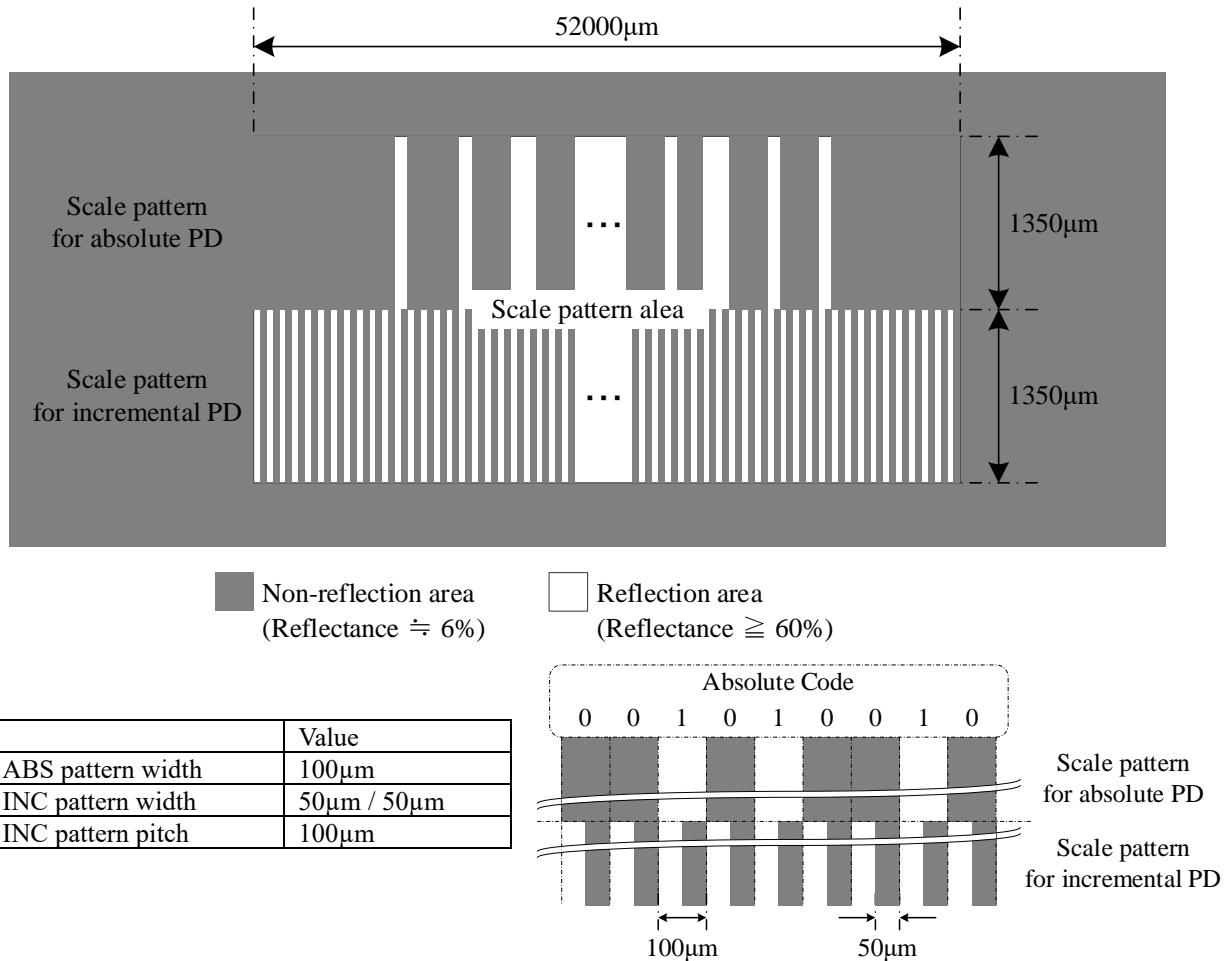
11.1. PD Layout



11.2. PD Width Dimensions



12. RECOMMENDED SCALE PATTERN



12.1. ABS Pattern Table (0: Non-reflective, 1: Reflective)

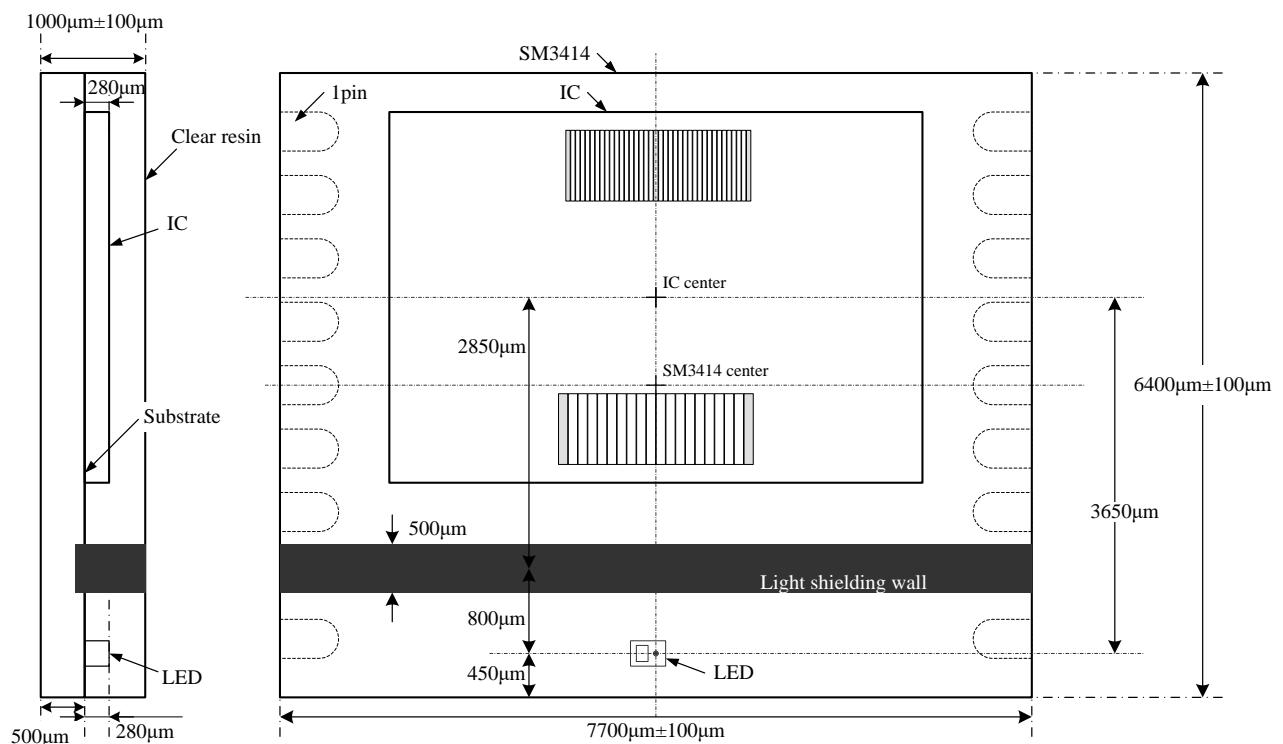
M-code to binary code conversion using the built-in ROM is supported using the following ABS pattern. If you use a pattern other than the recommended ABS pattern, do not read the ABS code (binary).

No	Pattern								
1	0	15	0	29	0	43	1	57	0
2	0	16	0	30	1	44	1	58	0
3	0	17	0	31	0	45	0	59	1
4	0	18	1	32	1	46	0	60	1
5	0	19	1	33	0	47	0	61	0
6	0	20	0	34	1	48	1	62	1
7	0	21	0	35	1	49	0	63	1
8	0	22	1	36	0	50	0	64	0
9	0	23	0	37	1	51	1	65	0
10	1	24	0	38	1	52	0	66	1
11	0	25	0	39	0	53	1	67	1
12	0	26	1	40	0	54	0	68	1
13	0	27	1	41	0	55	1	69	1
14	1	28	1	42	1	56	0	70	1

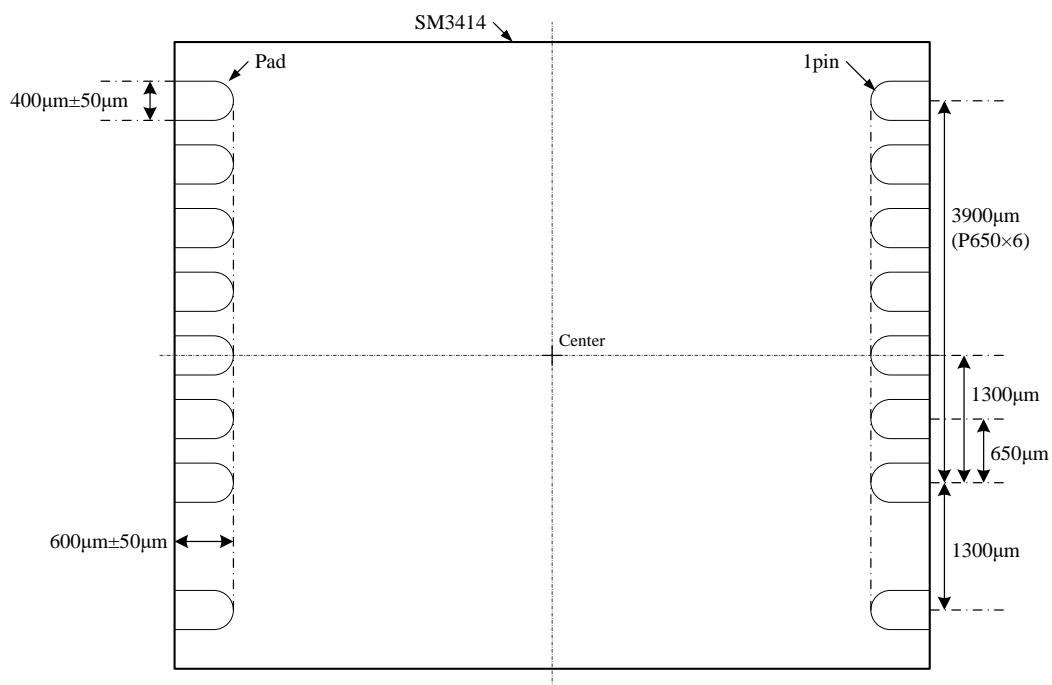
No	Pattern								
71	0	116	1	161	0	206	1	251	0
72	0	117	1	162	1	207	1	252	1
73	1	118	1	163	1	208	1	253	0
74	1	119	1	164	0	209	1	254	1
75	1	120	1	165	1	210	0	255	0
76	1	121	0	166	1	211	0	256	0
77	0	122	1	167	0	212	1	257	0
78	0	123	1	168	1	213	0	258	0
79	0	124	1	169	1	214	0	259	0
80	1	125	1	170	1	215	1	260	0
81	0	126	0	171	1	216	0	261	1
82	1	127	0	172	0	217	1	262	0
83	1	128	0	173	1	218	1	263	1
84	0	129	0	174	0	219	1	264	0
85	1	130	0	175	0	220	0	265	1
86	1	131	1	176	0	221	0	266	0
87	1	132	1	177	0	222	1	267	1
88	0	133	1	178	1	223	1	268	0
89	0	134	1	179	1	224	1	269	1
90	1	135	1	180	1	225	0	270	1
91	0	136	1	181	0	226	0	271	1
92	1	137	1	182	0	227	0	272	1
93	0	138	1	183	1	228	0	273	1
94	0	139	1	184	1	229	0	274	0
95	1	140	0	185	0	230	0	275	1
96	0	141	0	186	0	231	1	276	0
97	0	142	0	187	0	232	1	277	1
98	0	143	0	188	0	233	1	278	1
99	0	144	1	189	1	234	0	279	0
100	0	145	1	190	0	235	1	280	1
101	1	146	1	191	0	236	1	281	0
102	0	147	1	192	1	237	1	282	0
103	0	148	0	193	0	238	0	283	0
104	1	149	1	194	0	239	1	284	0
105	1	150	1	195	0	240	0	285	0
106	0	151	1	196	1	241	0	286	1
107	0	152	0	197	0	242	1	287	1
108	1	153	0	198	1	243	1	288	0
109	1	154	0	199	0	244	1	289	1
110	1	155	0	200	1	245	1	290	1
111	0	156	1	201	1	246	0	291	1
112	1	157	0	202	1	247	1	292	0
113	0	158	1	203	0	248	0	293	1
114	0	159	1	204	1	249	1	294	1
115	0	160	0	205	0	250	0	295	0

No	Pattern								
296	1	341	1	386	0	431	0	476	1
297	1	342	0	387	0	432	1	477	1
298	0	343	0	388	0	433	1	478	0
299	1	344	0	389	0	434	1	479	0
300	0	345	1	390	0	435	1	480	0
301	1	346	1	391	1	436	1	481	0
302	1	347	0	392	1	437	1	482	1
303	0	348	1	393	0	438	0	483	1
304	0	349	0	394	0	439	0	484	0
305	0	350	0	395	1	440	1	485	1
306	0	351	0	396	1	441	0	486	0
307	0	352	1	397	0	442	1	487	1
308	1	353	0	398	0	443	1	488	0
309	0	354	1	399	1	444	0	489	1
310	1	355	1	400	0	445	1	490	0
311	1	356	1	401	1	446	0	491	0
312	1	357	1	402	0	447	1	492	1
313	0	358	1	403	1	448	0	493	1
314	1	359	1	404	1	449	0	494	1
315	1	360	1	405	0	450	0	495	0
316	1	361	0	406	0	451	0	496	0
317	1	362	1	407	1	452	1	497	1
318	1	363	0	408	0	453	0	498	0
319	0	364	0	409	0	454	1	499	0
320	0	365	1	410	1	455	0	500	0
321	0	366	0	411	1	456	0	501	0
322	1	367	1	412	1	457	0	502	1
323	1	368	1	413	1	458	1	503	1
324	1	369	0	414	1	459	0	504	0
325	1	370	0	415	1	460	0	505	0
326	0	371	0	416	0	461	1	506	0
327	0	372	1	417	1	462	1	507	1
328	1	373	0	418	1	463	1	508	0
329	1	374	1	419	0	464	0	509	0
330	0	375	0	420	1	465	1	510	0
331	1	376	0	421	0	466	1	511	0
332	0	377	1	422	0	467	0	512	1
333	0	378	1	423	1	468	0	513	0
334	1	379	0	424	0	469	1	514	0
335	1	380	0	425	0	470	0	515	0
336	0	381	0	426	1	471	1	516	0
337	1	382	1	427	0	472	1	517	0
338	0	383	1	428	0	473	1	518	0
339	1	384	0	429	1	474	1	519	0
340	1	385	0	430	1	475	0	520	0

13. EXTERNAL DIMENSIONS

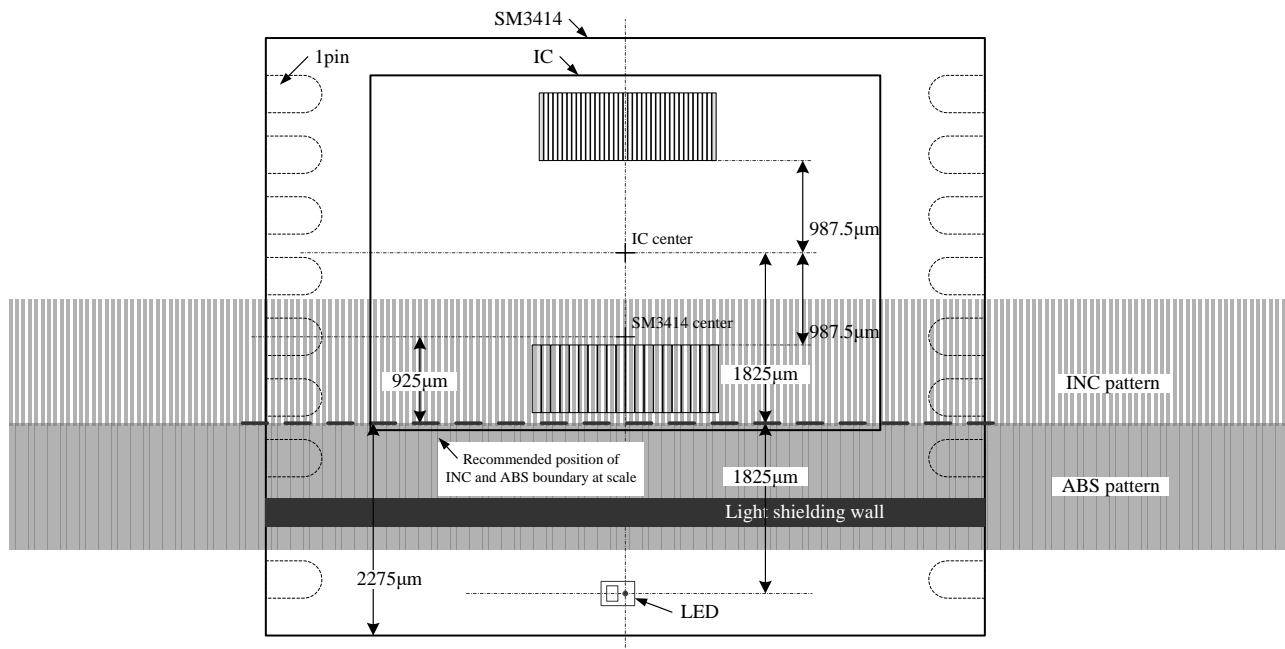


Top view

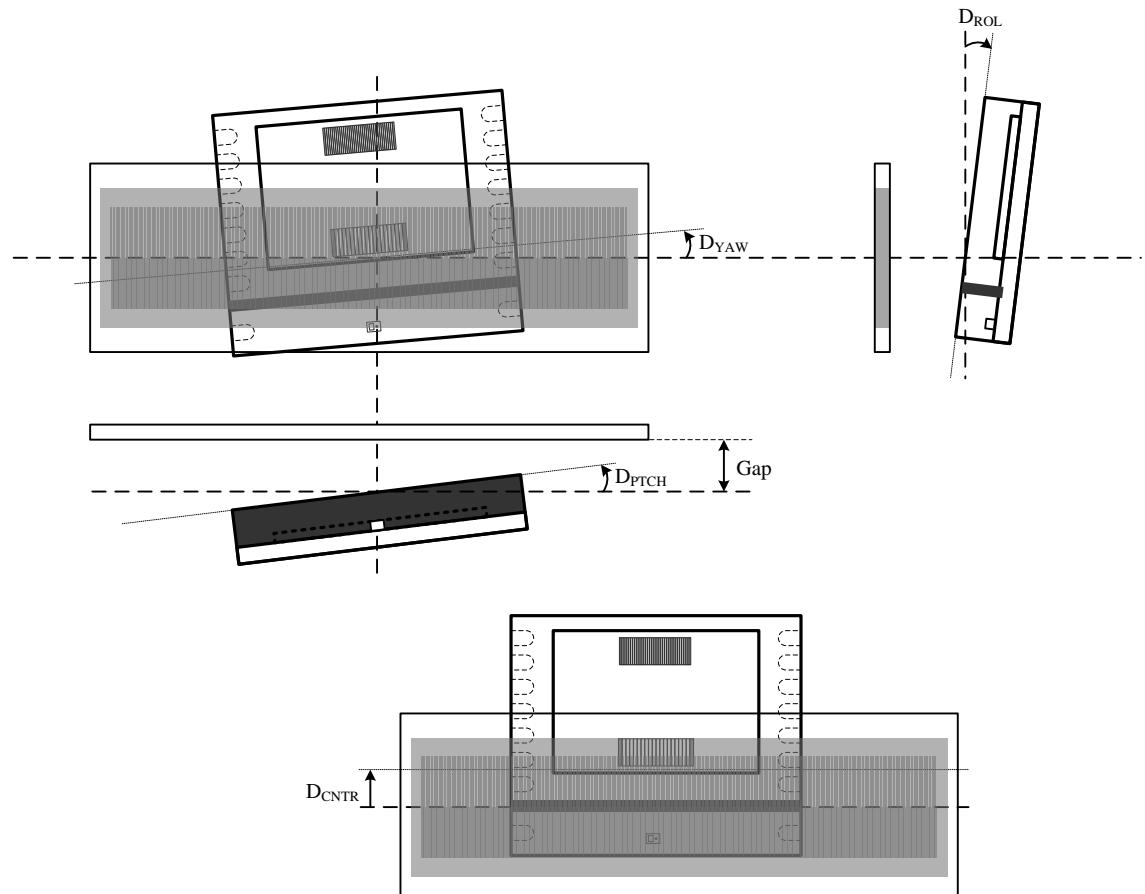


Bottom view

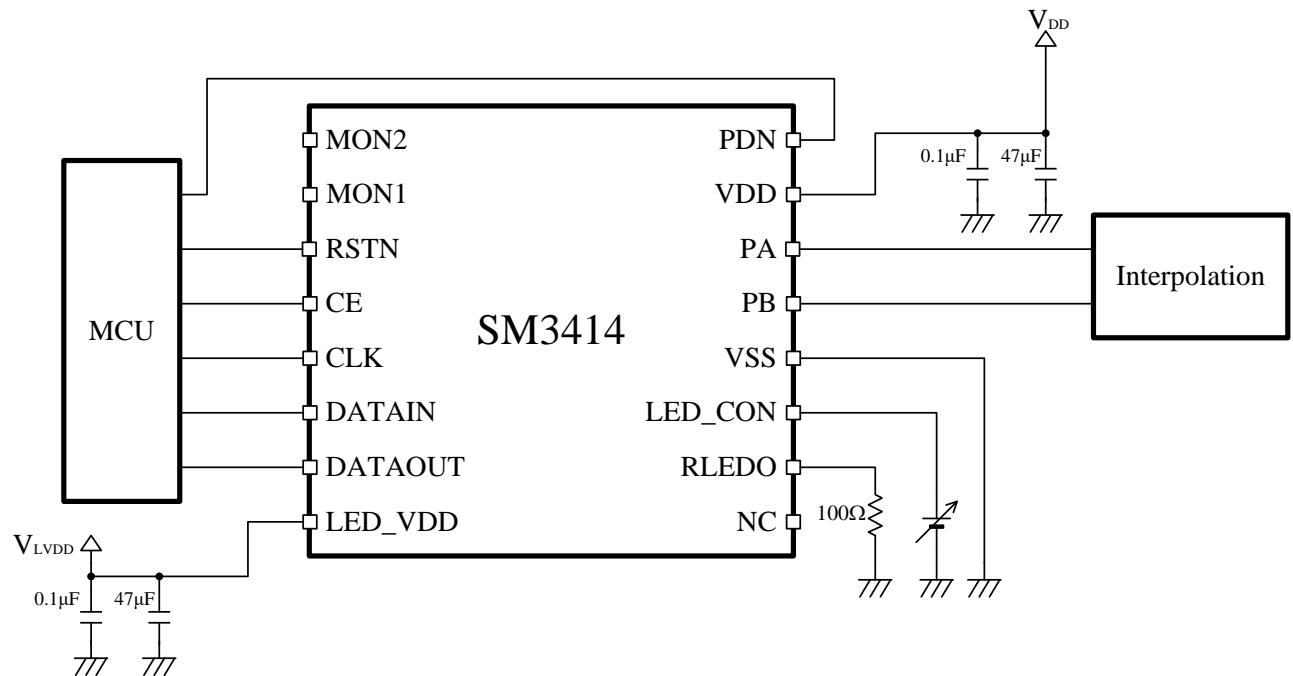
14. RECOMMENDED SCALE MOUNTING POSITION



14.1. Mounting Tolerance Definition



15. TYPICAL APPLICATION CIRCUIT



16. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.

If you wish to use this product in equipment requiring extremely high level of reliability, please contact our sales department or representative in advance.

In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

Please pay your attention to the following points at time of using the products shown in this document.

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If you wish to use the Products in that apparatus, please contact our sales section in advance.
In the event that the Products are used in such apparatus without our prior approval, we assume no responsibility whatsoever for any damages resulting from the use of that apparatus.
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