1. OVERVIEW

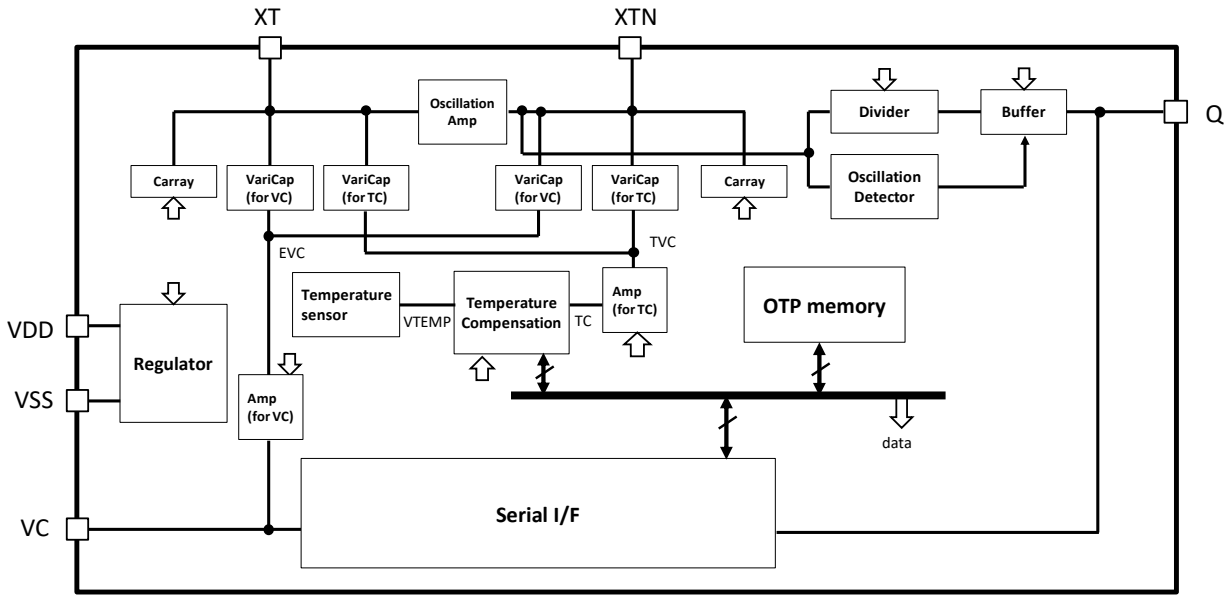
WF7502 is IC for VC-TCXO built-in temperature compensation function. The built-in OTP (One Time Programmable) memory and the temperature compensation circuit compensate the frequency temperature characteristic of AT-cut crystal element.

It is mainly targeted at applications with GPS.

2. FEATURES

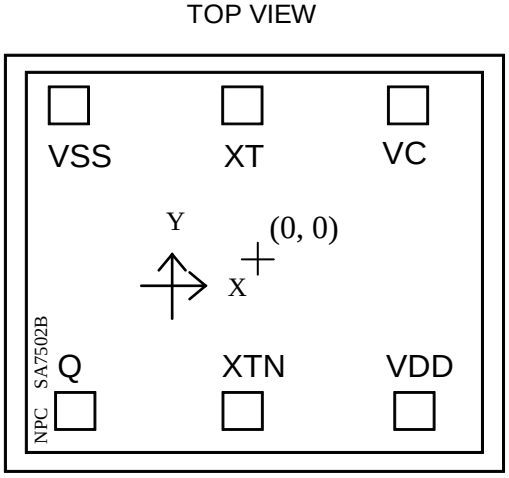
- Oscillation frequency (fosc) : 20MHz to 52MHz
- Output frequency (fout) : 10MHz to 52MHz
- Operating temperature : -40°C to +85°C
- Operating supply voltage : 1.62V to 3.63V
- Temperature compensation accuracy :±0.5ppm (Ta=-40°C to 85°C, Reference frequency at T_a=30°C, Standard crystal reference)
- Phase noise :-141dBc/Hz (TCXO mode, 1kHz Offset, fosc=26MHz, fout=26MHz, V_{DD}=1.8V)
- Current consumption: :1.3mA (TCXO mode, R_{LOAD}//C_{LOAD}=10kΩ//10pF, fosc=26MHz, fout=26MHz, V_{DD}=1.8V, V_{PQ}=0.9Vp-p)
- Embedded memory : Nonvolatile memory (OTP: One Time Programmable) 3bank
- Frequency re-adjustment function
- Clipped-sine Output

3. BLOCK DIAGRAM



4. PAD DIMENSIONS

(1) Chip size*1 : X=0.90mm, Y=0.63mm
(2) Rear surface : VSS potential
(3)Wafer size : 8 inch
(4) Pad aperture size : 70μm × 70μm
(5) Chip dimensions and pad coordinates
*1: The chip size is the value measured between scribe line centers.



Unit: μm

No.	Name	X	Y
1	Q	-284.8	-210.0
2	XTN	0.0	-210.0
3	VDD	+306.0	-210.0
4	VC	+273.8	+210.0
5	XT	0.0	+210.0
6	VSS	-306.0	+210.0

Note: Center of the die is the origin of the coordinate axes, that is, (0.0).

5. PIN DESCRIPTION

No.	Name	I/O	Function
1	Q	I/O	Clock output pin (Clipped sine). In program mode, SDA pin is the serial interface data input/output.
2	XTN	O	Crystal element connection pin2.
3	VDD	-	Supply voltage
4	VC	I	VC voltage input pin. In program mode, SCL pin is the serial interface Clock input and High voltage input.
5	XT	I	Crystal element connection pin1.
6	VSS	-	Ground

I: input pin, O: output pin, I/O: input/output pin

6. ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Supply voltage range	V_{DD}	Voltage between VDD and VSS Normal Operation	-0.3 ~ +4.5	V	*1
Program input voltage range	V_{DDP}	Voltage between VDD and VSS Program Mode	-0.3 ~ +5.5	V	*1,*2
	V_{PP}	Voltage between VC and VSS Program Mode	-0.3 ~ +5.5	V	*1,*2
Input voltage range 1	V_{IN1}	VC pin	-0.3 ~ V_{DD}+0.3	V	*1,*3
Input voltage range 2	V_{IN2}	VC pin Test Mode	-0.3 ~ +2.5	V	*1,*4
Input voltage range 3	V_{IN3}	Q pin Program Mode	-0.3 ~ +5.5	V	*1,*2
Input voltage range 4	V_{IN4}	XT pin	-0.3 ~ +2.5	V	*1
Output voltage range 1	V_{OUT1}	Q pin	-0.3 ~ V_{DD}+0.3	V	*1,*3,*4
Output voltage range 2	V_{OUT2}	XTN pin	-0.3 ~ +2.5	V	*1
Output current	I_Q	Q pin	±5	mA	*5
Junction temperature	T_j	Chip temperature	125	°C	*5
Storage temperature range	T_{STG}	wafer form	-55 ~ +125	°C	*6

*1: Absolute maximum ratings are the values that must never be exceeded, even for a moment. This product may suffer breakdown if any one of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.
*2: Refer to "10.1.1. Recommended Operating Conditions" for programming.
*3: VDD is the VDD value of recommended operating conditions.
*4: Refer to "10.5. Test Mode".
*5: Do not exceed the absolute maximum ratings. If they are exceeded, device characteristics and reliability will be degraded.
*6: When stored alone in nitrogen or vacuum atmosphere.

7. RECOMMENDED OPERATING CONDITIONS

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Supply voltage	V_{DD}	-	1.62	1.8	3.63	V	*1
Input voltage	V_{IN}	XT pin	V_{SS}	-	2.0	V	-
	V_C	VC pin Normal Operation	V_{SS}	-	V_{DD}	V	-
		VC pin Test Mode	V_{SS}	-	2.0	V	*3
Operating temperature	T_a	-	-40	-	+85	°C	-
Oscillator frequency	f_{OSC}	-	20	-	52	MHz	*2
Output frequency	f_{OUT}	Q pin	10	-	52	MHz	-
Output load	C_{LOAD}	Q pin, Load capacitance	-	-	10	pF	-
	R_{LOAD}	Q pin, Load resistance	10	-	-	kΩ	-

*1: For stable operation of this product, mount a ceramic chip capacitor of 0.01μF or larger between VDD and VSS in close proximity to IC (within 3mm). Wiring pattern between IC and capacitor should be as thick as possible.
*2: The oscillation frequency is a yardstick value and the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*3: Refer to "10.5. Test Mode".

8. ELECTRICAL CHARACTERISTICS

8.1. DC Characteristics

V_{DD}=1.62V to 3.63V, V_{SS}=0V, T_a=-40°C to +85°C, R_{LOAD}//C_{LOAD}=10kΩ//10pF unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Current consumption	I_{DD1}	TCXO mode, V_{DD}=1.8V, f_{OSC}=26MHz, f_{OUT}=26MHz, V_{PQ} =0.9Vp-p(VQ[1:0]=01), RVS[1:0]=10, VREG[1:0]=00, HARM=0	-	1.3	1.5	mA
	I_{DD2}	VC-TCXO mode, V_{DD}=1.8V, f_{OSC}=26MHz, f_{OUT}=26MHz, V_{PQ} =0.9Vp-p(VQ[1:0]=01), RVS[1:0]=10, VREG[1:0]=00, HARM=0	-	1.4	1.7	mA
	I_{DD3}	TCXO mode, V_{DD}=1.8V, f_{OSC}=52MHz, f_{OUT}=26MHz, V_{PQ} =0.9Vp-p(VQ[1:0]=01) RVS[1:0]=01, VREG[1:0]=00, HARM=0	-	1.5	1.85	mA
	I_{DD4}	VC-TCXO mode, V_{DD}=1.8V, f_{OSC}=52MHz, f_{OUT}=26MHz V_{PQ} =0.9Vp-p(VQ[1:0]=01) RVS[1:0]=01, VREG[1:0]=00, HARM=0	-	1.6	2.0	mA
Standby current	I_{STB}	Standby mode Register OP=1 V_C=V_{SS}	-	0.5	2.0	μA
HIGH-level input voltage (TCXO mode)	V_{IHS}	Register OP=1 VC pin	0.8V_{DD}	-	-	V
LOW-level input voltage (Standby mode)	V_{ILS}	Register OP=1 VC pin	-	-	0.2V_{DD}	V
Input resistance for VC pin	R_{IN1}	TCXO mode OP=1 V_C=V_{DD} or "OPEN"	50	100	200	kΩ
	R_{IN2}	Standby mode OP=1 V_C=V_{SS}	5	10	-	MΩ
	R_{IN3}	VC-TCXO mode OP=0 Bias=0, GV[3:0]=0001~1111 V_C=V_{SS} to V_{DD}	0.5	1	2	MΩ
		TCXO mode OP=0 Bias=0, GV[3:0]=0000 V_C=V_{SS} or V_{DD} or "OPEN"				
	R_{IN4}	VC-TCXO mode OP=0 Bias=1, GV[3:0]=0001~1111 V_C=V_{SS} to V_{DD}	0.65	1.3	2.6	MΩ
		TCXO mode OP=0 Bias=1, GV[3:0]=0000 V_C=V_{SS} or V_{DD} or "OPEN"				

8.2. AC Characteristics

Condition: The following standard crystal reference

Crystal parameters

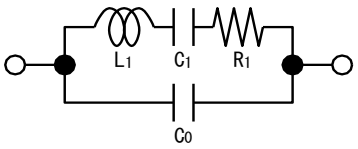


Table1 Standard crystral parameters

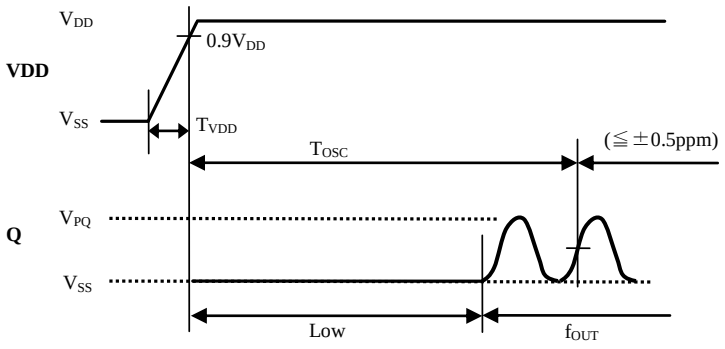
No	Oscillation frequency (f_{OSC})	R_1[Ω]	C_1[fF]	C_0[pF]
1	26MHz	20	2.2	0.7
2	52MHz	30	2.4	1.0

Table2 Standard crystal characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Temperature deviation	dFx	Reference frequency at T_a=30°C	-15	-	+15	ppm
Frequency Offset deviation	dF0	Reference frequency at T_a=30°C	-15	-	+15	ppm

V_{DD}=1.62V to 3.63V, T_a=-40°C to +85°C, R_{LOAD}//C_{LOAD}=10kΩ//10pF unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Temperature Compensation Characteristic	FT	Reference frequency at T_a=30°C	-0.5	-	+0.5	ppm
Frequency-load deviation	FL	C_{LOAD}=10pF±10%, R_{LOAD}=10kΩ or C_{LOAD}=10pF, R_{LOAD}=10kΩ±10%	-0.3	-	+0.3	ppm
Frequency-voltage deviation	FVD	V_{DD}=1.8V±5%	-0.2	-	+0.2	ppm
Output Amplitude	V_{PQ}	Q pin f_{OUT}=26MHz,VQ[1:0]=01 f_{OUT}=52MHz,VQ[1:0]=00	0.8	-	-	V_{P-P}
Harmonic distortion	HD	Q pin The ratio of overtones to fundamental	-	-10	-7	dB
Oscillator start time	T_{OSC}	Start up time by V_{DD} input f_{OSC}±0.5ppm, f_{OSC} resister after setting	-	1	2	ms
Negative Resistance	R_{OSC}	TCXO mode f_{OSC}=52MHz, C0=1pF, CL=5pF (T_a=30°C), RVS [1:0]=00	-	-240	-80	Ω



Oscillator star time

V_{DD}=1.62V to 3.63V, T_a=-40°C to +85°C, R_{LOAD}//C_{LOAD}=10kΩ//10pF unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency variable range (Capacitor Array)	FCA	TC variable capacitance : center VC variable capacitance : center CA capacitance : variable (CA resister) f_{OSC}=26MHz, 52MHz, T_a=30°C Design value	|±15|	-	-	ppm
Variable frequency resolution (CA resister)	dFCA	TC variable capacitance : center VC variable capacitance : center CA capacitance : variable (CA resister) Variable amount per LSB of CA resister. f_{OSC}=26MHz, 52MHz, T_a=30°C Design value	-	3	-	ppm
Frequency variable range (TC varicap)	FV1	TCXO mode TC variable capacitance : variable (TVC=0.9±0.6V) CA capacitance : CL=5pF f_{OSC}=26MHz, 52MHz, T_a=30°C Design value	|±15|	-	-	ppm
Frequency variable range (VC varicap)	FV2	VC-TCXO mode TC variable capacitance : center VC variable capacitance : variable (EVC=0.9±0.6V) CA capacitance : CL=5pF Bias=0, GV[3:0]=1111 f_{OSC}=26MHz, 52MHz, T_a=30°C Design value	|±7|	-	-	ppm

9. FUNCTIONAL DESCRIPTION

9.1. Operation Mode

Please change the operation mode by changing the setting value of register OP and GV.

Resister OP	Resister GV	VC pin	Q pin	Operation mode
0	0000	"OPEN" or V_{DD} or V_{SS}	Frequency output	TCXO mode
	0001~1111	V_C	Frequency output	VC-TCXO mode
1	XXXX	"OPEN" or V_{DD}	Frequency output	TCXO mode
		V_{SS}	Hi-Z	Standby mode

* X=Don't Care

9.2. Oscillation Detection Function

The WF7502 has an oscillation detection circuit.

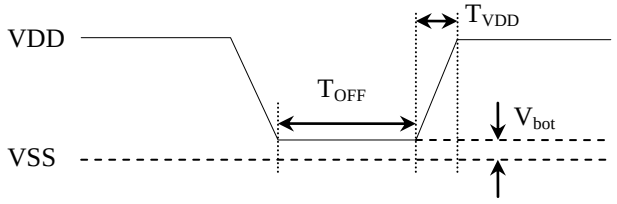
The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation during initial power up and when started again using VC.

When oscillation is detected, the serial interface internal circuits are initialized and the data written to OTP memory is read out. And, it is possible to program to OTP memory and register.

9.3. Power ON Reset Function

This device is equipped with a power-ON reset circuit to initialize internal settings when power is first applied. Ensure supply voltage rise time is the following values for stable, correct, power-ON reset circuit operation.

T_{VDD}	T_{OFF}	V_{bot}
Max.1ms	Min.100ms	0.1V



10. OTP MEMORY AND RESISTER

10.1. Programming Electrical Characteristics

10.1.1. Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Operating supply voltage	V_{DDP}	Voltage between VDD and VSS	4.8	5.0	5.2	V	*1
OTP memory programming supply voltage	V_{PP}	SCL(VC pin)	4.8	5.0	5.2	V	-
Operating temperature	T_{ap}	-	-40	25	+85	°C	-
OTP Memory data retention	-	-40°C～+85°C	10	-	-	year	-

*1: For stable operation of this product, mount a ceramic chip capacitor of (1μF) or larger between VDD and VSS in close proximity to IC (within 3mm). Wiring pattern between IC and capacitor should be as thick as possible.

10.1.2. DC Characteristics (3-wire type serial interface)

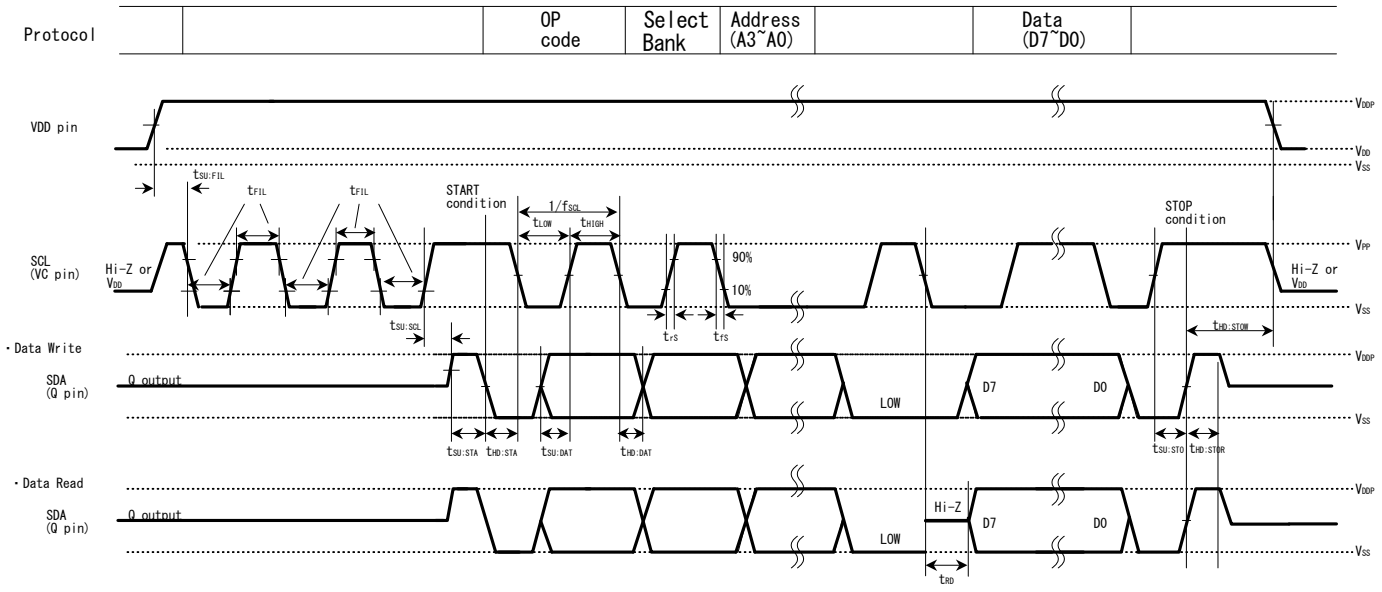
V_{DDP}=4.8V to 5.2V, V_{SS}=0V, T_{ap}=-40°C to +85°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL HIGH-level input voltage	V_{IHC}	SCL(VC pin)	$0.8V_{DDP}$	-	-	V
SCL LOW-level input voltage	V_{ILC}	SCL(VC pin)	-	-	$0.2V_{DDP}$	V
SDA HIGH-level input voltage	V_{IHD}	SDA(Q pin)	$0.8V_{DDP}$	-	-	V
SDA LOW-level input voltage	V_{ILD}	SDA(Q pin)	-	-	$0.2V_{DDP}$	V
SDA HIGH-level output voltage	V_{OHD}	SDA(Q pin), I_{OHD}=-10μA	$0.9V_{DDP}$	-	-	V
SDA LOW-level output voltage	V_{OLD}	SDA(Q pin), I_{OLD}=10μA	-	-	$0.1V_{DDP}$	V

10.1.3. AC Characteristics (3-wire type serial interface)

V_{DDP}=4.8V to 5.2V, V_{SS}=0V, T_{ap}=-40°C to +85°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL clock frequency	f_{SCL}	-	1	-	500	kHz
Start condition setup time	$t_{SU;STA}$	-	0.1	-	-	µs
Start condition hold time	$t_{HD;STA}$	-	0.1	-	-	µs
SCL setup time	$t_{SU;SCL}$	-	0.1	-	-	µs
SCL filter setup time	$t_{SU;FIL}$	-	1	-	-	µs
SCL filter width	t_{FIL}	-	100	-	-	µs
Data setup time	$t_{SU;DAT}$	-	0.1	-	-	µs
Data hold time	$t_{HD;DAT}$	-	0.1	-	-	µs
Stop condition setup time	$t_{SU;STO}$	-	0.1	-	-	µs
Stop condition hold time	$t_{HD;STOW}$	Write OTP mode	25	-	-	ms
	$t_{HD;STOR}$	except Write OTP mode	0.2	-	-	µs
SCL LOW-period	t_{LOW}	-	1	-	500	µs
SCL HIGH-period	t_{HIGH}	-	1	-	-	µs
SCL rise time	t_{rS}	SCL, SDA, 10%→90%	-	-	0.1	µs
SCL fall time	t_{fS}	SCL, SDA, 90%→10%	-	-	0.1	µs
Read data delay time	t_{RD}	-	-	-	0.5	µs

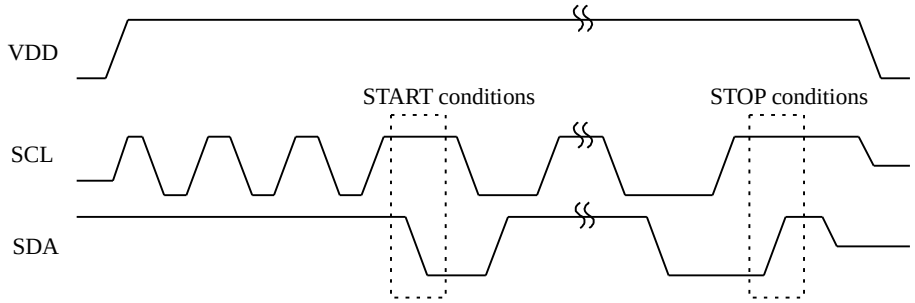


Serial interface timing diagrams

10.1.4. Programming Timing chart

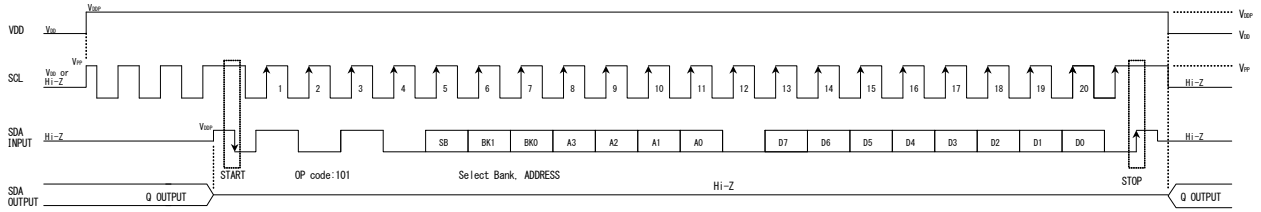
When High Voltage input VDD pin, Data is sent and received using a serial interface comprising SCL (VC clock line) and SDA (Q data line).

Hold SCL and SDA both HIGH level when the serial interface is not transferring data. Device access starts when SDA goes from HIGH to LOW with SCL held HIGH (START condition), and then data can be transferred. Conversely, device access ends when SDA goes from LOW to HIGH with SCL held HIGH (STOP condition). These conditions can be accepted during data transfer, so data transfer should always start with the START condition and end with the STOP condition.

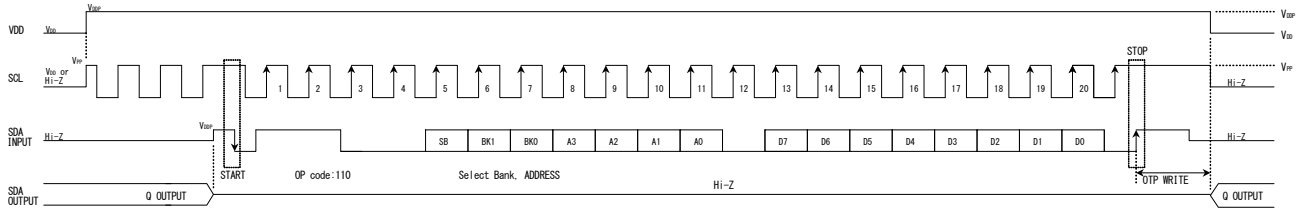


Programming start/stop condition waveform

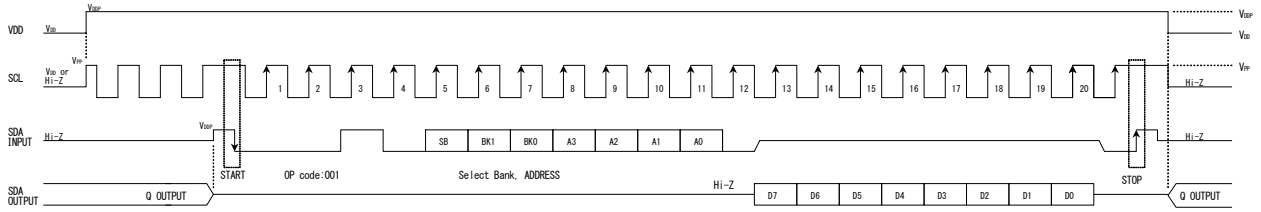
■**Emulation Mode**



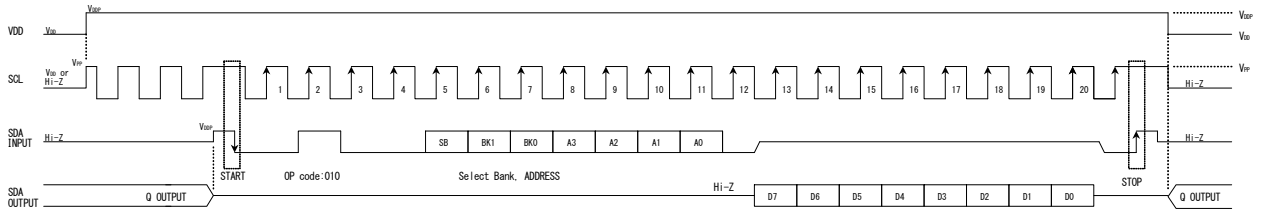
■**Write OTP Memory Mode**



■**Read Resister Mode**

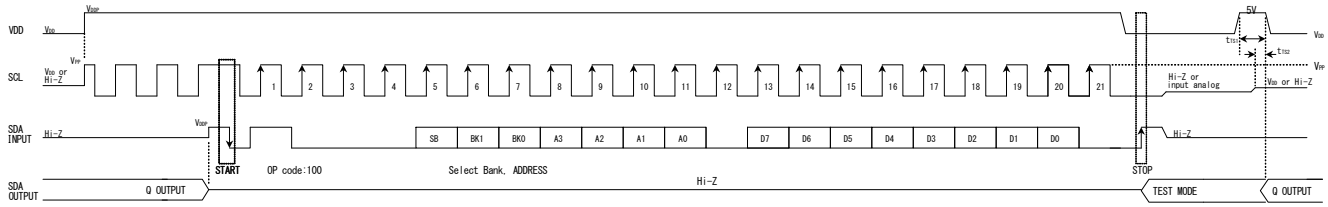


■**Read OTP Memory Mode**



* If using Read OTP Memory Mode at f_{SCL}=1kHz to 20kHz, must write the prescribed data by Emulation Mode before use. For details, see “10.3.1. Operation Mode”.

■**Test Mode**

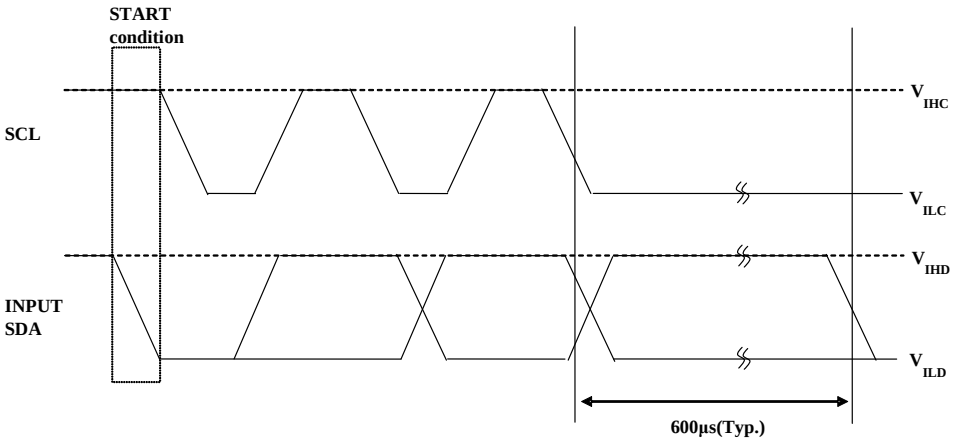


* In this Mode, access ends when SDA goes from LOW to HIGH with SCL held HIGH (STOP condition). After that, IC will be Test Mode state.

* To cancel Test Mode, set V_{DD}=5V once.
Condition: t_{TS1}>(10μs), t_{TS2}>(5μs)

10.2. Reset Timer

When a voltage V_{IHC} is applied to SCL, the output from the Q pin is disabled, and the device is in communication state. If the SCL clock is LOW level for 600μs(Typ.) or longer during communications state (*), the interface is initialized and communication ends.



***:When SCL isn't change from L state to H state for 600μs, the interface will be initialized automatically**

Reset timer operation

10.3. Serial Interface Bit Description

The serial interface data has the following structure.

START condition	OP2	OP1	OP0	0	SB	BK1	BK0	A3	A2	A1	A0	0	D7	D6	D5	D4	D3	D2	D1	D0	STOP condition

10.3.1. Operation Mode(OP code)

OP[2:0]	Operation Mode	Description
101	Emulation Mode (*1)	Write internal resister. Temperature compensation parameters can be changed in a pseudo.
110	Write OTP Memory Mode (*2)	Write OTP memory.
001	Read Resister Mode	Output data of internal resister.
010	Read OTP Memory Mode (*2)	Output data of Read OTP memory.
100	Test Mode	Enter Test Mode.

*1 : Please note that the data will be reset if the power is turned off.

*2 : Must write Resister FOSC according to oscillation frequency before use. For details, see “10.3.3. Resister Description”.

Some bits will be invalid depending on the Operation Mode, so in that case send “0”.
The details are as follows.

(1)Emulation Mode

START condition	1	0	1	0	0	0	0	A3	A2	A1	A0	0	D7	D6	D5	D4	D3	D2	D1	D0	STOP condition

(2)Write OTP Memory Mode

This IC has 3 Banks of registers (see 10.3.2.). Please select the bank by following procedure.

(a)Set SB=0, select the bank to use, and write data to OTP.
* Please use in order from Bank 1

START condition	1	1	0	0	0	BK1	BK0	A3	A2	A1	A0	0	D7	D6	D5	D4	D3	D2	D1	D0	STOP condition

BK1	BK0	Description
0	0	Select Bank 1
0	1	Select Bank 2
1	0	Select Bank 3
1	1	disallowance

(b)Set SB=1, set the bank for read in normal operation
* Please use in order from Bank 1
* Please note that writing “1” cannot return to “0”. For example, bank 1 cannot be set after bank 2 is set.

START condition	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D0	STOP condition

D1	D0	Bank for read in Normal Operation
0	0	Bank 1
0	1	Bank 2
1	X	Bank 3

* X=Don’t Care

(3)Read Resister Mode

START condition	0	0	1	0	0	0	0	A3	A2	A1	A0	0	D7	D6	D5	D4	D3	D2	D1	D0	STOP condition

(4)Read OTP Memory Mode

Note:

If using Read OTP Memory Mode at f_{SCL}=1kHz to 20kHz, must write the following data by Emulation Mode before use.

START condition	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	STOP condition

* In the case of f_{SCL} =20kHz to 500kHz, the above is unnecessary.

(a)To output temperature compensation data : Set SB=0

START condition	0	1	0	0	0	BK1	BK0	A3	A2	A1	A0	0	D7	D6	D5	D4	D3	D2	D1	D0	STOP condition

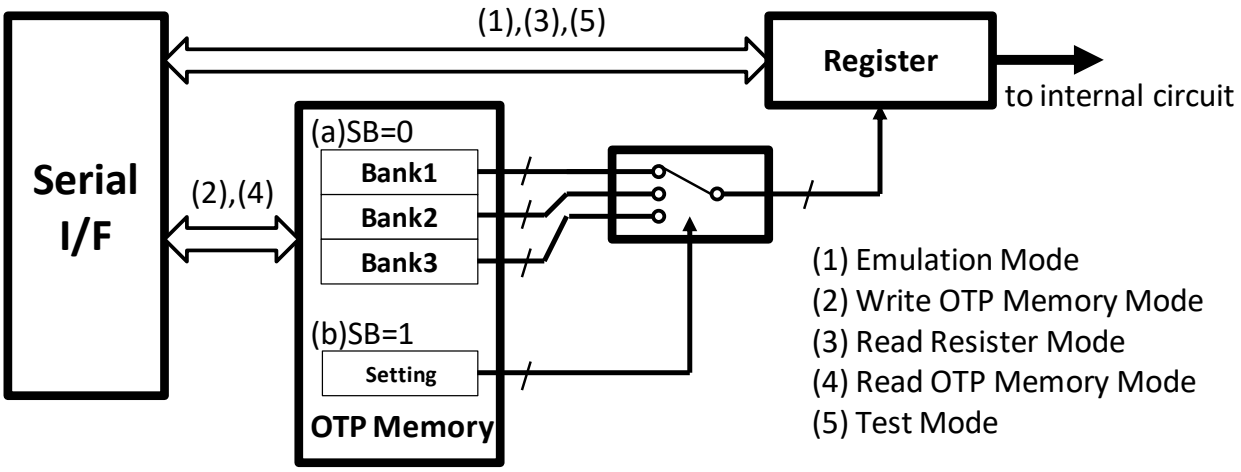
(b)To output the Bank for read in normal operation : Set SB=1

START condition	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D0	STOP condition

(5)Test Mode

START condition	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D3	D2	D1	D0	STOP condition

[Signal flow diagram]



10.3.2. Resister Map

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	CA[3:0]				-	DIV	Bias	OP
0	0	0	1	FOSC[3:0]				GV[3:0]			
0	0	1	0	GT2[1:0]		GT1[5:0]					
0	0	1	1	TR2[1:0]		TR1[5:0]					
0	1	0	0	VQ[1:0]		T0[5:0]					
0	1	0	1	VREG[1:0]		TH1[5:0]					
0	1	1	0	RVS[1:0]		TH2[5:0]					
0	1	1	1	LSFT[1:0]		TL1[5:0]					
1	0	0	0	HARM	-(*1)	TL2[5:0]					
1	0	0	1	-(*1)		F0[5:0]					
1	0	1	0	disallowance							
・ ・ ・											
1	1	1	1								

*1: These registers are for NPC evaluation. Please use the default value "0".

10.3.3. Resister Description

* The following values are design values at VDD=1.8V, Ta=30°C, Frequency-Compensation voltage sensitivity -55ppm/V and are not guaranteed.
* Initial value is all "0".

■The following Resister must be written according to oscillation frequency(f_{OSC}).

f_{OSC} [MHz]	FOSC[3]	FOSC[2]	FOSC[1]	FOSC[0]
20 ~ 22.4	1	X	X	X
22.4 ~ 25.8	0	1	1	1
25.8 ~ 29	0	1	1	0
29 ~ 32	0	1	0	1
32 ~ 35	0	1	0	0
35 ~ 39	0	0	1	1
39 ~ 42	0	0	1	0
42 ~ 46.5	0	0	0	1
46.5 ~ 52	0	0	0	0

* X=Don't Care

■The following Resisters can be written arbitrary.

DIV : Output frequency

DIV	Output Frequency (f_{OUT})
0	f_{OSC}
1	$f_{OSC}/2$

OP : Operation Mode

OP	Operation Mode
0	VC-TCXO
1	TCXO

VREG : Regulator voltage (normal 0)

VREG[1]	VREG[0]	⊿VREG[mV]
1	1	-14
0	0	0
0	1	+14
1	0	+28

VQ : Output Amplitude

VQ[1]	VQ[0]	$⊿V_{PQ}$[V]
0	1	-0.1
0	0	0
1	1	+0.1
1	0	+0.15

CA : Capacitor Array

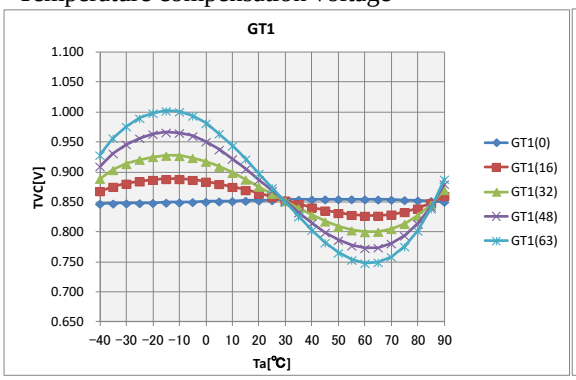
CA[3]	CA[2]	CA[1]	CA[0]	Cap Array
0	1	1	1	none
0	1	1	0	CL0
・・・				・・・
0	0	0	1	6*CL0
0	0	0	0	7*CL0
1	1	1	1	8*CL0
・・・				・・・
1	0	0	1	14*CL0
1	0	0	0	15*CL0

*Design value of CL0 is about (0.1pF)

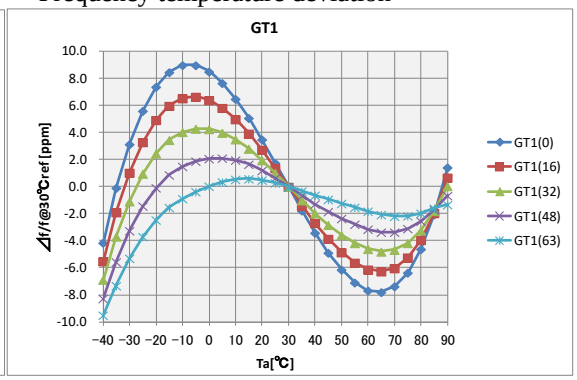
GT1 : Frequency Gain1 for TC
(TCXO mode, CA(14), GT2(1), T0(6), F0(46), other TC parameter(0))

GT1[5]	GT1[4]	GT1[3]	GT1[2]	GT1[1]	GT1[0]	GT1[μV/°C^3]
0	0	0	0	0	0	0
			• • •			-
1	0	0	0	0	0	0.54
			• • •			-
1	1	1	1	1	1	1.08

<Temperature compensation voltage>



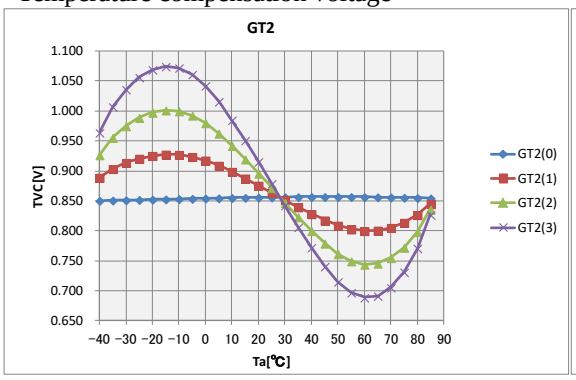
<Frequency temperature deviation>



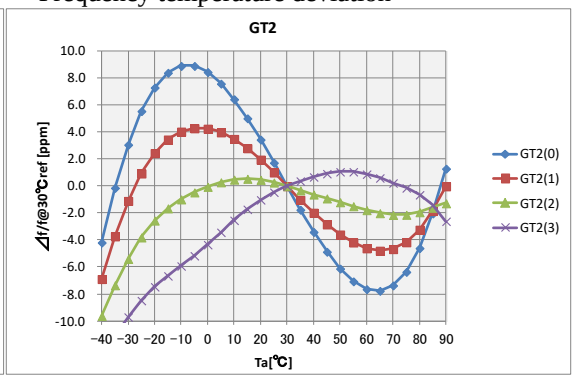
GT2 : Frequency Gain2 for TC
(TCXO mode, CA(14), GT1(32), T0(6), F0(46), other TC parameter(0))

GT2[1]	GT2[0]	GT2[μV/°C^3]
0	0	0
0	1	0.54
1	0	1.09
1	1	1.63

<Temperature compensation voltage>



<Frequency temperature deviation>



Bias : VC Reference Voltage

Bias	VC Reference[V]
0	0.9
1	1.2

In case of VDD is 2.2V or more, please set the VC reference voltage is 1.2V (register Bias=1).

GV : Frequency Gain for VC (VC-TCXO mode, EVC=0.9V, CA(0))

GV[3]	GV[2]	GV[1]	GV[0]	VC Gain[mV/V]
0	0	0	0	OFF
0	0	0	1	-43
・ ・ ・				-
0	1	1	1	-167
1	0	0	0	-188
1	0	0	1	-209
・ ・ ・				-
1	1	1	0	-313
1	1	1	1	-333

In case of the register OP=0 and GV[3: 0]=0000, VC gain adjustment circuit stops and operates in TCXO mode. This operation mode has no standby function. Refer to “9.1. Operation mode” for details.

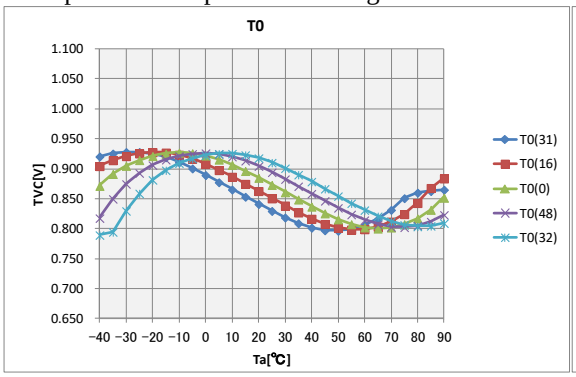
In addition, the equivalent load capacitance (CL) of the oscillator in TCXO mode is smaller than VC-TCXO mode, and the capacitance array(CA) has a difference of about 6 codes.

In case of the output voltage of VC gain adjustment circuit is 0.4V (Typ.) or less, the output voltage will be saturated and will not operate linearly. The output voltage (EVC) of the VC gain adjustment circuit can be monitored in test mode 14. Refer to “10.5. List of test modes” for details.

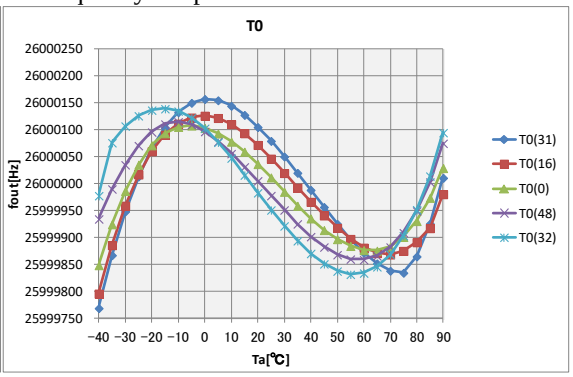
T0 : adjust Offset for Temperature Compensation
(TCXO mode, CA(14), GT2(1), GT1(32), F0(46), other TC parameter (0))

T0[5]	T0[4]	T0[3]	T0[2]	T0[1]	T0[0]	T0[°C](TVC)
0	1	1	1	1	1	9.5
0	1	1	1	1	0	10
・ ・ ・						-
0	0	0	0	0	1	26.5
0	0	0	0	0	0	27
1	1	1	1	1	1	28.5
・ ・ ・						-
1	0	0	0	0	1	47.5
1	0	0	0	0	0	48

<Temperature compensation voltage>



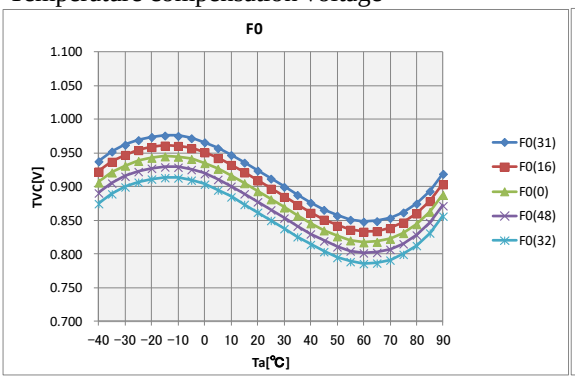
<Frequency temperature deviation>



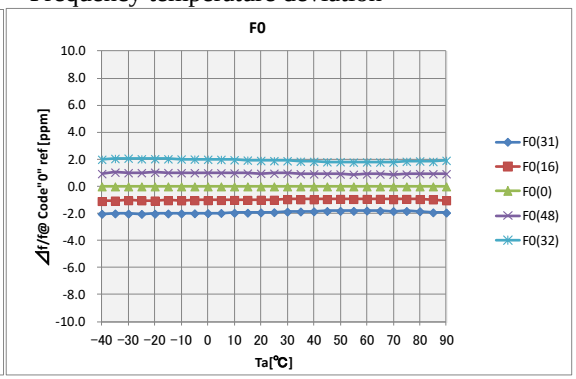
F0 : adjust Frequency Offset
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), other TC parameter(0))

F0[5]	F0[4]	F0[3]	F0[2]	F0[1]	F0[0]	F0[mV]
0	1	1	1	1	1	31
0	1	1	1	1	0	30
• • •						-
0	0	0	0	0	1	+1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
• • •						-
1	0	0	0	0	1	-31
1	0	0	0	0	0	-32

<Temperature compensation voltage>



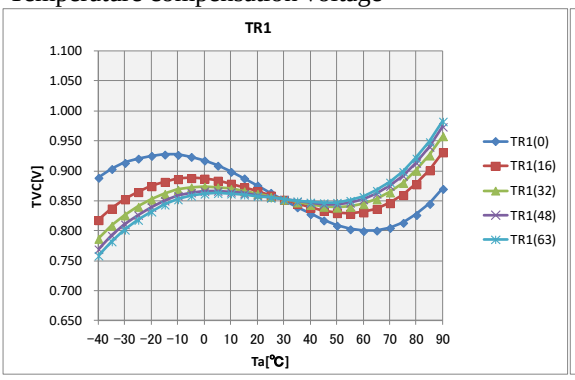
<Frequency temperature deviation>



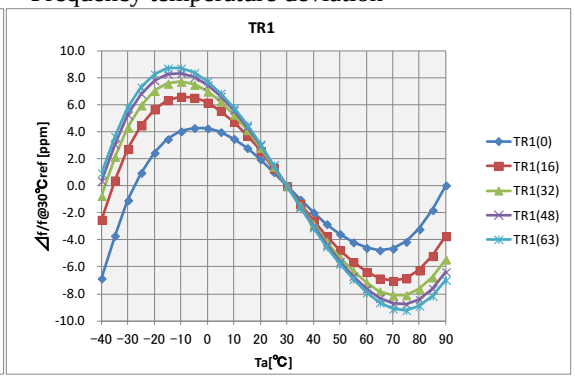
TR1 : adjust Temperature Rotation Compensation1
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

TR1[5]	TR1 [4]	TR1[3]	TR1[2]	TR1[1]	TR1[0]	TR1[mV/°C]
0	0	0	0	0	0	-2.47
• • •						-
1	0	0	0	0	0	-0.99
• • •						-
1	1	1	1	1	1	-0.58

<Temperature compensation voltage>



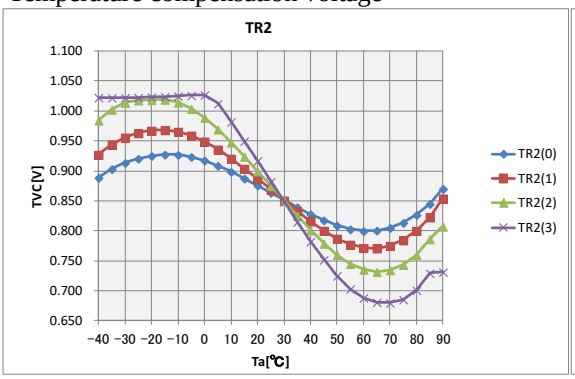
<Frequency temperature deviation>



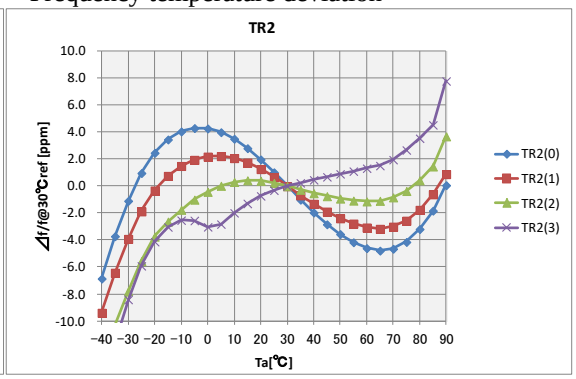
TR2 : adjust Temperature Rotation Compensation2
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

TR2[1]	TR2[0]	TR2[mV/°C]
0	0	-2.47
0	1	-3.63
1	0	-5.04
1	1	-6.10

<Temperature compensation voltage>



<Frequency temperature deviation>

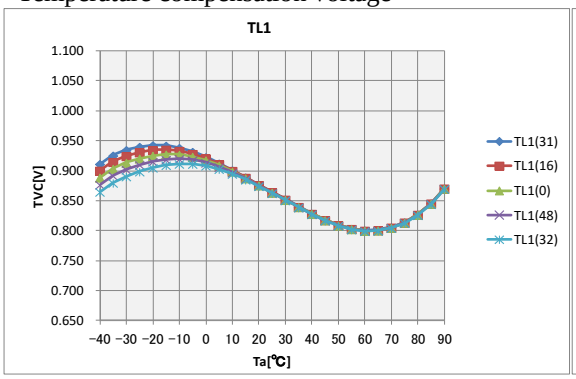


※When using TR2 [1: 0] = 11, set GT2 register to GT2 [1: 0] = 11 (frequency gain 2 max setting).

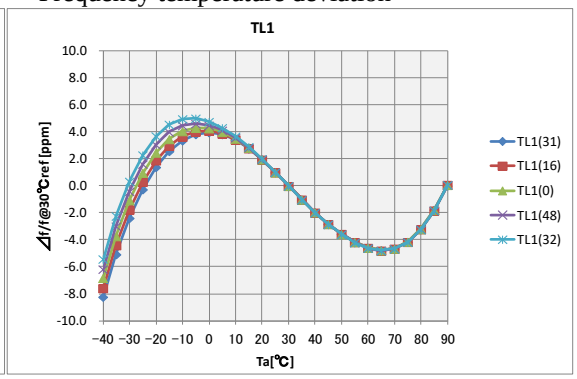
TL1 : adjust Inside for Low Temperature Compensation
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

TL1[5]	TL1[4]	TL1[3]	TL1[2]	TL1[1]	TL1[0]	TL1[mV] T0-60°C
0	1	1	1	1	1	21.7
0	1	1	1	1	0	21
・ ・ ・						-
0	0	0	0	0	1	0.7
0	0	0	0	0	0	0
1	1	1	1	1	1	-0.7
・ ・ ・						-
1	0	0	0	0	1	-22.4
1	0	0	0	0	0	-23.1

<Temperature compensation voltage>



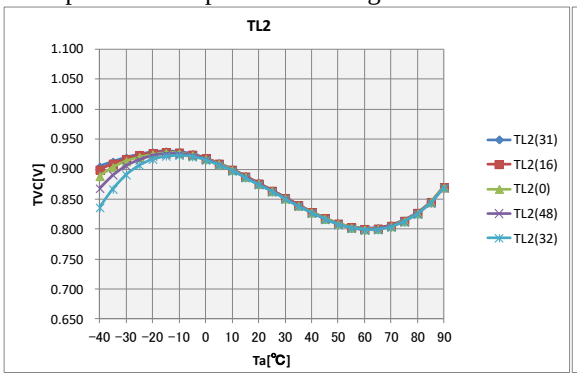
<Frequency temperature deviation>



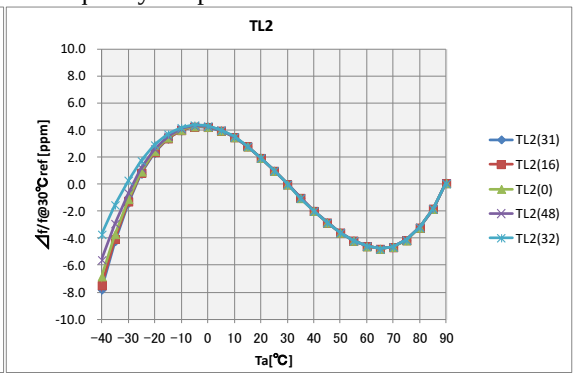
TL2 : adjust Outside for Low Temperature Compensation
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

TL2[5]	TL2[4]	TL2[3]	TL2[2]	TL2[1]	TL2[0]	TL2[mV] T0-60°C
0	1	1	1	1	1	5.8
0	1	1	1	1	0	5.7
• • •						-
0	0	0	0	0	1	0.4
0	0	0	0	0	0	0
1	1	1	1	1	1	-0.2
• • •						-
1	0	0	0	0	1	-21.4
1	0	0	0	0	0	-22.6

<Temperature compensation voltage>



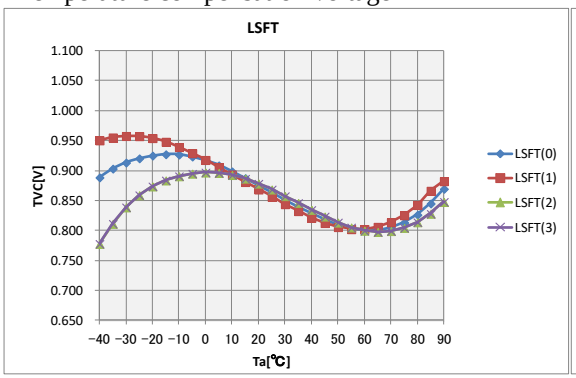
<Frequency temperature deviation>



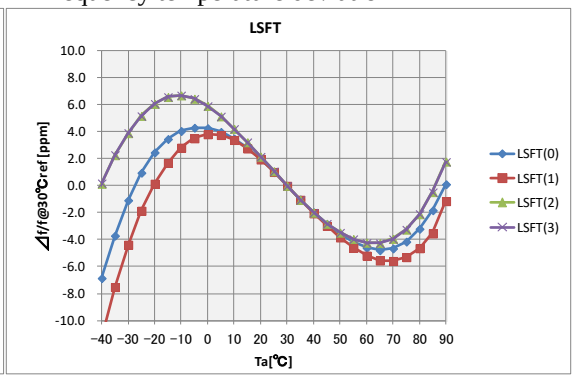
LSFT : adjust Low Temperature Compensation
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

LSFT[1]	LSFT[0]	LSFT[mV] T0-60°C
0	0	0
0	1	+44
1	0	-74
1	1	-74

<Temperature compensation voltage>



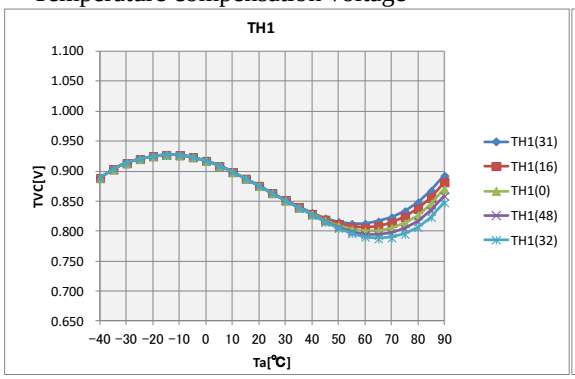
<Frequency temperature deviation>



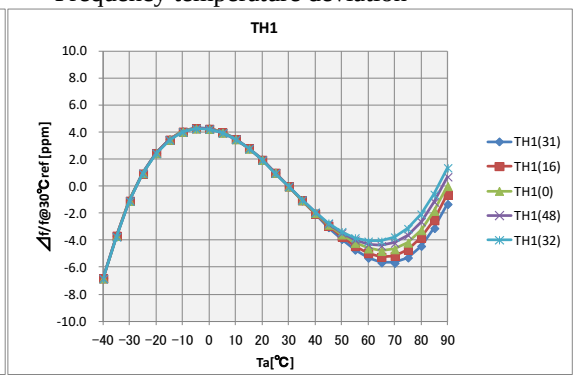
TH1 : adjust Inside for High Temperature Compensation
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

TH1[5]	TH1[4]	TH1[3]	TH1[2]	TH1[1]	TH1[0]	TH1[mV] T0+60°C
0	1	1	1	1	1	21.7
0	1	1	1	1	0	21
・・・						-
0	0	0	0	0	1	0.7
0	0	0	0	0	0	0
1	1	1	1	1	1	-0.7
・・・						-
1	0	0	0	0	1	-22.4
1	0	0	0	0	0	-23.1

<Temperature compensation voltage>



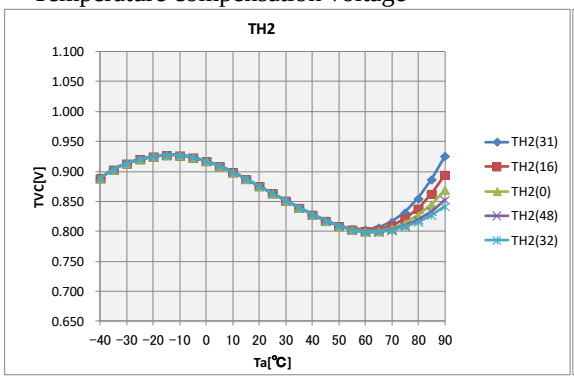
<Frequency temperature deviation>



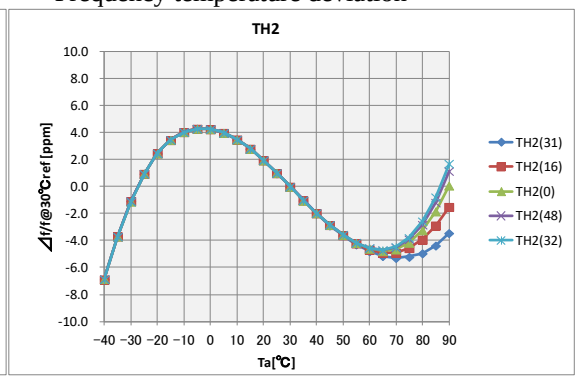
TH2 : adjust Outside for High Temperature Compensation
(TCXO mode, CA(14), GT2(1), GT1(32), T0(6), F0(46), other TC parameter(0))

TH2[5]	TH2[4]	TH2[3]	TH2[2]	TH2[1]	TH2[0]	TH2[mV] T0+60°C
0	1	1	1	1	1	56
0	1	1	1	1	0	53.8
・・・	-					
0	0	0	0	0	1	1.47
0	0	0	0	0	0	0
1	1	1	1	1	1	-1.22
・・・	-					
1	0	0	0	0	1	-27.1
1	0	0	0	0	0	-27.5

<Temperature compensation voltage>



<Frequency temperature deviation>



RVS: adjust oscillator current

RVS[1]	RVS[0]	Δ Iosc(26MHz)[uA]	Δ Iosc(52MHz)[uA]
0	0	+20	+30
0	1	+10	0
1	0	0	-20
1	1	-10	-30

HARM: Harmonic reduction mode

HARM	Harmonic reduction
0	OFF
1	ON

10.4. OTP Memory Test Mode

After writing an arbitrary data to OTP Memory, send the following command, switch the read condition to confirm strength of writing in OTP memory. If you can correctly read the codes that you wrote in OTP memory, the strength of writing in OTP memory is guaranteed.

(1) Set OP=1 using Emulation Mode (condition: V_{DDP}=V_{PP}=5V)

START condition	1	0	1	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	1	STOP condition

* X : user code

(2) Send the following command using Emulation Mode (condition :V_{DDP}=V_{PP}=5V)

START condition	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	STOP condition

(3) After setting the register with (2), set V_C=0V while keeping the state of V_{DDP}=5V

(4) Next, set V_{DDP}=3.3V

(5) Next ,set V_C=3.3V

(6) Please Read arbitrary address using Read Resister Mode

(7) Repeat (6) without turning off the power supply, and read all data for arbitrary address

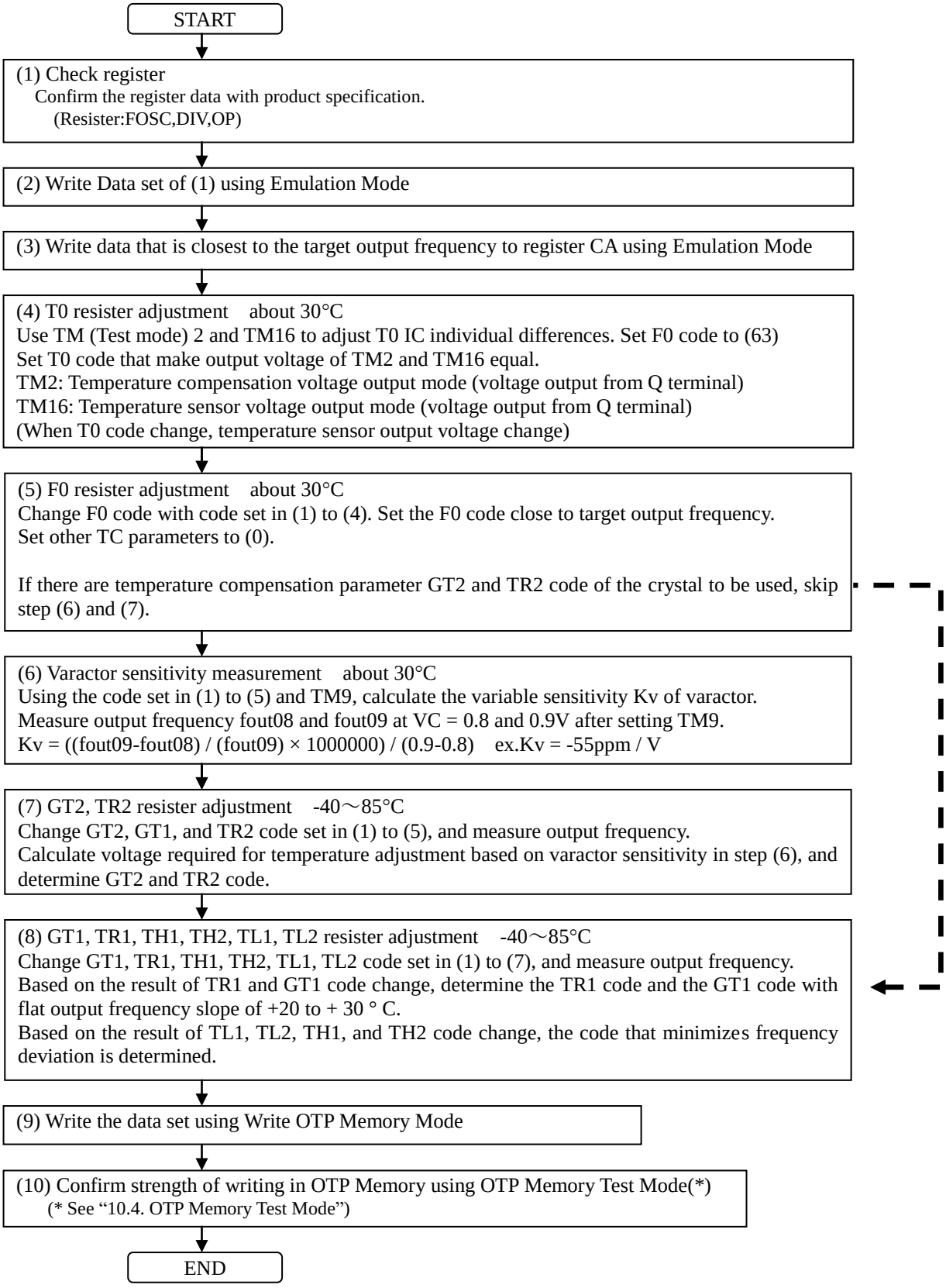
(8) Confirm that the result of (7) matches an arbitrary data

10.5. Test Mode

Mode	D7	D6	D5	D4	D3	D2	D1	D0	Set mode	VC Pin(input)	Q Pin(output)
TM0	0	0	0	0	0	0	0	0	Normal	See. Section.9.1	
TM1	0	0	0	0	0	0	0	1	Temperature sensor voltage output mode	-	V_{TEMP}
TM2	0	0	0	0	0	0	1	0	Temperature compensation voltage output mode	-	TVC
TM3	0	0	0	0	0	0	1	1	disallowance	-	-
TM4	0	0	0	0	0	1	0	0	disallowance	-	-
TM5	0	0	0	0	0	1	0	1	Reference voltage output mode	-	VREG
TM6	0	0	0	0	0	1	1	0	Reference voltage output mode	-	LDOA
TM7	0	0	0	0	0	1	1	1	disallowance	-	-
TM8	0	0	0	0	1	0	0	0	disallowance	-	-
TM9	0	0	0	0	1	0	0	1	Temperature compensation voltage variable mode (Controllable by applying the compensation voltage) * Varactor for VC is center value	TVC	f_{OUT}
TM10	0	0	0	0	1	0	1	0	Temperature sensor voltage output control mode (Controllable by applying the temperature sensor voltage)	V_{TEMP}	TVC
TM11	0	0	0	0	1	0	1	1	Variable Capacitance Lowest mode (TVC=EVC=0V)	-	f_{OUT}
TM12	0	0	0	0	1	1	0	0	Variable Capacitance Highest mode (TVC=EVC=LDOA)	-	f_{OUT}
TM13	0	0	0	0	1	1	0	1	disallowance	-	-
TM14	0	0	0	0	1	1	1	0	EVC voltage output mode.	V_C	EVC
TM15	0	0	0	0	1	1	1	1	disallowance	-	-
TM16	0	0	0	1	X	X	X	X	Temperature sensor voltage output mode	-	V_{TEMP1}
TM17	0	0	1	X	X	X	X	X	disallowance	-	-
TM18	0	1	X	X	X	X	X	X	disallowance	-	-
TM19	1	X	X	X	X	X	X	X	disallowance	-	-

* X=Don't Care

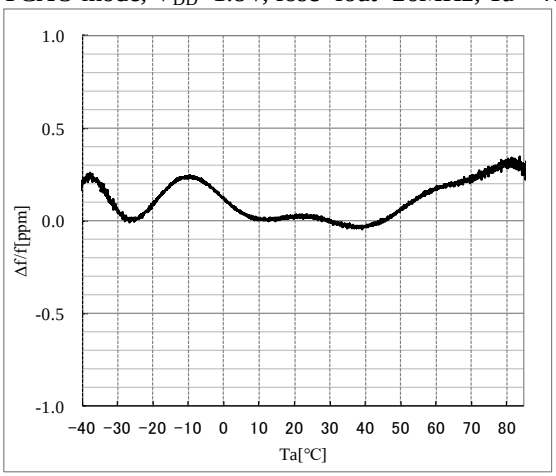
11. TEMPERATURE COMPENSATION FLOW CHART (EXAMPLE)



12. REFERENCE CHARACTERISTICS

■Temperature Compensation Characteristic

TCXO mode, V_{DD}=1.8V, fosc=fout=26MHz, Ta=-40°C to 85°C, Reference frequency at T_a=30°C,



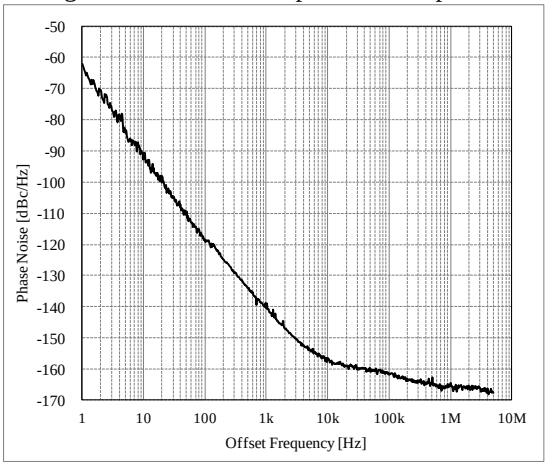
Setting Code

Address	Resister	Dec	Hex
0	CA	10	
	DIV	0	
	Bias	0	
	OP	1	A1
1	FOSC	0	
	GV	0	0
2	GT2	2	
	GT1	37	A5
3	TR2	0	
	TR1	8	8
4	VQ	0	
	T0	15	0F
5	VREG	0	
	TH1	7	7
6	RVS	1	
	TH2	2	42
7	LSFT	2	
	TL1	25	99
8	HARM	0	
	TL2	55	37
9	F0	12	0C

■Phase Noise

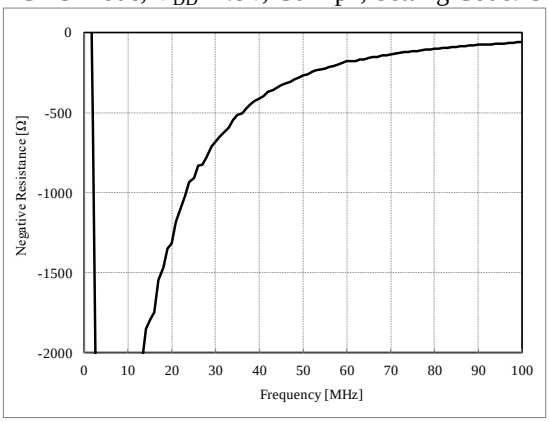
TCXO mode, V_{DD}=1.8V, fosc=fout=26MHz, Ta=R.T.

Setting code is same as temperature compensation characteristics.

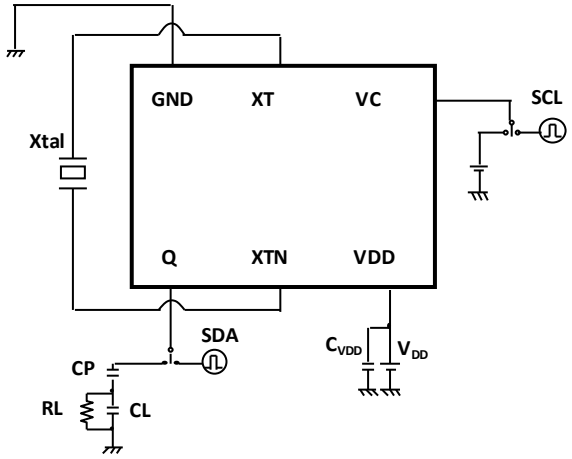


■Negative Resistance

TCXO mode, V_{DD}=1.8V, C0=1pF, Setting Code: OP(1), FOSC(6), RVS(1),other(0)



13. TYPICAL APPLICATIONS

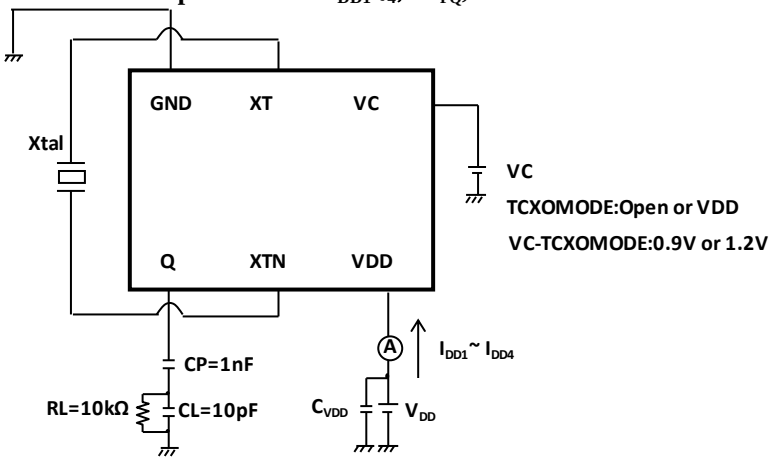


[External components]
Xtal: crystal resonator (20 MHz to 52 MHz)
R_{LOAD}: Load resistance (10 kΩ)
C_{LOAD}: Load capacitance (10 pF)
CP: resonant circuit bypass capacitor
C_{VDD}: power supply bypass capacitor

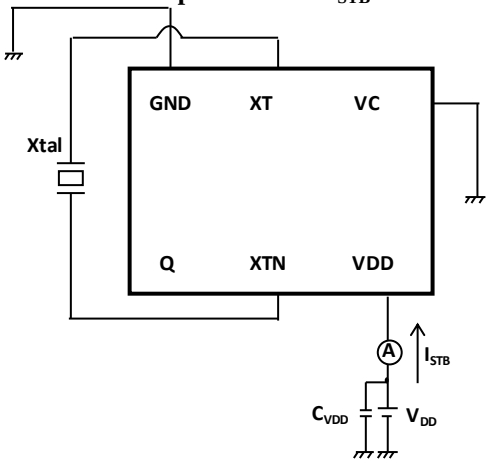
Notes: The circuit example shown above does not guarantee the operation of application products.
When designing application products, sufficiently perform evaluation and verification to use the device on your own responsibility.

14. MESUREMENT CIRCUITS

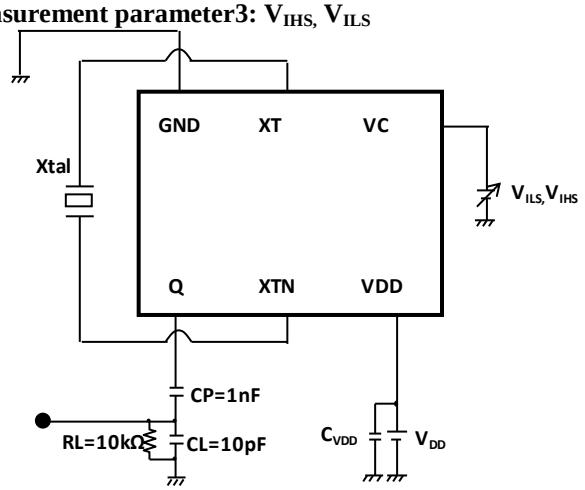
Measurement parameter1: $I_{DD1\sim4}$, V_{PQ}, HD



Measurement parameter2: I_{STB}

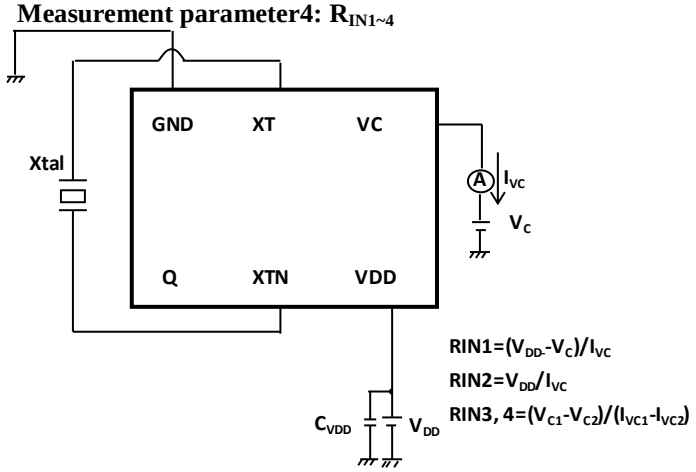


Measurement parameter3: V_{IHS}, V_{ILS}

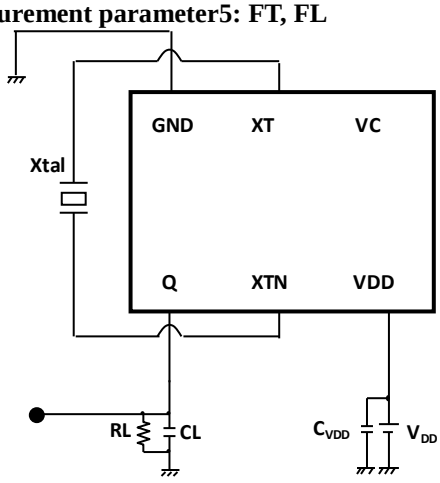


V_{ILS}: $V_{DD}\rightarrow V_{SS}$, voltage that changes disable output state
V_{IHS}: $V_{SS}\rightarrow V_{DD}$, voltage that changes enable output state

Measurement parameter4: $R_{IN1\sim4}$

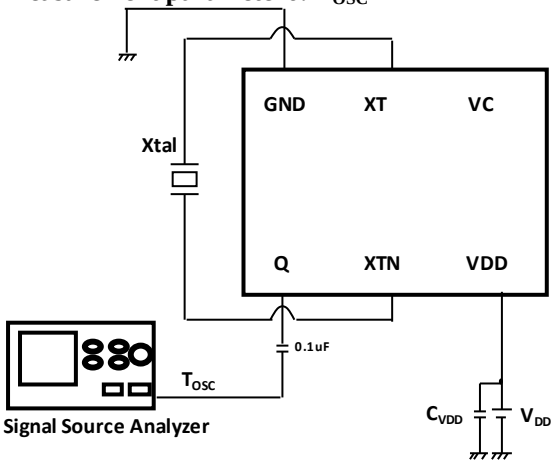


Measurement parameter5: FT, FL



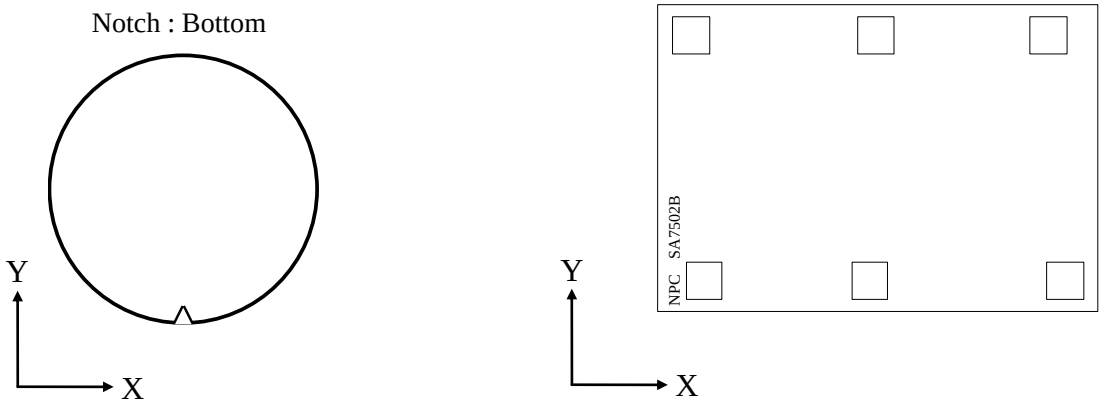
FL
CL=10pF± 10%, RL=10kΩ
or
CL=10pF, RL=10kΩ±10%

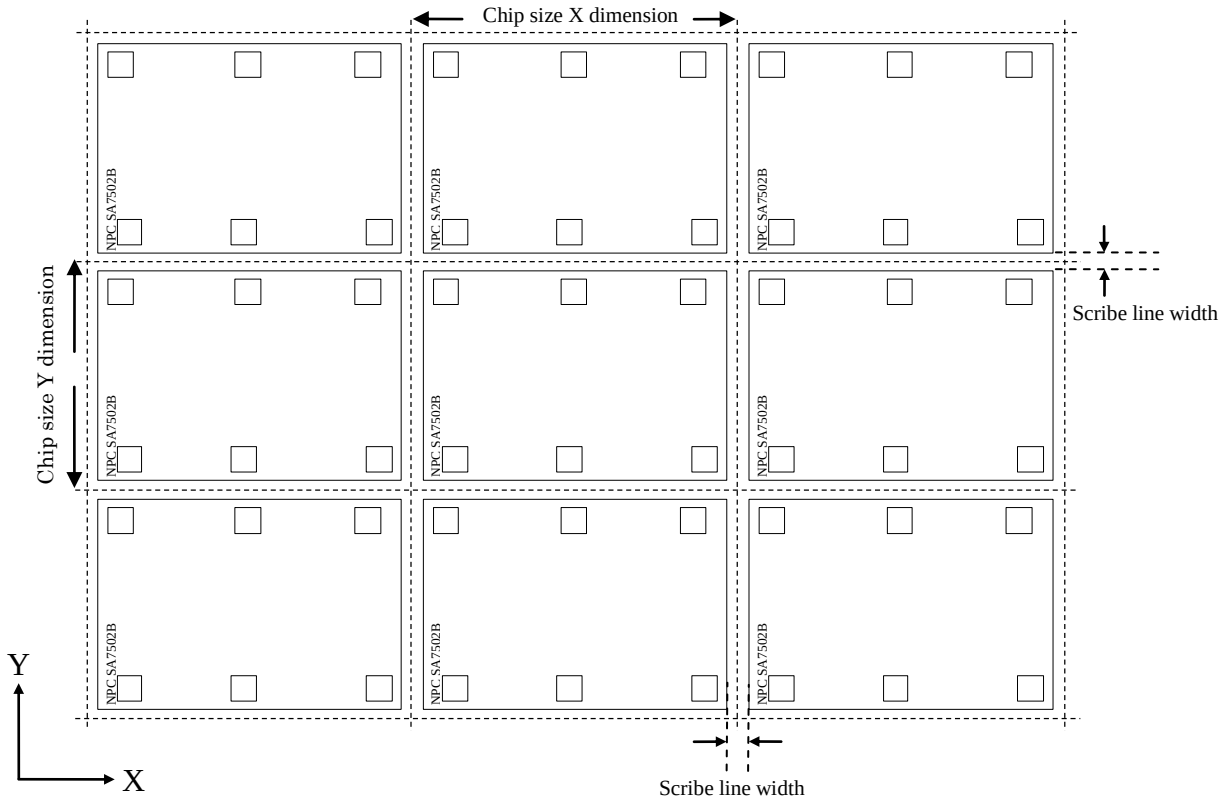
Measurement parameter6: T_{OSC}



15. WAFER SURFACE ALIGNMENT DIAGRAM

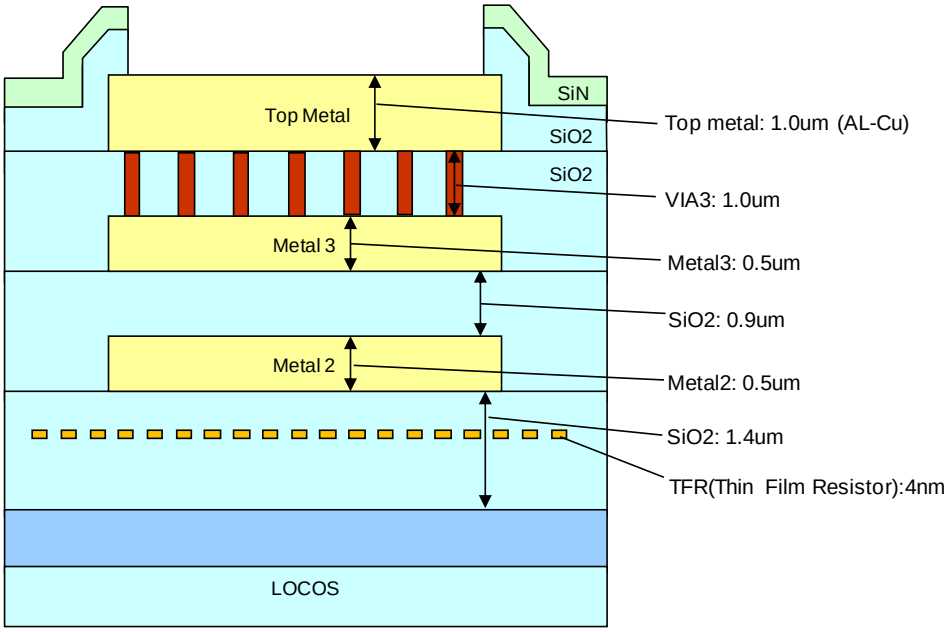
Wafer size: 200mm ± 0.5mm
Scribe line width: 60µm





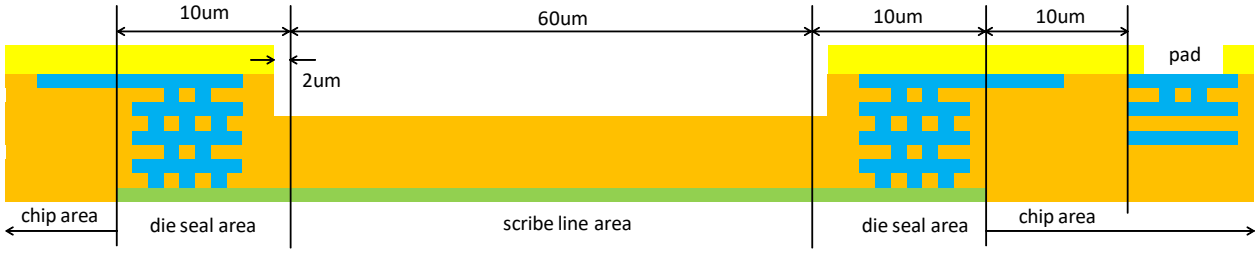
16. CROSS SECTION STRUCTURE

16.1. PAD Cross Section Structure



*Film thicknesses of mention is a value in the designs as above and is not the actual value in the chip.

16.2. Seal Ring and Scribe Line Cross Section Structure



* Widths of mention is a value in the designs as above and is not the actual value in the chip.

<Notes on UBM formation>

In UBM (Under Bump Metal) formation to the mounting pad electrode by electroless plating, UBM is similarly formed on the scribe line TEG and the metal exposed part of the accessory. So mask process covering the scribe line is required to prevent these effects.

17. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.
If you wish to use this product in equipment requiring extremely high level of reliability, please contact our sales department or representative in advance.
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