#### 1. OVERVIEW

The CF7321xx/WF7321xx is a 122.88MHz oscillator frequency, CMOS output, VCXO module IC. It incorporates a bipolar oscillator circuit and varicap diode built-in for low phase noise characteristic and wide frequency pulling range.

#### 2. FEATURES

- Varicap diode built-in Oscillator: Fundamental frequency oscillation
- Output frequency (f<sub>OUT</sub>): 30 to 122.88MHz
- Oscillator frequency: 60 to 122.88MHz (7321Bx versions)
- Frequency divider output: Available in fundamental (f<sub>OSC</sub>) and half frequency (f<sub>OSC</sub>/2) output versions
  - Low standby current Oscillator stopped, power saving pull-up resistor built-in
- Output type:
- CMOS Operating voltage: 3.135 to 3.465V
- Phase noise characteristics(typ):-80dBc/Hz (B1 version, 10Hz offset, f=122.88MHz (γ=300, C0=1.5pF))
  - -136dBc/Hz (B1 version, 1kHz offset, f=122.88MHz )
    - -161dBc/Hz (B1 version, 10MHz offset, f=122.88MHz)
- Frequency pulling range(typ):  $\pm 40$  ppm (B1 version, V<sub>C</sub>=1.65  $\pm$  1.65V, f=122.88MHz ( $\gamma$ =300, C0=1.5pF))

# 3. BLOCK DIAGRAM



### 4. PAD LAYOUT

- (1) Chip size:  $^{*1}$
- (2) Rear surface potential:

V<sub>ss</sub> 80μm × 80μm (VSS PAD 80μm × 160μm) (3) Pad size:

X=0.94mm, Y=0.90mm

- (4) Chip dimensions
- \*1: Chip size is the distance between the scribe line centers.



No.	Name	Х	Y
1	XT	-365.0	177.0
2	XTN	-365.0	-98.0
3	VC	-55.4	-345.0
4	INHN	113.2	-345.0
5	VSS	357.0	-305.0
6	Q	351.9	345.0
7	VDD	70.1	345.0

#### Pad coordinates (origin at chip center) Unit: [µm]

#### 5. PAD DESCRIPTION

No.	Name	I/O	Function
1	XT	Ι	Crystal element connection terminals.
2	XTN	0	Connect crystal between XT and XTN
3	VC	Ι	Control voltage input.
4	INHN	Ι	Output enable input. Oscillation stopped and the device goes into standby mode when Low. Power saving pull-up resistor built-in.
5	VSS	-	Ground
6	Q	Ο	Clock output High-impedance when standby mode
7	VDD	-	Supply voltage

\*I: Input, O: Output

### 6. SERIES LINEUP

Device	Recommended oscillation frequency range $(f_{OSC})^{*1}$	Output frequency (f <sub>OUT</sub> )
7321B1	60 to 122.88MHz	$f_{OSC}$
7321B2	30 to 61.44MHz	f <sub>OSC</sub> /2

\*1: Recommended values based on IC characteristics.

The oscillator characteristics are determined by the combination of crystal element and the IC, hence the actual oscillator is not limited to these values. Always conduct thorough circuit evaluation beforehand. The recommended characteristics for the crystal element are:

Bx versions:  $R1 < 20\Omega$ , C0 < 1.5pF

### 7. ABSOLUTE MAXIMUM RATINGS

					$V_{SS}=0V$
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage range <sup>*1</sup>	$V_{DD}$	VDD		-0.3 to +5.0	V
Input voltage range <sup>*1,*3</sup>	$V_{IN}$	XT, INHN,	VC	-0.3 to $V_{DD}$ +0.3	V
Output voltage range <sup>*1,*3</sup>	V <sub>OUT</sub>	XTN, Q		-0.3 to V <sub>DD</sub> +0.3	V
Junction temperature <sup>*2</sup>	$T_j$			+125	°C
Storage temperature range <sup>*4</sup>	T <sub>STG</sub>	Wafers, chips		-55 to +125	°C
Q (m (m m m * 2	т	0	$T_a = -40 \sim +85^{\circ}C$	$\pm 20$	mA
Output current	LOUT	Q	$T_a = -40 \sim +105^{\circ}C$	±10	mA

\*1: Parameters must not exceed ratings, not even momentarily. If a rating is exceeded, there is a risk of IC failure, deterioration in characteristics, and decrease in reliability.

\*2: Parameters should not exceed ratings. If a rating is exceeded, there is a risk of deterioration in characteristics and decrease in reliability.

\*3: Recommended operating voltage V<sub>DD</sub> value.

\*4: Store separately in Nitrogen or vacuum atmosphere.

### 8. RECOMMENDED OPERATING CONDITIONS

						V <sub>SS</sub> =0V
Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Unit
Operating supply voltage	V <sub>DD</sub>	Between VDD and VSS <sup>*2</sup>	3.135	3.3	3.465	V
Input voltage	V <sub>IN</sub>	INHN, VC	0		$V_{DD}$	V
Operating temperature	T <sub>a</sub>		-40		105	°C
Output load	CL				15	pF
Oscillator frequency <sup>*1</sup>	f <sub>OSC</sub>	7321Bx	60		122.88	MHz
Output frequency	f <sub>OUT</sub>	7321B1	60		122.88	MHa
Output frequency		7321B2	30		61.44	IVITIZ

\*1: The characteristics will vary greatly depending on the crystal element characteristics and mounting conditions. Use only after thorough evaluation of the oscillator characteristics.

\*2: For stable device operation, connect 0.01µF or larger ceramic chip capacitors between VDD and VSS, mounted as close as possible to the IC (within approximately 3mm). Also, use as thick a wiring pattern as possible between the IC and the capacitors.

\*Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

# 9. ELECTRICAL CHARACTERISTICS

# 9

<b>9.1.</b> B1, B2 Version	ns			40 . 1	0.500 1		
Parameter	Symbol	$V_{DD} = 3.135 \text{ to } 3.465 \text{ V}, \text{ V}_{C}$	=-40  to  +10	US°C unle	MAX	se noted	
Current consumption B1 version	I <sub>DD</sub>	Measurement circuit 1, no load INHN=Open f <sub>OSC</sub> =122.88MHz, f <sub>OUT</sub> =122.88MHz			8.0	14.0	mA
Current consumption B2 version	I <sub>DD</sub>	Measurement circuit 1, no load INHN=Open f <sub>OSC</sub> =122.88MHz, f <sub>OUT</sub> =61.44MHz Vpp=3.3V			7.0	12.0	mA
Standby current	I <sub>STB</sub>	Measurement circuit 1 INHN=LOW	$\Gamma_{a} = -40 \sim +85^{\circ}C$ $\Gamma_{a} = -40 \sim +105^{\circ}C$			10 100	μA
HIGH-level output voltage	V <sub>OH</sub>	Measurement circuit 2, I <sub>OH</sub> =-4mA	Q output	V <sub>DD</sub> -0.4			v
LOW-level output voltage	V <sub>OL</sub>	Measurement circuit 2, I <sub>OL</sub> =4mA	Q output			0.4	v
Output leakage current	IZ	Measurement circuit 3, INHN=Low, T <sub>a</sub> =25°C	Q output	-1		1	μΑ
HIGH-level input voltage	V <sub>IH</sub>	Measurement circuit 4, INHN input		$0.7V_{DD}$			V
LOW-level input voltage	V <sub>IL</sub>	Measurement circuit 4, INHN input				0.3V <sub>DD</sub>	V
Pull-up resistance1	R <sub>PU1</sub>	Measurement circuit 5, INHN input INHN=0V		1	4	9	MΩ
Pull-up resistance2	R <sub>PU2</sub>	Measurement circuit 5, INHN input INHN=0.7V <sub>DD</sub>		50	100	200	kΩ
Oscillator internal	R <sub>VC1</sub>	Between VC-XT, measure	urement circuit 6	70	140	210	1-0
resistance	R <sub>VC2</sub>	Between VC-XTN, mea	asurement circuit 6	70	140	210	K\$2
Input leakage resistance	R <sub>VIN</sub>	VC, T <sub>a</sub> =25°C, measurement circuit 7		10			MΩ
			V <sub>C</sub> =0.3V	4.38	4.86	5.35	
Oscillator capacitance	C <sub>VC1</sub>	Confirmed using wafer	V <sub>C</sub> =1.65V	2.62	3.08	3.55	pF
		monitor pattern, design	V <sub>C</sub> =3.0V	1.38	1.72	2.06	
		value, excluding parasit	tic $V_{\rm C}=0.3\rm V$	6.24	6.94	7.63	pF
	C <sub>VC2</sub>	capacitance	V <sub>C</sub> =1.65V	3.70	4.36	5.01	
			V <sub>C</sub> =3.0V	1.89	2.36	2.83	
	C <sub>XT</sub>	Confirmed using wafer	Confirmed using wafer monitor pattern,		6	8	- T
	C <sub>XTN</sub>	capacitance		4	6	8	рг

Maximum modulation

frequency

 $F_M$ 

-3dB frequency, T<sub>a</sub>=25°C, design value,

circuit 8, f<sub>OSC</sub>=122.88MHz

 $V_{DD}$ =3.3V,  $V_{C}$ =1.65 ± 1.65V, measurement

20

50

kHz

# 10. SWITCHING CHARACTERISTICS

#### 10.1. B1, B2 Versions

 $V_{DD}$ =3.135 to 3.465V,  $V_{C}$ =0.5 $V_{DD}$ ,  $V_{SS}$ =0V,  $T_{a}$ =-40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Unit
HIGH-level output voltage	V <sub>TOP</sub>	$C_L$ =15pF, measurement circuit 9	$0.9 \mathrm{V_{DD}}$			V
LOW-level output voltage	V <sub>BASE</sub>	C <sub>L</sub> =15pF, measurement circuit 9			$0.1 V_{\text{DD}}$	V
Duty cycle	Duty	$T_a = 25^{\circ}C$ , $V_{DD} = 3.3V$ , measurement circuit 9	45	50	55	%
Output rise time	t <sub>r</sub>	$C_L=15$ pF, output amplitude, measurement circuit 9, $0.1V_{DD}\rightarrow 0.9V_{DD}$		1.5	3.0	ns
Output fall time	t <sub>f</sub>	$C_L=15$ pF, output amplitude, measurement circuit 9, $0.9V_{DD}\rightarrow 0.1V_{DD}$		1.5	3.0	ns
Output enable propagation delay <sup>*1</sup>	t <sub>OE</sub>	T <sub>a</sub> =25°C, measurement circuit 10 INHN="Low"→"High"			2	ms
Output disable propagation delay	t <sub>OD</sub>	T <sub>a</sub> =25°C, measurement circuit 10 INHN="High"→"Low"			200	ns

\*1: Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

#### Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended. The recommended crystal element characteristics are  $R1 < 20\Omega$  and C0 < 1.5pF.

# **Timing Diagrams**



### 11. FUNCTIONAL DESCRIPTION

#### **11.1. INHN Function**

When INHN pin goes Low, the Q pin becomes high impedance and the oscillation stops.

INHN	Q	Oscillator
High(Open)	f <sub>OUT</sub>	Operating
Low	Disabled (Hi-Z)	Disabled

#### 11.2. Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes in response to the input level (High or Low). When INHN pin is tied Low (standby state), the pull-up resistance becomes large ( $R_{PU1}$ ), reducing the current consumed by the resistance. When INHN pin is open circuit, the pull-up resistance becomes small ( $R_{PU2}$ ), decreasing the susceptibility to the effects of external noise.

#### **11.3.** Oscillation Detection Function

The 7321 series incorporate an oscillation detector circuit.

The oscillation detector circuit disables the Q output until crystal oscillation becomes stable when oscillation circuit starts up. This reduces the risk of abnormal oscillation behavior when in the initial power up and in a reactivation by INHN.

#### 11.4. Boot Function

At the time of oscillation starting, XTN pin potential is made into the  $V_{DD}$  level. It makes negative resistance enlarged and it becomes easy to start oscillation. Beware that a current flows into VC pin until it starts oscillation, when XTN pin is  $V_{DD}$  level and the voltage below  $V_{DD}$  level is being applied to VC pin.

A boot function is canceled after an oscillation start.

# 12. REFERENCE CHARACTERISTICS EXAMPLE (7321Bx Typical Characteristics)

The characters given below were measured using an NPC standards jig and standard crystal element, and do not represent a guarantee of device characteristics.

Note that the characteristics will vary due to measurement environment and the oscillator element used.

Crystal used for evaluation				
Parameter	B1			
f <sub>OSC</sub> (MHz)	122.88			
C0 (pF)	1.8			
γ (=C0/C1)	354			
$R1(\Omega)$	8.1			



#### 12.1. Pulling Range

[Measurement condition]  $V_{DD}=3.3V$ ,  $V_{SS}=0V$ , Ta=25°C

#### [7321Bx]f<sub>OSC</sub>=122.88MHz



#### [Measurement circuit diagram]



#### 12.2. Phase Noise

$$\label{eq:vd} \begin{split} & [Measurement \ condition] \\ & V_{DD} \!\!=\!\! 3.3 V, \ \! V_{SS} \!\!=\!\! 0 V, \ \! Ta \!\!=\!\! 25^{\circ} \! C \end{split}$$



# $[7321B2]f_{OSC} = 122.88MHz, f_{OUT} = 61.44MHz$



### [Measurement circuit diagram]



12.3. Modulation Bandwidth

[Measurement condition]  $V_{DD}$ =3.3V,  $V_{SS}$ =0V, Ta=25°C



 $[7321B1]f_{OSC} = 122.88MHz, f_{OUT} = 122.88MHz$ 

# $[7321B2]f_{OSC} = 122.88MHz, f_{OUT} = 61.44MHz$



[Measurement circuit diagram] P22. Measurement circuit 8.

**12.4.** Negative Resistance

[Measurement condition]  $V_{DD}$ =3.3V,  $V_{SS}$ =0V, Ta=25°C, C0=0pF



At the time of oscillation starting, negative resistance becomes deep by boot function. The boot function is released when oscillation is steady, and oscillation output starts.



Measurement results using 4396B Agilent analyzer on NPC test jig. Measurements will vary with test jig and measurement environment.

#### 12.5. Drive Level

[Measurement condition]  $V_{DD}$ =3.3V, Ta=25°C





[Measurement circuit diagram]



 $DL = (IX' tal)^2 \times Re$ 

IX'tal : Current though Crystal(RMS) Re : Crystal's effective resistance

#### **12.6.** Oscillator CL Characteristics

[Measurement condition]

 $V_{DD}$ =3.3V,  $V_{SS}$ =0V, Ta=25°C

#### $[7321Bx]f_{OSC} = 122.88MHz$



#### [Measurement circuit diagram]





#### **12.7.** VC Terminal Input Impedance

[Measurement condition] Ta= $25^{\circ}$ C, V<sub>C</sub>=0V



[Measurement circuit diagram]



**12.8.** Current Consumption

[Measurement condition] Ta=25°C, no load



 $[7321B1]f_{OSC} = 122.88MHz, f_{OUT} = 122.88MHz$ 

# $[7321B2]f_{OSC} = 122.88MHz, f_{OUT} = 61.44MHz$



[Measurement circuit diagram] P18. Measurement circuit 1.

### 12.9. Output Waveform

[Measurement condition]  $V_{DD}$ =3.3V,  $V_{C}$ =1.65V, Ta=25°C



[Measurement circuit diagram]P22. Measurement circuit 9.

Measurement equipment: Oscilloscope DSO80604B(Agilent), Differential probe 1134A (Probe head E2678A)

### **13. MEASUREMENT CIRCUITS**

These measurement circuits are used for the evaluation of the electrical and switching characteristics.

#### Notes

Connect the bypass capacitors, specified in the measurement circuits, VDD/-VSS.

Connect the bypass capacitors and load resistors with wiring pattern as short as possible (less than 3mm length). If the wiring pattern is too long, the desired characteristics cannot be obtained.

Note that if bypass capacitors and load resistors other than the specified values are connected, or if the components are not connected at all, the desired characteristics cannot be obtained.

\* Capacitor and resistor values used by NPC

• Capacitors: 0.01µF GRM188B11H103K (Murata Manufacturing Co., Ltd.)

### **13.1.** Measurement Circuit 1 Measurement parameter: I<sub>DD</sub>, I<sub>STB</sub>



Figure 13-1. Measurement circuit 1



Figure 13-2. Measurement circuit 2





Figure 13-3. Measurement circuit 3

### **13.4.** Measurement Circuit 4 Parameter:V<sub>IH</sub>, V<sub>IL</sub>





Figure 13-4. Measurement circuit 4



Figure 13-5. Measurement circuit 5

#### **13.6.** Measurement Circuit 6 Parameters: R<sub>VC1</sub>, R<sub>VC2</sub>



Figure 13-6. Measurement circuit 6

### **13.7.** Measurement Circuit 7 Parameters : R<sub>VIN</sub>



Figure 13-7. Measurement circuit 7





Figure 13-8. Measurement circuit 8





Figure 13-9. Measurement circuit 9

### **13.10.** Measurement Circuit 10 Parameter: t<sub>OE</sub>, t<sub>OD</sub>



Figure 13-10. Measurement circuit 10

# 14. WAFER SURFACE ORIENTATION DIAGRAM

Scribe line width : 70µm



#### **15. USAGE AND PRECAUTIONS**

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