1. OVERVIEW

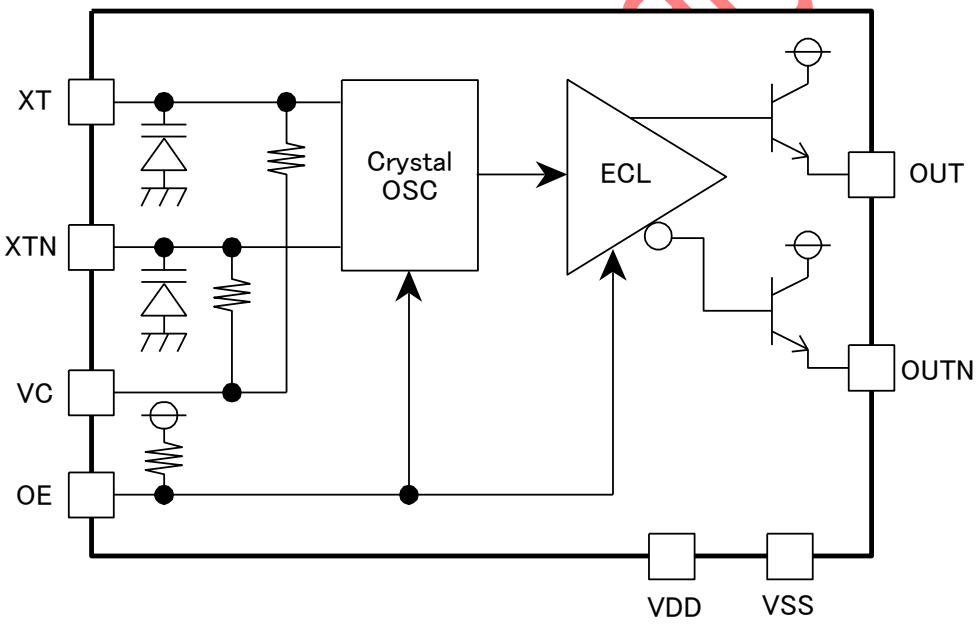
The CF7320/WF7320 series are LV-PECL output VCXO module ICs.
It supports 100MHz to 250MHz fundamental-frequency and +105°C operation. It incorporates a bipolar oscillator circuit and a varactor built-in for low phase noise characteristic and wide frequency pulling range. The miniature chip size enables it to be implemented in a 2520 or 3225 size SMD package.

2. FEATURES

- Oscillator : Fundamental frequency oscillation
- Output frequency (f_{OUT}) : 100 to 170MHz (7320A version)
  : 170 to 250MHz (7320B version)
- Oscillator frequency : 100 to 170MHz (7320A version)
  : 170 to 250MHz (7320B version)
- Output type : Differential LV-PECL
- Operating voltage : 2.97 to 3.63V
- Phase noise characteristics(typ) : (-126dBc/Hz @7320A version) (1kHz offset, f=122.88MHz)
  : (-162dBc/Hz @7320A version) (1MHz offset, f=122.88MHz)
- Frequency pulling range(typ) :(±120ppm@7320A version) (V_C=1.65 ± 1.65V, f=122.88MHz)

*() target value

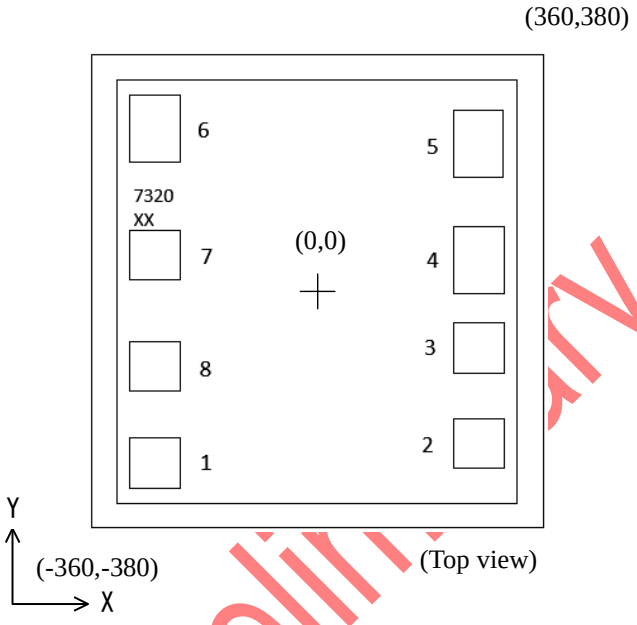
3. BLOCK DIAGRAM



4. PAD DIMENSIONS

(1) Chip size:*1 X=0.72mm, Y=0.76mm
(2) Rear surface potential: V_{SS}
(3) Pad size: 80µm × 80µm (XT, XTN, VC, OE, VSS)
80µm × 110µm (OUT, OUTN, VDD)
(4) Chip dimensions

*1: Chip size is the distance between the scribe line centers.



Pad coordinates (origin at chip center) Unit: [µm]

No.	Name	X	Y
1	VC	-258	-276
2	OE	258	-244
3	VSS	258	-91
4	OUT	258	50
5	OUTN	258	237
6	VDD	-258	261
7	XT	-258	58
8	XTN	-258	-121

5. PAD DESCRIPTION

No.	Name	I/O	Function
1	VC	I	Control voltage input.
2	OE	I	Output enable input. With pull-up built-in. Refer to section 14-1 for OE function.
3	VSS	-	Ground
4	OUT	O	Clock output (differential output)
5	OUTN	O	Clock output (differential inverted output)
6	VDD	-	Supply voltage
7	XT	I	Crystal element connection terminals.
8	XTN	O	

*I: Input, O: Output

6. SERIES LINEUP

Version name	Recommended oscillation frequency range (f_{OSC})*1	Operating temperature
7320A	100MHz ~ 170MHz	-40～105°C
7320B	170MHz ~ 250MHz	

*1: Recommended values based on IC characteristics.
The oscillator characteristics are determined by the combination of crystal element and the IC, hence the actual oscillator is not limited to these values. Always conduct thorough characteristic evaluation beforehand. The recommended characteristics for the crystal element are R1 < 20Ω, C0=1 to 1.5pF.

7. ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range*1	V_{DD}	Voltage between VDD and VSS	-0.3 ~ +4.5	V
Input voltage range*1,*3	V_{IN}	XT, OE, VC pin	-0.3 ~ V_{DD}+0.3	V
Output voltage range*1,*3	V_{OUT}	XTN, OUT, OUTN pin	-0.3 ~ V_{DD}+0.3	V
Junction temperature*2	T_j		+150	°C
Storage temperature range*4	T_{STG}	Chip form wafer form	-55 ~ +150	°C

*1: Parameters must not exceed ratings, not even momentarily. If the rating is exceeded, it may affect the electrical characteristics and reliability.
*2: V_{DD} is the V_{DD} value of recommended operating conditions.
*3: Do not exceed the absolute maximum ratings. If they are exceeded, device characteristics and reliability will be degraded.
*4: When stored alone in nitrogen or vacuum atmosphere.

8. RECOMMENDED OPERATING CONDITIONS

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating supply voltage	V_{DD}	Between VDD and VSS*2	2.97	3.3	3.63	V
Input voltage	V_{IN}	OE, OEN, VC	0	-	V_{DD}	V
Operating temperature	T_a	-	-40	-	105	°C
Output load	R_L	V_{DD}-2V termination	49.5	50.0	50.5	Ω
Oscillator frequency*1	f_{OSC}	7320A version	100	-	170	MHz
		7320B version	170	-	250	

*1: The characteristics will vary greatly depending on the crystal element characteristics and mounting conditions. Use only after thorough evaluation of the oscillator characteristics.
*2: For stable device operation, connect 0.01µF or larger ceramic chip capacitors between VDD and VSS, mounted as close as possible to the IC (within approximately 3mm). Also, use as thick a wiring pattern as possible between the IC and the capacitors.

*Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

9. ELECTRICAL CHARACTERISTICS

9.1. 7320A version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a=-40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption 1	I_{DD1}	OE=Open, V_{DD}-2V termination, Measurement circuit 1		-	(48)	(70)	mA
Current consumption 2	I_{DD2}	OE=Low, V_{DD}-2V termination, Measurement circuit 1, oscillator operating, outputs disabled		-	(4.5)	(8.2)	mA
HIGH-level output voltage	V_{OH}	OUT/OUTN pin, V_{DD}=3.3V, OE=Open, V_{DD}-2V termination, Measurement circuit 2		(2.2)	(2.35)	-	V
LOW-level output voltage	V_{OL}	OUT/OUTN pin, V_{DD}=3.3V, OE=Open, V_{DD}-2V termination, Measurement circuit 2		-	(1.6)	(1.8)	V
Output leakage current	I_Z	OUT/OUTN pin, OE=Low, T_a=25°C, V_{DD}-2V termination		-1	-	1	µA
HIGH-level input voltage	V_{IH}	OE pin, Measurement circuit 1		0.7V_{DD}	-	-	V
LOW-level input voltage	V_{IL}	OE pin, Measurement circuit 1		-	-	0.3V_{DD}	V
Pull-up resistance	R_{PU}	OE pin, Measurement circuit 1		50	100	200	kΩ
Input leakage resistance	R_{VIN}	VC pin, T_a=25°C		10	-	-	MΩ
Oscillator capacitance	C_{VC1}	Design value	V_C =0.3V	-	(8.6)	-	pF
			V_C =1.65V	-	(6.1)	-	
			V_C =3.0V	-	(5.6)	-	
	C_{VC2}	Design value	V_C =0.3V	-	(16.8)	-	pF
			V_C =1.65V	-	(12.0)	-	
			V_C =3.0V	-	(6.5)	-	
Maximum modulation frequency	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=3.3V, V_C=1.65 ± 1.65V, f_{OSC}:122.88MHz		25	-	-	kHz

9.2. 7320B version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a=-40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption 1	I_{DD1}	OE=Open, V_{DD}-2V termination, Measurement circuit 1		-	(53)	(81)	mA
Current consumption 2	I_{DD2}	OE=Low, V_{DD}-2V termination, Measurement circuit 1, oscillator operating, outputs disabled		-	(6.3)	(10.3)	mA
HIGH-level output voltage	V_{OH}	OUT/OUTN pin, V_{DD}=3.3V, OE=Open, V_{DD}-2V termination, Measurement circuit 2		(2.2)	(2.35)	-	V
LOW-level output voltage	V_{OL}	OUT/OUTN pin, V_{DD}=3.3V, OE=Open, V_{DD}-2V termination, Measurement circuit 2		-	(1.6)	(1.8)	V
Output leakage current	I_Z	OUT/OUTN pin, OE=Low, T_a=25°C, V_{DD}-2V termination		-1	-	1	µA
HIGH-level input voltage	V_{IH}	OE pin, Measurement circuit 1		0.7V_{DD}	-	-	V
LOW-level input voltage	V_{IL}	OE pin, Measurement circuit 1		-	-	0.3V_{DD}	V
Pull-up resistance	R_{PU}	OE pin, Measurement circuit 1		50	100	200	kΩ
Input leakage resistance	R_{VIN}	VC pin, T_a=25°C		10	-	-	MΩ
Oscillator capacitance	C_{VC1}	Design value	V_C =0.3V	-	(7.8)	-	pF
			V_C =1.65V	-	(6.1)	-	
			V_C =3.0V	-	(5.7)	-	
	C_{VC2}	Design value	V_C =0.3V	-	(15.3)	-	pF
			V_C =1.65V	-	(11.8)	-	
			V_C =3.0V	-	(7.6)	-	
Maximum modulation frequency	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=3.3V, V_C=1.65 ± 1.65V, f_{OSC}:245.76MHz		25	-	-	kHz

10. SWITCHING CHARACTERISTICS

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a=-40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Duty cycle	Duty1	Measured at output crossing point T_a=25°C, V_{DD}=3.3V, Measurement circuit 2	45	50	55	%
	Duty2	Measured at 50% output amplitude T_a=25°C, V_{DD}=3.3V, Measurement circuit 2	45	50	55	%
Output amplitude	V_{OPP}	Peak-to-peak output waveform, single-ended output signal, Measurement circuit 2	0.4	-	-	V
Output rise time	t_r*2	20 to 80% output amplitude, single-ended output signal, Measurement circuit 2	-	(0.2)	(0.4)	ns
Output fall time	t_f*2	80 to 20% output amplitude, single-ended output signal, Measurement circuit 2	-	(0.2)	(0.4)	ns
Output enable propagation delay*1	t_{OE}	T_a=25°C, design value	-	-	(20)	µs
Output disable propagation delay	t_{OD}	T_a=25°C, design value	-	-	(200)	ns

*1: Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

Notes

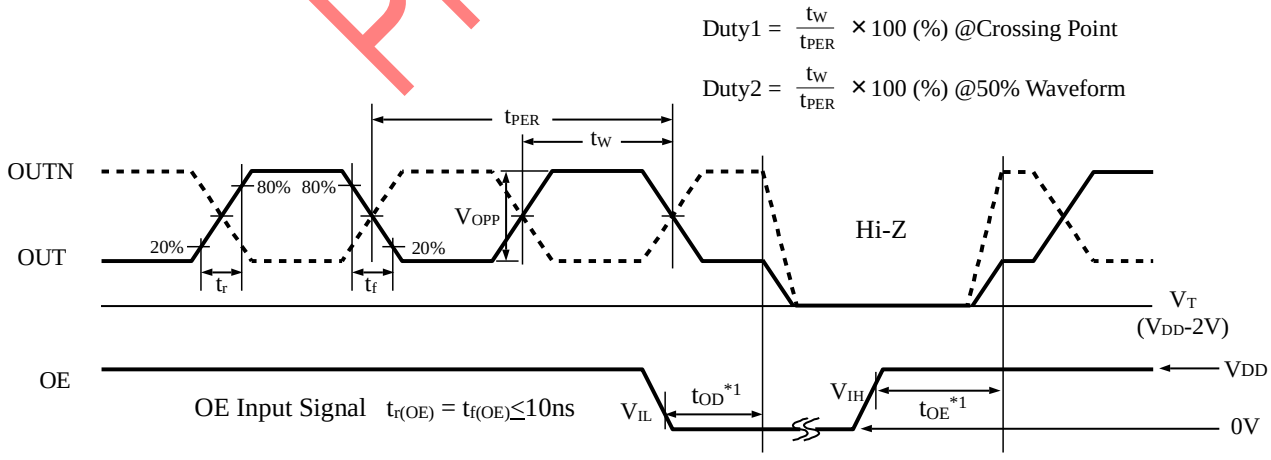
The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

The recommended crystal element characteristics are R1 < 20Ω and C0=1 to 1.5pF.

*2. Output rise time and output fall time may vary depending on measurement environment.

11. Timing Diagrams

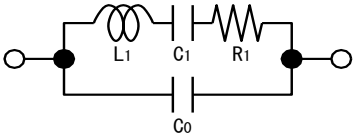


*1: On an OE falling edge, the outputs go high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) has elapsed. When this occurs, the output signal is pulled down to V_T (termination voltage) by the load resistance. On an OE rising edge, the output starts after the output enable propagation delay (t_{OE}) has elapsed.

12. REFERENCE CHARACTERISTICS EXAMPLE (7320A,B Typical Characteristics)

Crystal used for evaluation

Parameter	A	B
f_{OSC} (MHz)		
C0 (pF)		
R1 (Ω)		
γ (=C0/C1)		



T.B.D

13. MEASUREMENT CIRCUITS

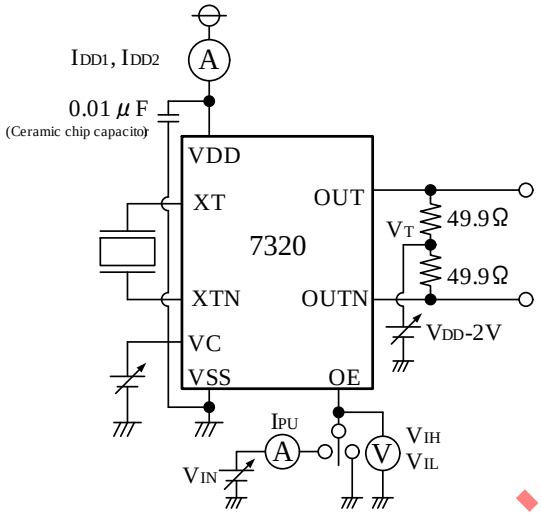
These measurement circuits are used for the evaluation of the electrical and switching characteristics.

***** Cautions for output waveform *****

To obtain good waveform characteristics, place a ceramic chip capacitor of 0.01 μF (or more) between the VDD and VSS pins of the IC (within about 3 mm).

13.1. Measurement circuit 1

Measurement parameters: **I_{DD1}, I_{DD2}, V_{IH}, V_{IL}, R_{PU}**



$$R_{PU} = \frac{V_{DD}}{I_{PU}} \quad (V_{IN} = 0V)$$

V_{IH} : $V_{SS} \rightarrow V_{DD}$ voltage that changes output state
V_{IL} : $V_{DD} \rightarrow V_{SS}$ voltage that changes output state

Fig 13-1. Measurement circuit 1

13.2. Measurement circuit 2

Measurement parameters: **Duty1, Duty2, V_{OPP}, t_r, t_f, V_{OH}, V_{OL}**

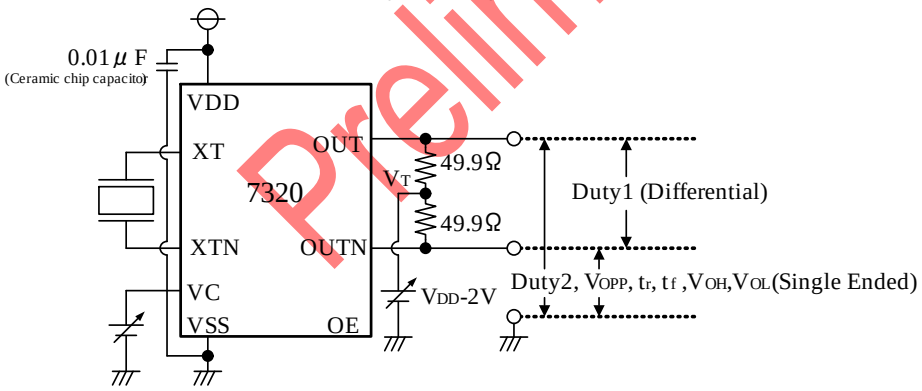
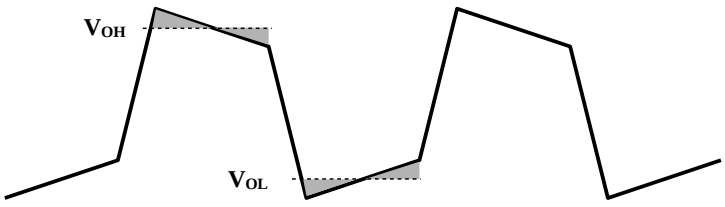


Fig 13-2. Measurement circuit 1

*If there is no flat area when measuring VOH and VOL, take the average value.



14. FUNCTIONAL DESCRIPTION

14.1. OE Function

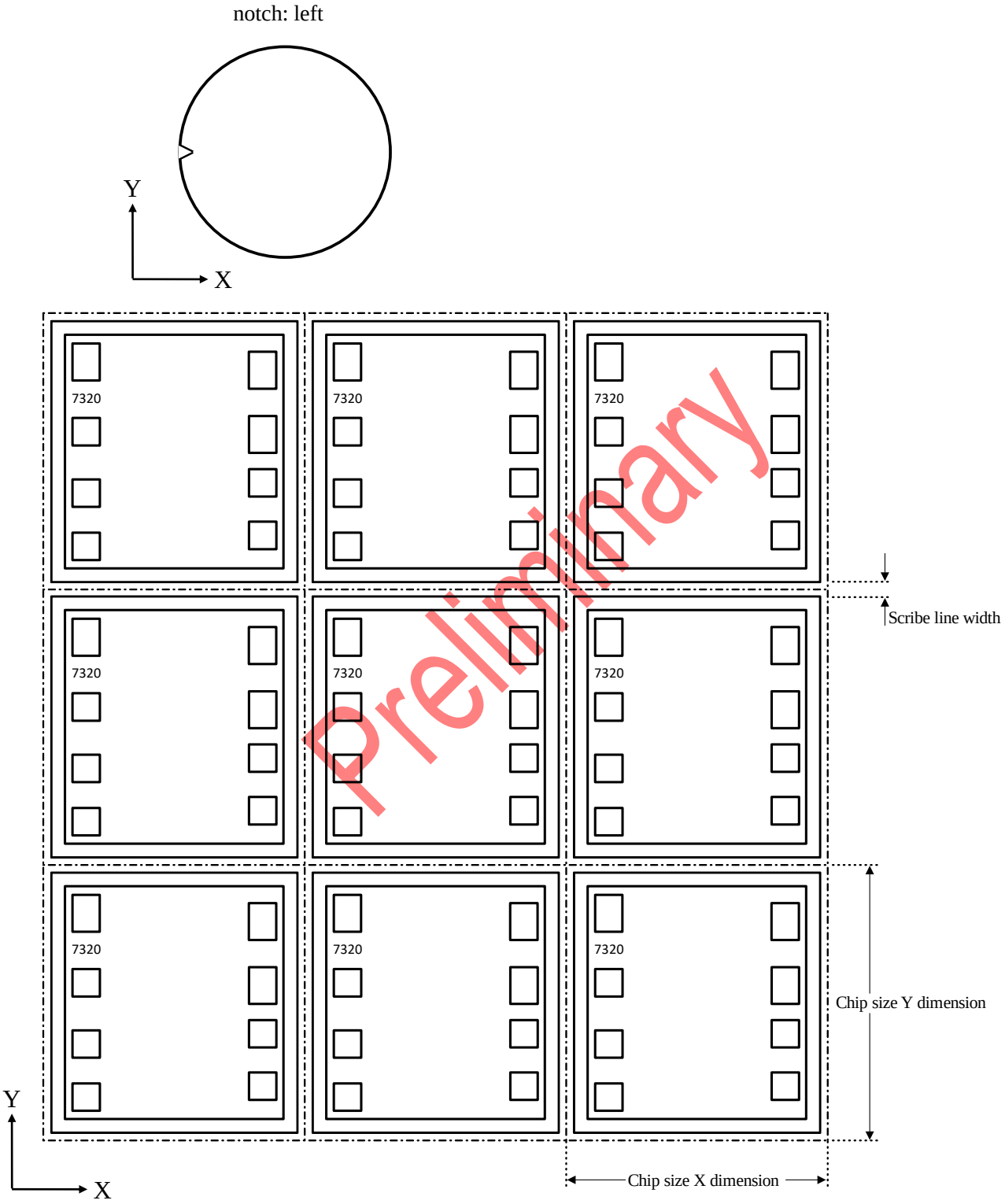
OE (pull-up resistance built-in)	Oscillator	Output stage
HIGH/Open	Operating	Operating
LOW	Operating	Disabled (Hi-Z)

14.2. Oscillator Startup Detection Function

An oscillator startup detection circuit is built-in. The circuit disables the OUT/OUTN outputs (high impedance) until the oscillator starts. This function prevents unstable oscillation and other problems, which can occur when power is applied, from appearing at the output.

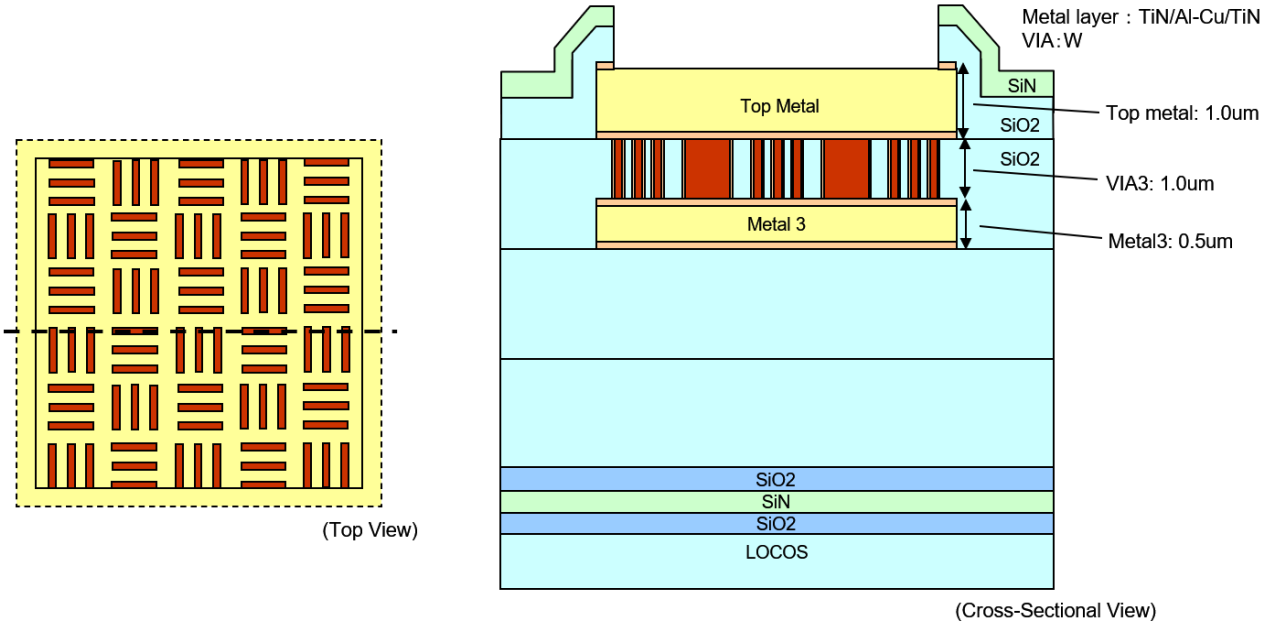
15. WAFER SURFACE ALIGNMENT DIAGRAM

Wafer size: 200mm±0.5mm
Scribe line width: 80µm



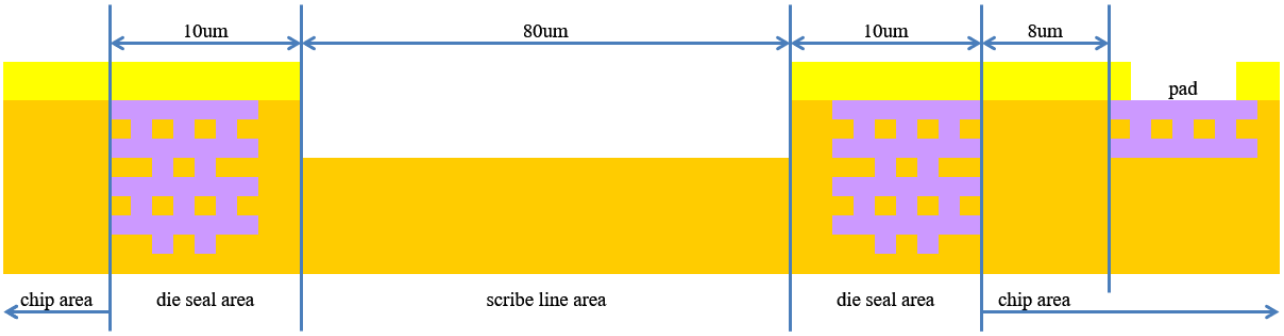
16. CROSS SECTION STRUCTURE

16.1. PAD Cross Section Structure



*Film thicknesses of mention is a value in the designs as above and is not the actual value in the chip.

16.2. Seal Ring And Scribe Line Cross Section Structure



*Film thicknesses of mention is a value in the designs as above and is not the actual value in the chip.

<Notes on UBM formation>

In UBM (Under Bump Metal) formation to the mounting pad electrode by electroless plating, UBM is similarly formed on the scribe line TEG and the metal exposed part of the accessory. So mask process covering the scribe line is required to prevent these effects.

17. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.
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In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

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