

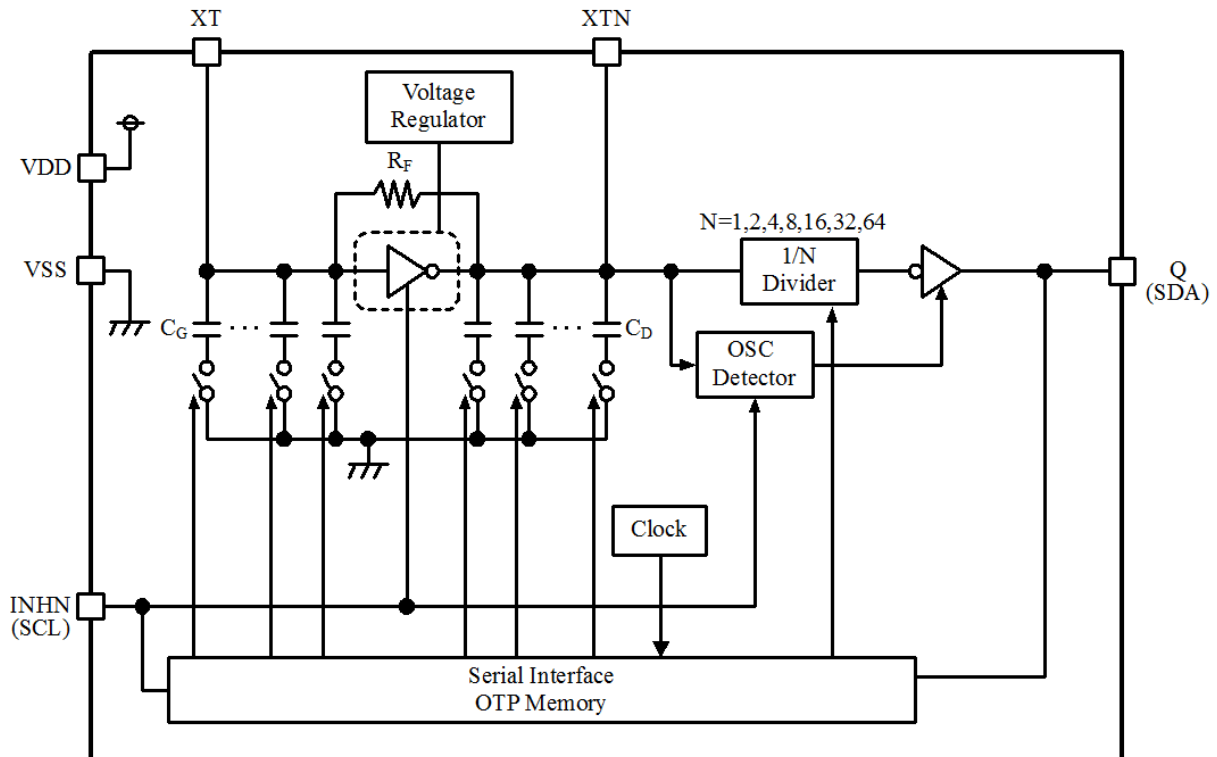
1. OVERVIEW

The CF7101Hx/WF7101Hx series are crystal oscillator module CMOS ICs with f0 adjustment function. It supports 16MHz to 100MHz fundamental-frequency and +125°C operation. The oscillator circuit stage has a voltage regulator drive, which reduces current consumption and frequency deviation due to fluctuations in the supply voltage. Even with an f0 adjustment function built in, the miniature chip size enables it to be implemented in a 1612 or 2016 size package.

2. FEATURES

- Operating supply voltage : 1.6V to 3.63V
- Recommended oscillation frequency (Fundamental-frequency) : 16MHz to 100MHz
- Output frequency : 0.25MHz to 100MHz
- Operating temperature : -40 to +125°C
- Chip size : X=0.6mm, Y=0.62mm
- Output level : CMOS
- Embedded memory : Nonvolatile memory (OTP: One Time Programmable)
- f0 adjustment function
 - Adjustment method : OTP Memory writing
 - Oscillator load capacitance (C_L) : 5pF
 - Frequency adjustment range : ±30ppm (min)
 - Frequency adjustment resolution : 1.5ppm/bit (max)
- Frequency division function
 - Setting method : OTP Memory writing
 - Selectable divider's ratio : 1/2, 1/4, 1/8, 1/16, 1/32, 1/64
- Phase noise characteristics (typ.)
 - f_{OSC}=40MHz, V_{DD}=3.3V : -87dBc/Hz@10Hz, -140dBc/Hz@1kHz, -157dBc/Hz@100kHz
 - (The ratings above are values obtained by measurements using NPC evaluation standard crystal element)
- Output 3-state function
- Low standby current (oscillator stopped, power saving pull-up resistor)
- Oscillation detection circuit built-in

3. BLOCK DIAGRAM

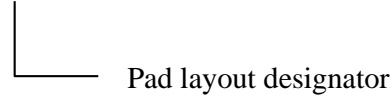


4. VERSION NAME CONVENTION

The version name comprises 1 alphanumeric characters [A-C].
The meaning of the character in each figure is:

- A : Flip Chip Bonding
- B : Wire Bonding Type I
- C : Wire Bonding Type II

7101Hx



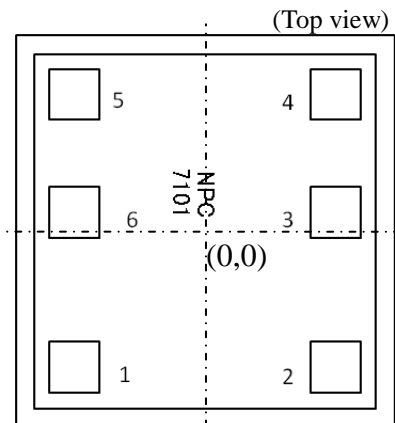
5. PAD DIMENSIONS

- (1) Chip size*¹ : X=0.60mm, Y=0.62mm
- (2) Rear surface : V_{SS} potential
- (3) Pad aperture size : 80μm×80μm
- (4) Chip form

*1: The chip size is the value measured between scribe line centers.

Pad Dimensions Unit:[μm]

No.	X	Y	Version name		
			7101HA	7101HB	7101HC
1	-206	-216	XT	XTN	XT
2	206	-216	XTN	XT	XTN
3	206	30	VDD	INH N	VSS
4	206	216	Q	VSS	Q
5	-206	216	VSS	Q	VDD
6	-206	30	INH N	VDD	INH N



6. PAD DESCRIPTION

Name	I/O	Function
XT	I	Crystal element connection pins. Connect crystal between XT and XTN pins.
XTN	O	
VDD	-	Supply voltage
Q (SDA)	O (I/O)	Oscillator output f _{osc} , f _{osc} /2, f _{osc} /4, f _{osc} /8, f _{osc} /16, f _{osc} /32, f _{osc} /64 frequency output. In program mode, SDA pin is the serial interface data input/output.
VSS	-	Ground
INH N (SCL)	I (I)	Output state control input (Inhibit) pin. Oscillator is stopped in standby mode when LOW. Pull-up resistor built-in. In program mode, SCL pin is the serial interface Clock input.

I: input pin, O: output pin, f_{osc}: oscillator frequency

7. ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Supply voltage range	V _{DD}	Voltage between VDD and VSS	-0.3 to +4.5	V	*1
Program input voltage range	V _{PP}	Voltage between INHN and VSS	-0.3 to +6.75	V	*1,*5
Input voltage range 1	V _{IN1}	INHN pin	-0.3 to V _{DD} +0.3	V	*1,*2,*5
Input voltage range 2	V _{IN2}	XT pin	-0.3 to +2.5	V	*1,*2
Output voltage range 1	V _{OUT1}	Q pin	-0.3 to V _{DD} +0.3	V	*1,*2,*5
Output voltage range 2	V _{OUT2}	XTN pin	-0.3 to +2.5	V	*1,*2
Output current	I _{OUT}	Q pin	±20	mA	*3
Junction temperature	T _j		150	°C	*3
Storage temperature range	T _{STG}	Chip form wafer form	-55 to +150	°C	*4

*1: Absolute maximum ratings are the values that must never be exceeded, even for a moment. This product may suffer breakdown if any one of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.

*2: V_{DD} is the V_{DD} value of recommended operating conditions.

*3: Do not exceed the absolute maximum ratings. If they are exceeded, device characteristics and reliability will be degraded.

*4: When stored alone in nitrogen or vacuum atmosphere.

*5: Refer to “10. RECOMMENDED OPERATING CONDITIONS (OTP MEMORY PROGRAMMING)” for OTP memory programming.

8. RECOMMENDED OPERATING CONDITIONS

Since it may influence the reliability if it is used out of the recommended operating conditions range, this product should be used within this range. Refer to “10. RECOMMENDED OPERATING CONDITIONS (OTP MEMORY PROGRAMMING)” for OTP memory programming.

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Oscillator frequency	f _{OSC}	V _{DD} =1.6 to 3.63V	16		100	MHz	*1
Output frequency	f _{OUT}	V _{DD} =1.6 to 3.63V	0.25		100	MHz	
Operating supply voltage	V _{DD}	Voltage between VDD and VSS	1.6		3.63	V	*2
Input voltage 1	V _{IN1}	INHN pin	V _{SS}		V _{DD}	V	
Input voltage 2	V _{IN2}	XT pin	V _{SS}		2.0	V	
Operating temperature	T _a		-40		+125	°C	
Output load capacitance	C _L	Q pin			15	pF	
OTP Memory data retention		T _a =-40 to 125°C	10			year	

*1: The oscillation frequency is a yardstick value and the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2: For stable operation of this product, mount a ceramic chip capacitor of 0.01μF or larger between VDD and VSS in close proximity to IC (within 3mm). Wiring pattern between IC and capacitor should be as thick as possible.

9. ELECTRICAL CHARACTERISTICS

9.1. DC Characteristics

9.1.1. Current consumption (f_{OSC}=40MHz)

V_{DD}=1.6 to 3.63V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Current consumption Fundamental (DSL Code=0H)	I _{DD} ^{*1}	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =40MHz	V _{DD} =1.8V		1.00	1.70	mA
			V _{DD} =2.5V		1.30	2.00	
			V _{DD} =3.3V		1.70	2.40	
Current consumption Divide-by-2 (DSL Code=1H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =20MHz	V _{DD} =1.8V		0.75	1.35	mA
			V _{DD} =2.5V		0.95	1.55	
			V _{DD} =3.3V		1.15	1.75	
Current consumption Divide-by-4 (DSL Code=2H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =10MHz	V _{DD} =1.8V		0.60	1.15	mA
			V _{DD} =2.5V		0.75	1.30	
			V _{DD} =3.3V		0.90	1.45	
Current consumption Divide-by-8 (DSL Code=3H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =5MHz	V _{DD} =1.8V		0.55	1.05	mA
			V _{DD} =2.5V		0.65	1.15	
			V _{DD} =3.3V		0.75	1.25	
Current consumption Divide-by-16 (DSL Code=4H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =2.5MHz	V _{DD} =1.8V		0.50	1.00	mA
			V _{DD} =2.5V		0.60	1.10	
			V _{DD} =3.3V		0.70	1.20	
Current consumption Divide-by-32 (DSL Code=5H)	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =1.25MHz	V _{DD} =1.8V		0.45	0.90	mA	
		V _{DD} =2.5V		0.55	1.00		
		V _{DD} =3.3V		0.65	1.10		
Current consumption Divide-by-64 (DSL Code=6H)	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =40MHz, f _{OUT} =0.625MHz	V _{DD} =1.8V		0.45	0.90	mA	
		V _{DD} =2.5V		0.50	0.95		
		V _{DD} =3.3V		0.60	1.05		

*1: The consumption current I_{DD}(C_{LOUT}) with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA] + C_{LOUT}[pF] \times V_{DD}[V] \times f_{OUT}[MHz] \times 10^{-3}$$

9.1.2. Current consumption (f_{OSC}=96MHz)

V_{DD}=1.6 to 3.63V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Current consumption Fundamental (DSL Code=0H)	I _{DD} ^{*1}	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =96MHz	V _{DD} =1.8V		2.00	2.70	mA
			V _{DD} =2.5V		2.65	3.35	
			V _{DD} =3.3V		3.50	4.20	
Current consumption Divide-by-2 (DSL Code=1H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =48MHz	V _{DD} =1.8V		1.30	1.90	mA
			V _{DD} =2.5V		1.70	2.30	
			V _{DD} =3.3V		2.20	2.80	
Current consumption Divide-by-4 (DSL Code=2H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =24MHz	V _{DD} =1.8V		1.00	1.55	mA
			V _{DD} =2.5V		1.25	1.80	
			V _{DD} =3.3V		1.55	2.10	
Current consumption Divide-by-8 (DSL Code=3H)		Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =12MHz	V _{DD} =1.8V		0.80	1.30	mA
			V _{DD} =2.5V		1.00	1.50	
			V _{DD} =3.3V		1.20	1.70	
Current consumption Divide-by-16 (DSL Code=4H)	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =6MHz	V _{DD} =1.8V		0.75	1.25	mA	
		V _{DD} =2.5V		0.90	1.40		
		V _{DD} =3.3V		1.05	1.55		
Current consumption Divide-by-32 (DSL Code=5H)	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =3MHz	V _{DD} =1.8V		0.70	1.15	mA	
		V _{DD} =2.5V		0.80	1.25		
		V _{DD} =3.3V		0.95	1.40		
Current consumption Divide-by-64 (DSL Code=6H)	Measurement circuit 1, INHN=OPEN, no load, f _{OSC} =96MHz, f _{OUT} =1.5MHz	V _{DD} =1.8V		0.70	1.15	mA	
		V _{DD} =2.5V		0.80	1.25		
		V _{DD} =3.3V		0.90	1.35		

*1: The consumption current I_{DD} (C_{LOUT}) with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA] + C_{LOUT}[pF] \times V_{DD}[V] \times f_{OUT}[MHz] \times 10^{-3}$$

9.1.3. Other DC characteristics

$V_{DD}=1.6$ to $3.63V$, $V_{SS}=0V$, $T_a=-40$ to $+125^{\circ}C$ unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
HIGH-level output voltage	V_{OH}	Q pin, Measurement circuit 2, $I_{OH}=-4mA$	V_{DD} -0.4		V_{DD}	V
		Q pin, Measurement circuit 2, $I_{OH}=-1mA$	$0.9V_{DD}$		V_{DD}	V
LOW-level output voltage	V_{OL}	Q pin, Measurement circuit 3, $I_{OL}=4mA$	0		0.4	V
		Q pin, Measurement circuit 3, $I_{OL}=1mA$	0		$0.1V_{DD}$	V
HIGH-level input voltage	V_{IH}	INH pin, Measurement circuit 4	$0.7V_{DD}$			V
LOW-level input voltage	V_{IL}	INH pin, Measurement circuit 4			$0.3V_{DD}$	V
Output leakage current	I_Z	Q pin, $INH=V_{SS}$ Measurement circuit 5	$Q=V_{DD}$		10	μA
			$Q=V_{SS}$	-10		
Standby current	I_{ST}	Measurement circuit 1, $INH=V_{SS}$			10	μA
pull-up resistance	R_{PU1}	INH pin, Measurement circuit 4	1	2	3	$M\Omega$
	R_{PU2}	INH pin, Measurement circuit 4	50	100	200	$k\Omega$
Oscillator feedback resistance	R_f	Measurement circuit 6	50	100	200	$k\Omega$

9.2. Oscillator Characteristics

V_{DD}=1.6 to 3.63V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillation start voltage	V _{STR}	V _{DD} slowly increasing, Measurement circuit 7			1.5	V
Frequency adjustment range	Δf/f	F0 Code : 00H(=60H) Center, T _a =25°C F0 Code range = 01H to FFH	±30			ppm
Frequency adjustment resolution	Δf _{Res}	F0 Code : 00H(=60H) Center, T _a =25°C Frequency fluctuation by 1 code unit in the Frequency adjustment range			1.5	ppm
Oscillator minimum load capacitance	C _{LMIN}	C _L minimum setting, T _a =25°C F0 Code = 01H, CLS Code = 0H		3.25		pF
Oscillator maximum load capacitance	C _{LMAX}	C _L maximum setting, T _a =25°C F0 Code = FFH, CLS Code = 3H		9.83		pF
Oscillator start time	t _{STA}	T _a =25°C, V _{DD} applied (rising edge: 0-90% of V _{DD}), V _{OH} and V _{OL} ratings nominal, Measurement circuit 7			2	ms

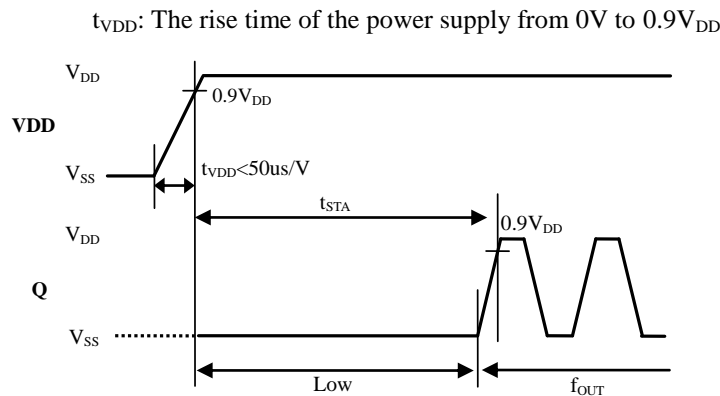
Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

The recommended crystal element characteristics are R1 ≤ 20Ω, C0 = 1.5pF and γ = 300.

Timing Diagrams



Oscillator start time

9.3. Clock Output Characteristics

$V_{DD}=1.6$ to $3.63V$, $V_{SS}=0V$, $T_a=-40$ to $+125^\circ C$ unless otherwise noted

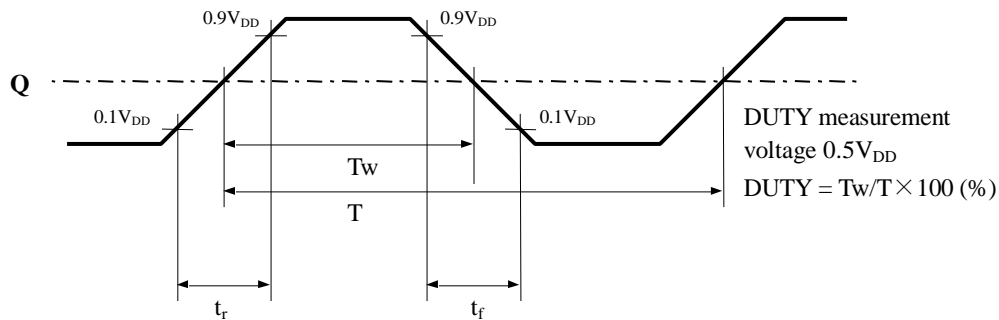
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Rise time	Tr	Q pin, Measurement circuit 1, $C_{LOUT}=15pF$, $0.1V_{DD} \rightarrow 0.9V_{DD}$	$V_{DD}=1.6$ to $2.25V$		1.8	5.0	ns
			$V_{DD}=2.25$ to $2.97V$		1.2	3.0	ns
			$V_{DD}=2.97$ to $3.63V$		0.9	2.5	ns
Fall time	Tf	Q pin, Measurement circuit 1, $C_{LOUT}=15pF$, $0.9V_{DD} \rightarrow 0.1V_{DD}$	$V_{DD}=1.6$ to $2.25V$		1.8	5.0	ns
			$V_{DD}=2.25$ to $2.97V$		1.2	3.0	ns
			$V_{DD}=2.97$ to $3.63V$		0.9	2.5	ns
Output duty cycle	DUTY	Q pin, Measurement circuit 1, $T_a=25^\circ C$, $C_{LOUT} \leq 15pF$	45	50	55	%	
Output enable delay time	t_{OE}	Q pin, Measurement circuit 7, design value, $T_a=25^\circ C$, $C_{LOUT} \leq 15pF$, INHN=Low→High			2	ms	
Output disable delay time	t_{OD}	Q pin, Measurement circuit 7, design value, $T_a=25^\circ C$, $C_{LOUT} \leq 15pF$, INHN=High→Low			200	ns	

Notes

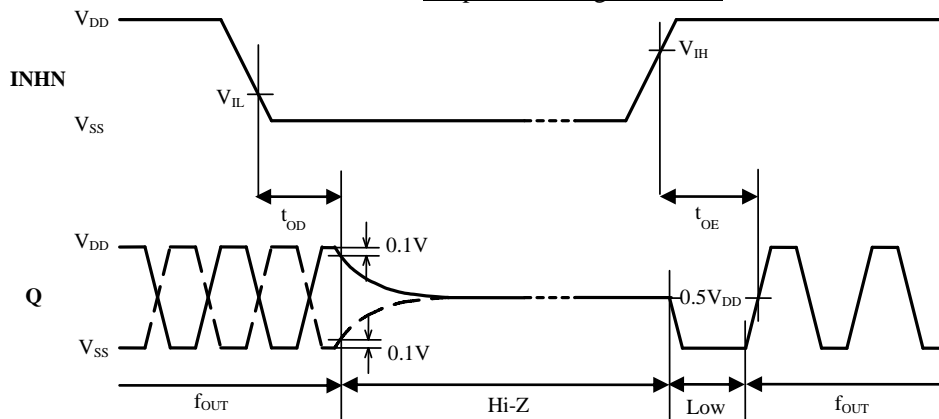
The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

Timing Diagrams



Outputs witching waveform



Output disable and enable timing

*When INHN goes HIGH to LOW, the Q output becomes high impedance.

*When INHN goes LOW to HIGH, the Q output goes LOW once and then becomes normal output operation after having detected oscillation signals.

10. RECOMMENDED OPERATING CONDITIONS (OTP MEMORY PROGRAMMING)

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Operating supply voltage	V _{DD}		3.0		3.63	V	*1
OTP memory programming supply voltage	V _{PP}	SCL(INHN) pin	6.25	6.5	6.75	V	
Operating temperature	T _a		0		+50	°C	

*1: For stable operation of this product, mount a ceramic chip capacitor of 0.01μF or larger between VDD and VSS in close proximity to IC (within 3mm). Wiring pattern between IC and capacitor should be as thick as possible.

11. ELECTRICAL CHARACTERISTICS (OTP MEMORY PROGRAMMING)

11.1. DC Characteristics (2-wire type serial interface)

V_{PP}=6.25 to 6.75V, V_{DD}=3.0 to 3.63V, V_{SS}=0V, T_a=0 to +50°C unless otherwise noted

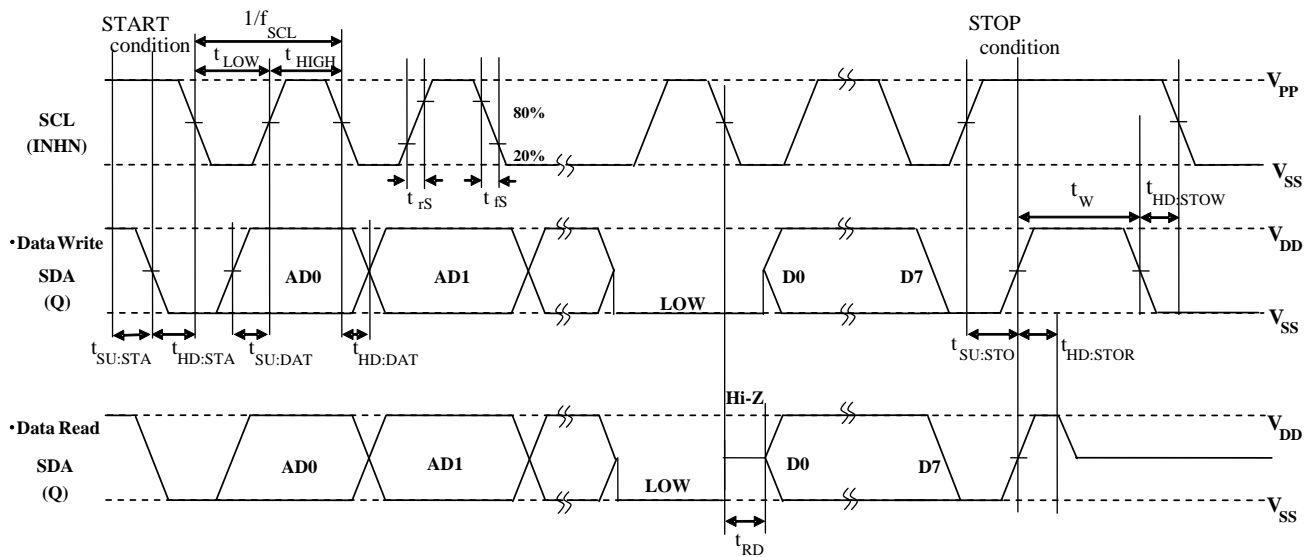
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL(INHN) pin HIGH-level input voltage	V _{IHC}	SCL(INHN) pin	V _{DD} +1.7V			V
SCL(INHN) pin LOW-level input voltage	V _{ILC}	SCL(INHN) pin			0.3V _{DD}	V
SDA(Q) pin HIGH-level input voltage	V _{IHD}	SDA(Q) pin	0.7V _{DD}			V
SDA(Q) pin LOW-level input voltage	V _{ILD}	SDA(Q) pin			0.3V _{DD}	V
SDA(Q) pin HIGH-level output voltage	V _{OHD}	SDA(Q) pin, I _{OHD} =-0.1mA	V _{DD} -0.4V		V _{DD}	V
SDA(Q) pin LOW-level output voltage	V _{OLD}	SDA(Q) pin, I _{OLD} =0.1mA	0		0.4	V

11.2. AC Characteristics (2-wire serial interface)

$V_{PP}=6.25$ to $6.75V$, $V_{DD}=3.0$ to $3.63V$, $V_{SS}=0V$, $T_a=0$ to $+50^\circ C$ unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL clock frequency	f_{SCL}	After program start condition	25		500	kHz
Start condition setup time	$t_{SU:STA}$		0.3			μs
Start condition hold time	$t_{HD:STA}$		0.3			μs
Data setup time	$t_{SU:DAT}$		0.3			μs
Data hold time	$t_{HD:DAT}$		0.3			μs
Stop condition setup time	$t_{SU:STO}$		0.3			μs
Stop condition hold time	$t_{SU:STOW}$	Write the data to OTP memory	0.3			μs
	$t_{HD:STOR}$	Read the data to OTP memory Access the registers	0.2			μs
OTP memory write time	t_w		150	200	250	μs
SCL LOW-period	t_{LOW}		1			μs
SCL HIGH-period	t_{HIGH}		1			μs
SCL rise time	t_{rS}	20% \rightarrow 80%			0.2	μs
SCL fall time	t_{fS}	80% \rightarrow 20%			0.2	μs
Read data delay time	t_{RD}	$C_{LOUT}=15pF$			0.5	μs

Timing Diagrams



Serial interface timing diagrams

12. FUNCTIONAL DESCRIPTION

12.1. INHN Function

The INHN pin switches the IC between normal operating/standby mode and serial interface mode, depending on the input voltage.

When INHN is left open-circuit or tied to HIGH level, the IC is in normal operating mode.

When INHN is tied to LOW level, the IC enters standby mode. The Q output becomes high-impedance and the oscillator circuit stops.

When the INHN pin voltage is between V_{IHC} and V_{PP} (4.7V[min] ~ 6.75V[max]), the device enters serial interface mode. For more information about serial interface mode, see sections 12.4 and 12.5.

INHN pin	Q pin	Oscillator	Mode
HIGH or Open	f_{OUT}	Operating	Normal operating mode
LOW	Hi-Z	Stopped	Standby mode
$V_{IHC} \leq V_{PP}(SCL)$	SDA	Operating	Serial interface mode

12.2. Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), and the internal circuit of INHN becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

12.3. Oscillation Detection Function and Power ON Reset Function

The 7101 series have an oscillation detection circuit.

The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation during initial power up and when started again using INHN.

When oscillation is detected, the serial interface internal circuits are initialized and the data written to OTP memory is read out.

12.4. OTP (One Time Programmable) Memory Function and Register Function

12.4.1. OTP Memory, Register Map

The 7101 series has a 4-bit address used to access the OTP memory or register.

Users can use addresses 0H to 5H and FH. Addresses 6H to EH are used for NPC device testing. Accessing addresses 6H to EH is prohibited to prevent unstable operation.

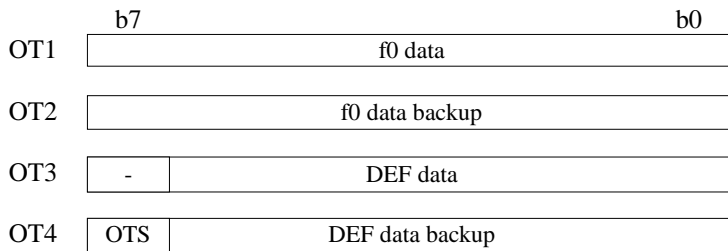
During normal operation, f0 adjustment data and internal settings data in OTP memory are loaded after oscillation detection. You use settings data by writing to the OTP memory.

Backup memory is used when you want to change data written in memory to other data. Data in backup memory side is enabled by writing “1” to the OTS bit of address 3H (OT4).

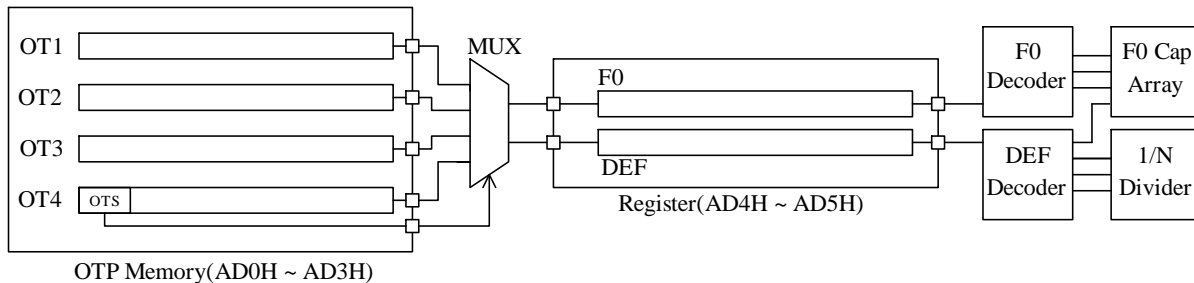
You can check the f0 adjustment and various settings using the register before data is written to the OTP memory.

Address	Memory	Function	Symbol	R/W	Initial value
0H	OTP	f0 adjustment memory	OT1	R/W	0H
1H		f0 adjustment memory backup	OT2	R/W	0H
2H		Internal setting memory	OT3	R/W	0H
3H		Internal setting memory backup	OT4	R/W	0H
4H	Register	f0 adjustment register	F0	W	Don't care
5H		Internal setting register	DEF	R/W	0H
6H-EH	Unusable (for IC testing)				
FH	Register	OTP Memory Test Register	PTM	W	0H

12.4.2. OTP Memory (Address: 0H to 3H)

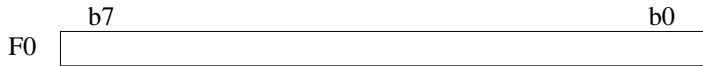


When the OTS bit is 0, OT1 and OT3 data is output. When the OTS bit is 1, the backup data is selected, and OT2 and OT4 data is output.



Block diagram of the OTP memory and register

12.4.3. f0 Adjustment Register F0 (Address: 4H)



The F0 register is directly linked to the capacitor array connected to the XT and XTN terminals of the oscillator. It supports 255 gradations of adjustment, from 01H (minimum oscillator load capacitance code) to FFH (maximum oscillator load capacitance code). The F0 register is set to the F0 [7:0]=60H when the F0 [7:0]=00H setting. This setting is in the OTP memory initial value 00H, is intended to be in the CL = 5pF. Refer to the following table for code settings (design values).

Bit	Function		Capacitance (pF)	
	“ON”	“OFF”	XT	XTN
b0	1	0	0.04	0.04
b1	1	0	0.08	0.08
b2	1	0	0.16	0.16
b3	1	0	0.32	0.32
b4	1	0	0.64	0.64
b5	1	0	1.28	1.28
b6	1	0	2.56	2.56
b7	1	0	5.12	5.12

C_L: Load capacitance setting *1

Dec.	Hex.	Code								Capacitance array		C _L (pF)
		b7	b6	b5	b4	b3	b2	b1	b0	XT (pF)	XTN (pF)	
0	00	0	1	1	0	0	0	0	0	3.84	3.84	5.15
1	01	0	0	0	0	0	0	0	1	0.04	0.04	3.25
2	02	0	0	0	0	0	0	1	0	0.08	0.08	3.27
3	03	0	0	0	0	0	0	1	1	0.12	0.12	3.29
4	04	0	0	0	0	0	1	0	0	0.16	0.16	3.31
⋮												
88	58	0	1	0	1	1	0	0	0	3.52	3.52	4.99
89	59	0	1	0	1	1	0	0	1	3.56	3.56	5.01
90	5A	0	1	0	1	1	0	1	0	3.60	3.60	5.03
91	5B	0	1	0	1	1	0	1	1	3.64	3.64	5.05
92	5C	0	1	0	1	1	1	0	0	3.68	3.68	5.07
93	5D	0	1	0	1	1	1	0	1	3.72	3.72	5.09
94	5E	0	1	0	1	1	1	1	0	3.76	3.76	5.11
95	5F	0	1	0	1	1	1	1	0	3.80	3.80	5.13
96	60	0	1	1	0	0	0	0	0	3.84	3.84	5.15
97	61	0	1	1	0	0	0	0	1	3.88	3.88	5.17
⋮												
252	FC	1	1	1	1	1	0	1	1	10.08	10.08	8.27
253	FD	1	1	1	1	1	1	0	0	10.12	10.12	8.29
254	FE	1	1	1	1	1	1	1	0	10.16	10.16	8.31
255	FF	1	1	1	1	1	1	1	1	10.20	10.20	8.33

*1: Settings when CLS adjustment code is 0H.

12.4.4. Internal Settings Register DEF (Address: 5H)

	b7	b5	b4	b3	b2	b0
DEF	Unusable		CLS		DSL	

The DEF register is an internal settings register. It can switch the internal state, such as switching the frequency division factor. If you change the DEF register, in order to confirm that the state has changed, writes to f0 adjustment register without exiting the serial interface mode. Along with the f0 adjustment register set value, it outputs the oscillation frequency of the modified internal state. Bits 5-7 are for NPC device testing. When writing, write data 0 to this register.

Divider select bits DSL[2:0]

The DSL bits switch the frequency division conditions. The DSL[2:0]=7H setting is for NPC device testing. Its use is prohibited to prevent unstable operation.

Output frequency	DSL[2:0]
f0 output	0H
f0/2 output	1H
f0/4 output	2H
f0/8 output	3H
f0/16 output	4H
f0/32 output	5H
f0/64 output	6H
Unusable	7H

CL offset adjustment bits CLS[1:0]

The CLS bits switch the oscillator load capacitance offset adjustment value (design values). When the code 00H of f0 adjustment register has been set, CLS will be invalid.

CL set value	CLS[1:0]
CL	0H
CL+0.5pF	1H
CL+1.0pF	2H
CL+1.5pF	3H

12.4.5. OTP Memory Test Register PTM (Address: FH)

	b7	b2	b1	b0
PTM	-			PTM[1:0]

The PTM bits switch the read condition to confirm strength of writing in OTP memory. Margin-1 Read Mode provides a read condition to confirm state of strength of writing in OTP memory. The OTP Memory Test Register is set to the Margin-1 Read Mode when the PTM[1:0]=3H setting. After writing the 3H in PTM, lead the Memory without exiting the serial interface mode. If you can correctly read the codes that you wrote in OTP memory, the strength of writing in OTP memory is guaranteed.

PTM[1:0]	Mode
0H	User Mode (Normal Mode)
3H	Margin-1 Read Mode

12.4.6. The factory setting for the IC

The following table shows the settings of the IC function in memory initial value.

Function	State
Use memory	Main memory(Initial) Selectable memory: Main memory or Backup memory
f0 adjustment capacitor array	$C_L=5.15\text{pF}$ (Initial) Selectable CL capacitance value range: 3.25pF ~ 9.83pF
frequency division conditions	Fundamental (Initial) Selectable division setting: Fundamental, $f_{\text{OSC}}/2$, $f_{\text{OSC}}/4$, $f_{\text{OSC}}/8$, $f_{\text{OSC}}/16$, $f_{\text{OSC}}/32$, $f_{\text{OSC}}/64$

12.5. 2-Wire Serial Interface

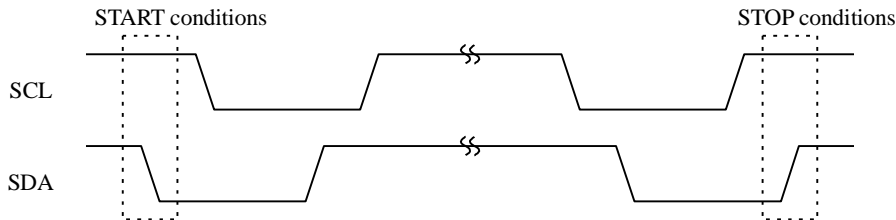
12.5.1. Serial Interface Start Condition

Oscillation detection is required to initialize the serial interface internal circuits. Start the serial interface when the oscillation startup time (t_{STA}) has elapsed after power is applied. When the device is disabled using INHN pin control (INHN = LOW), start the serial interface when the enable delay time (t_{OE}) has elapsed after setting INHN open circuit or HIGH level. This start condition also applies when restarting after the serial interface is stopped.

12.5.2. Programming Start/Stop Conditions

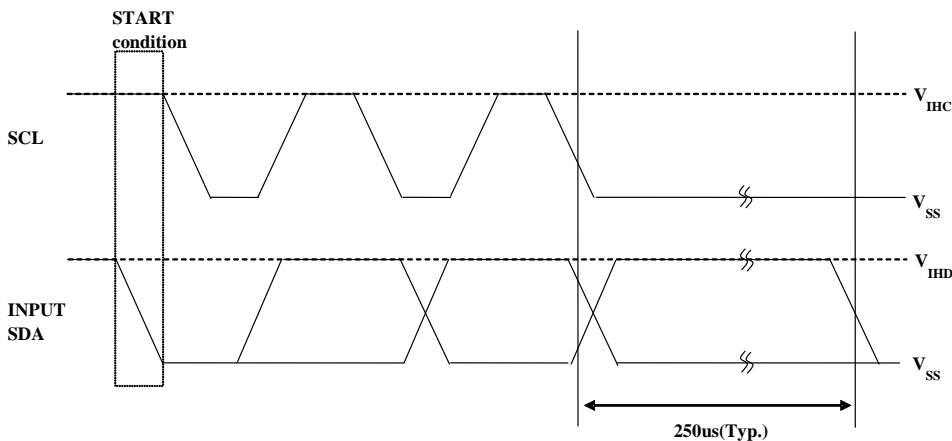
Data is sent and received using a 2-wire serial interface comprising SCL (INHN clock line) and SDA (Q data line).

Hold SCL and SDA both HIGH level when the serial interface is not transferring data. Device access starts when SDA goes from HIGH to LOW with SCL held HIGH (START condition), and then data can be transferred. Conversely, device access ends when SDA goes from LOW to HIGH with SCL held HIGH (STOP condition). These conditions can be accepted during data transfer, so data transfer should always start with the START condition and end with the STOP condition. See section 12.5.3 for details about the data transfer format.



Programming start/stop condition waveform

When a voltage V_{IHC} is applied to SCL, the output from the Q pin is disabled, and the device is in communication state. If the SCL clock is LOW level for 250 us (Typ.) or longer during communications state (*), the interface is initialized and communication ends.



*:When SCL isn't change from L state to H state for 250us(Typ.), the interface will be initialized automatically

Reset timer operation

12.5.3. Register and OTP Memory Data Transfer Format

The register and OTP memory data transfer formats are described below. Data is always transferred with LSB first.

Data Write Format

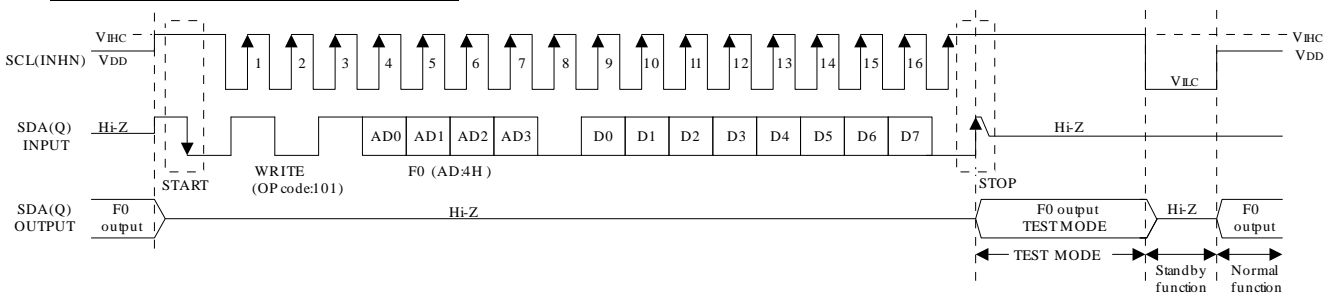
The transmitting device sends the START condition and 8-bit data comprising the write operation code (101), address, followed by a LOW-level 8th bit. Followed by 8-bit data, 16-bit transfers in total, and then send the STOP condition.

When writing data to the register, data is written into the register in sync with the 16th rising edge on SCL.

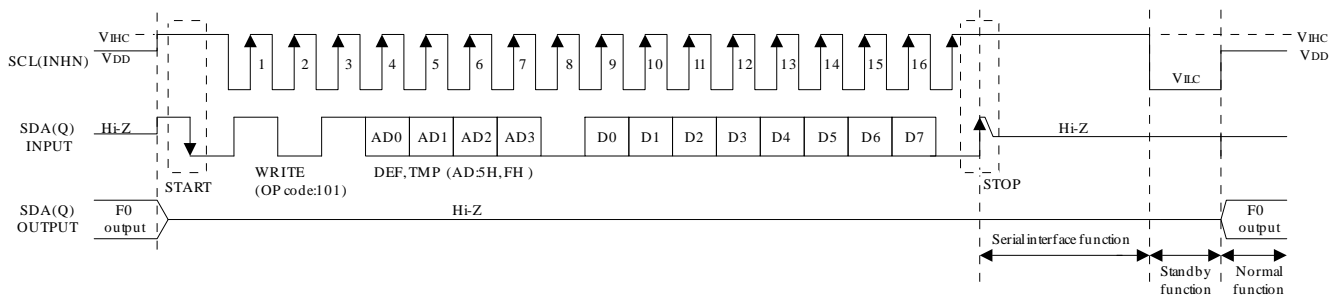
When writing to OTP memory, specify the OTP memory address and send the data and STOP condition. After sending the STOP condition, maintain the write state (SCL=V_{PP}, SDA=V_{IHD}) during the OTP memory write time (t_w). Once the OTP memory write time has elapsed, set SDA to LOW level (V_{ILD}).

To end serial communication and return to normal operation, set SCL to LOW level (V_{ILC}) after the STOP condition, and set SDA open circuit (Hi-Z).

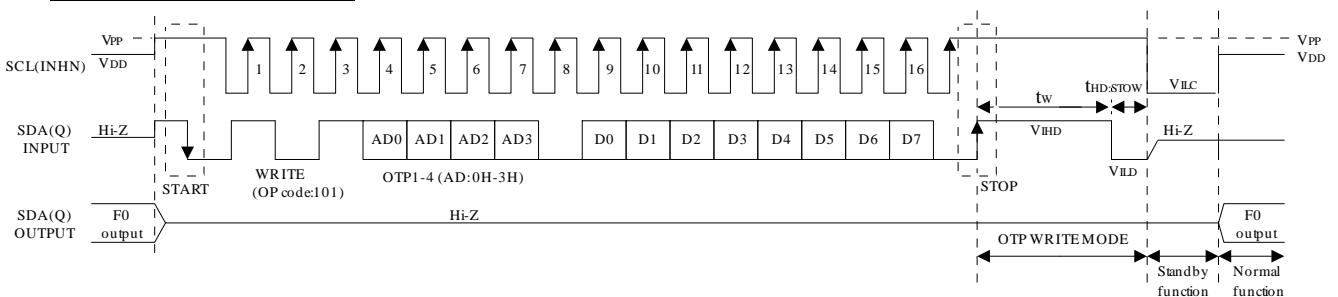
Register write timing (Address: 4H)



Register write timing (Address: 5H or FH)

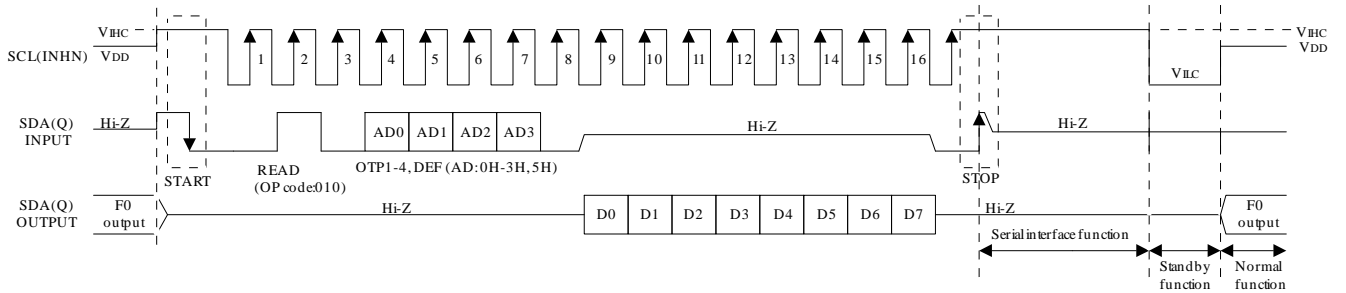


OTP Memory write timing



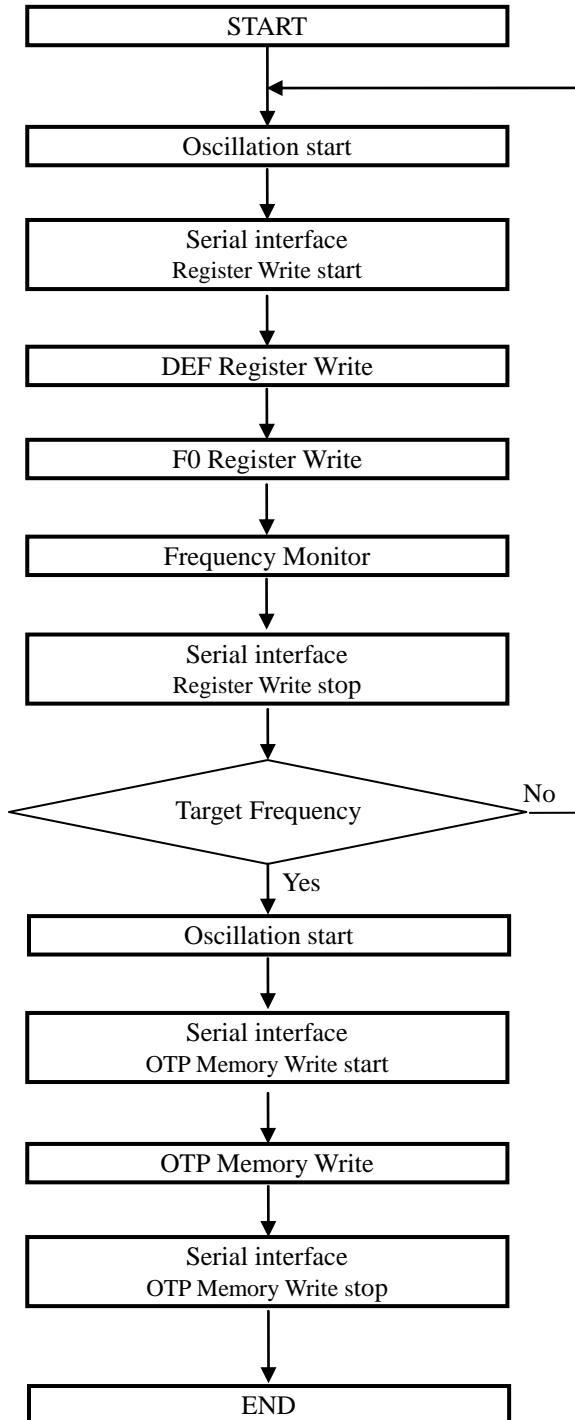
Data Read Format

When reading from OTP memory, the transmitter sends the START condition and 7-bit data comprising the read operation code (010) and address, followed by a LOW-level 8th bit. SDA goes open circuit (Hi-Z) on the SCL falling edge after 8 bits have been sent, and then data is output from SDA in sync with the SCL falling edge. The procedure for returning to normal operation is the same as that described in section 12.5.3.1.



12.5.4. f0 Adjustment Flow Chart

The following adjustment flow is an example. The flow will vary depending on the required frequency precision, manufacturing process, and adjustment environment. This example does not show DSL or CLS setting.



When adjusting the frequency using the register, start the interface when the oscillation startup time (t_{STA}) or enable delay time (t_{OE}) has elapsed after applying the START condition (see section 12.5.1).

After the interface starts, write data to the register. After writing to the DEF register (after sending the STOP condition), you can continue and write to the F0 register by sending the START condition.

After writing to the F0 register (after sending the STOP condition), monitor the frequency on the Q output.

After the serial interface stops, check whether the target frequency is achieved, and readjust as necessary.

When writing to OTP memory, start the interface when the oscillation startup time (t_{STA}) has elapsed after sending the START condition (see section 12.5.1).

After the interface starts, write the adjustment code obtained by the register write.

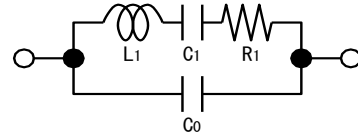
After writing to OTP memory (after sending the STOP condition), monitor the frequency on the Q output or read the OTP memory to check the written data, as necessary.

13. REFERENCE DATA (7101 TYPICAL CHARACTERISTICS)

The following characteristics are measured using the crystal below.
Note that the characteristics will vary with the crystal used.

Crystal used for measurement

Parameter	40MHz	80MHz	100MHz
C0(pF)	1.5	2.4	2.1
R1(Ω)	27.5	6.3	8.1

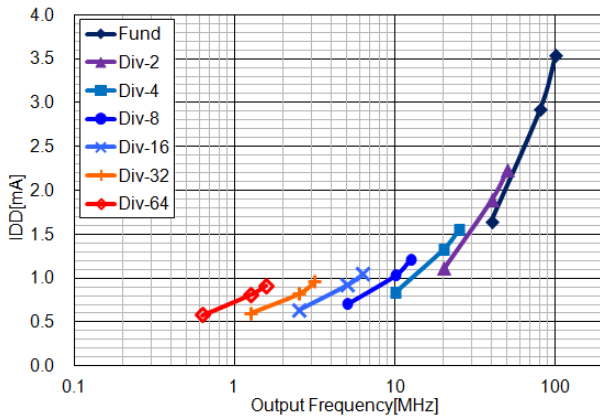


Crystal parameters

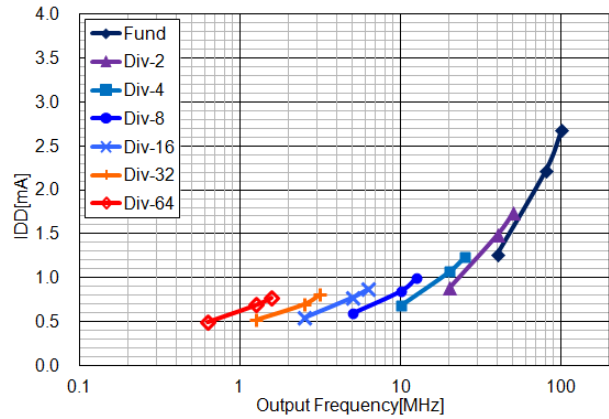
13.1. Current Consumption

[Measurement condition] Ta=25°C, no load, F0Code=00H

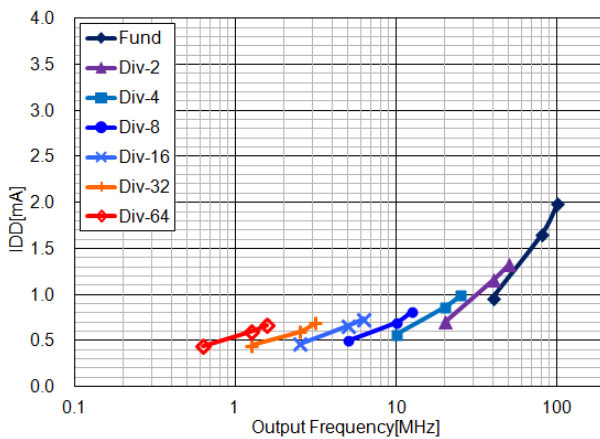
■ V_{DD}=3.3V



■ V_{DD}=2.5V

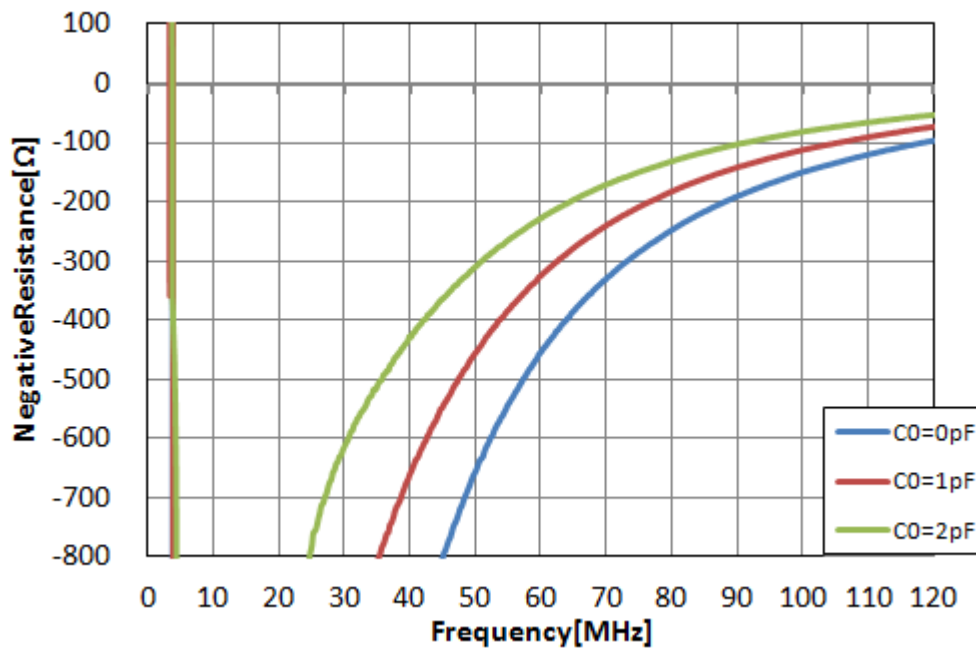


■ V_{DD}=1.8V



13.2. Negative resistance

[Measurement condition] $V_{DD}=3.3V$, $T_a=25^{\circ}C$, Measurement circuit 8

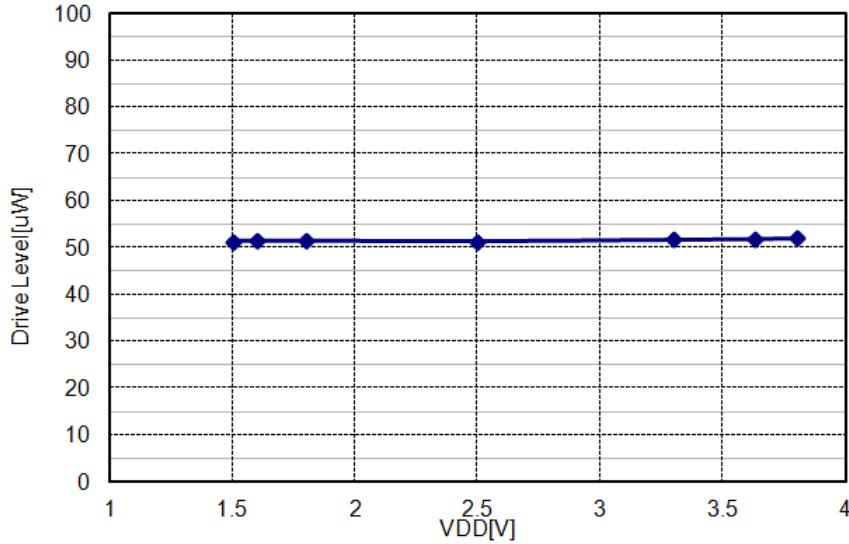


The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XT and XTN pins. They were performed with Agilent 4396B using the NPC test jig. They may vary in a measurement jig, and measurement environment.

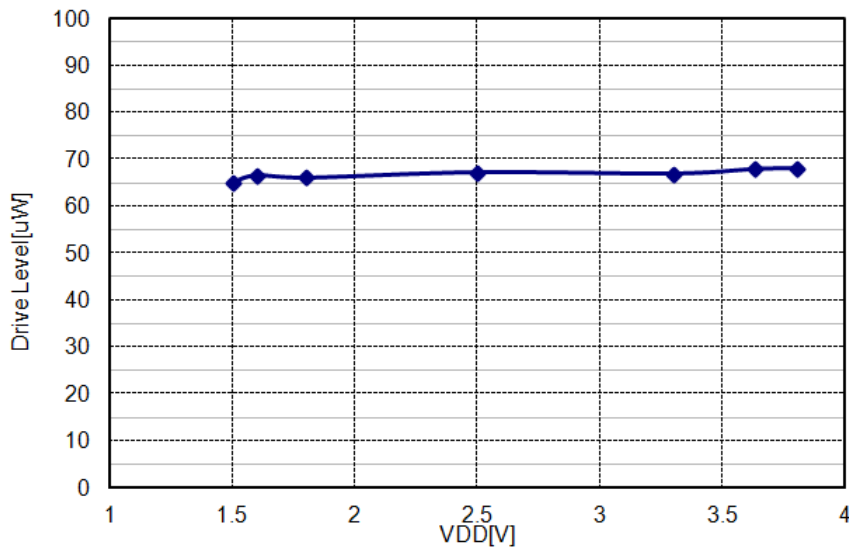
13.3. Drive Level

[Measurement condition] Ta=25°C, F0Code=00H, Measurement circuit 9

■ f_{osc}=40MHz



■ f_{osc}=100MHz



$$DL = (I_{X'tal})^2 \times Re$$

I_{X'tal} : Current though Crystal(RMS)

Re : Crystal's effective resistance

Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

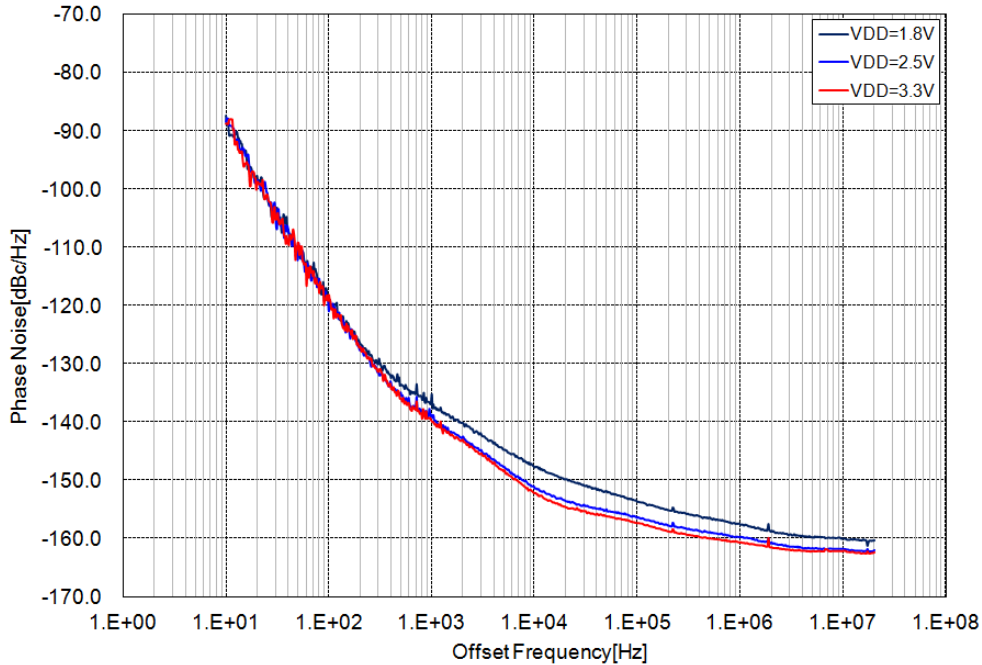
Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

13.4. Phase Noise

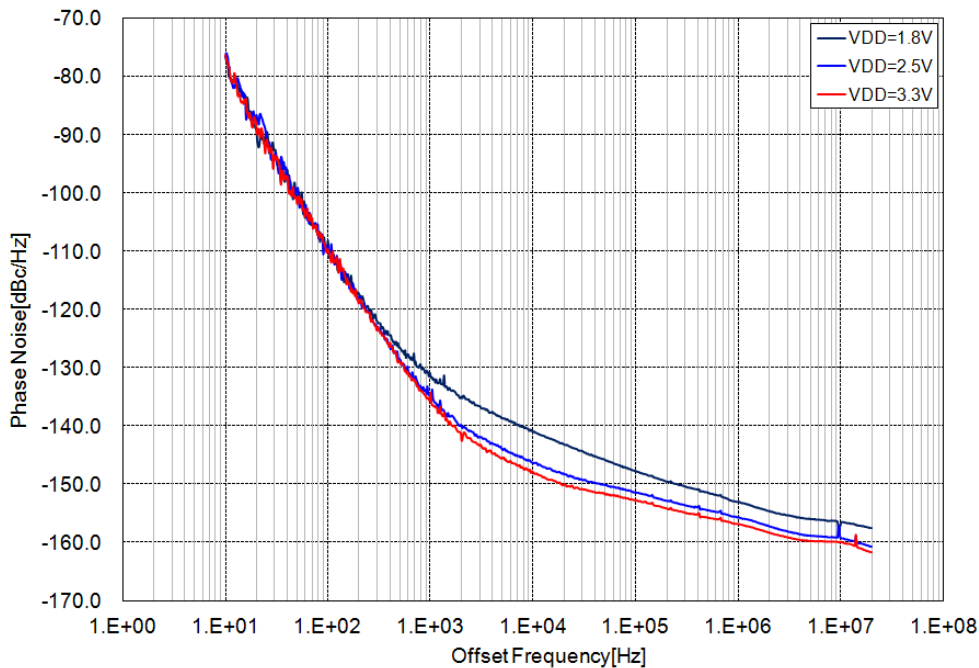
[Measurement condition] Ta=25°C

[Measurement equipment] Signal Source Analyzer Agilent E5052B

■ f_{OUT}=40MHz, F0Code=00H, DEFCODE=00H



■ f_{OUT}=100MHz, F0Code=00H, DEFCODE=00H



Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

13.5. Output Waveform

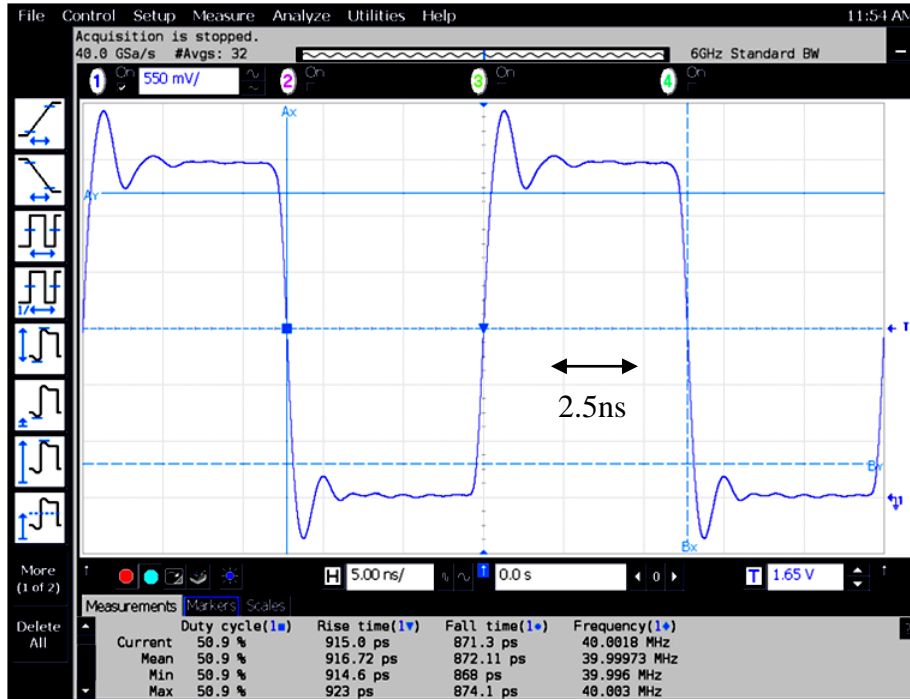
[Measurement condition] V_{DD}=3.3V, T_a=25°C, C_L=15pF, Measurement circuit 1

[Measurement equipment] Oscilloscope Agilent DSO80604B, Differential probe 1134A (Probe head E2678A)

■ f_{OUT}=40MHz, F0Code=00H, DEFCODE=00H



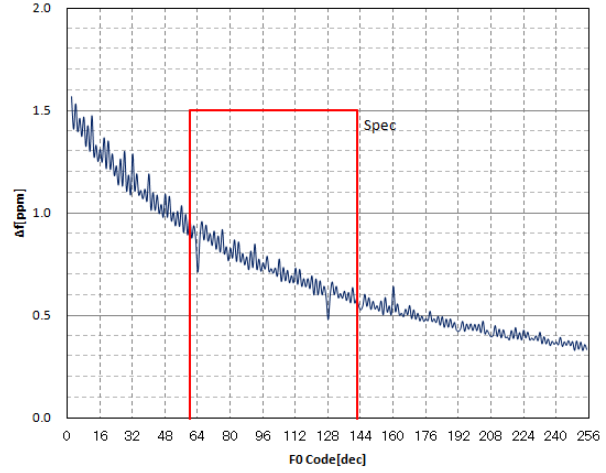
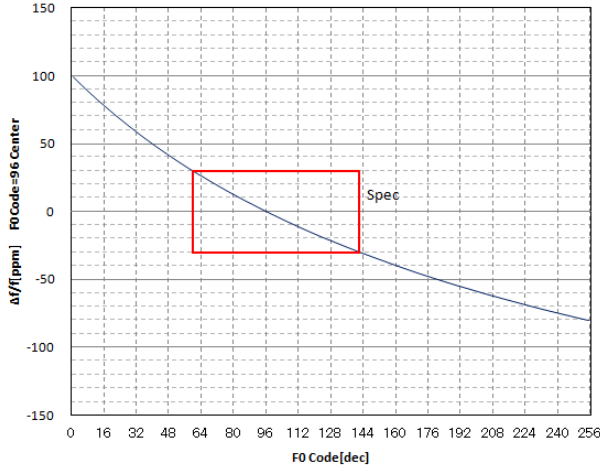
■ f_{OUT}=100MHz, F0Code=00H, DEFCODE=00H



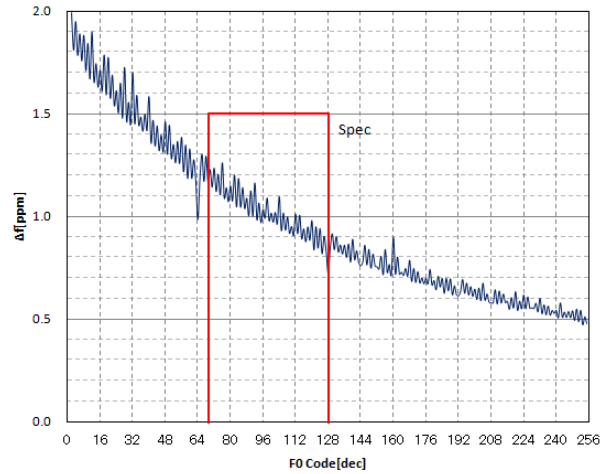
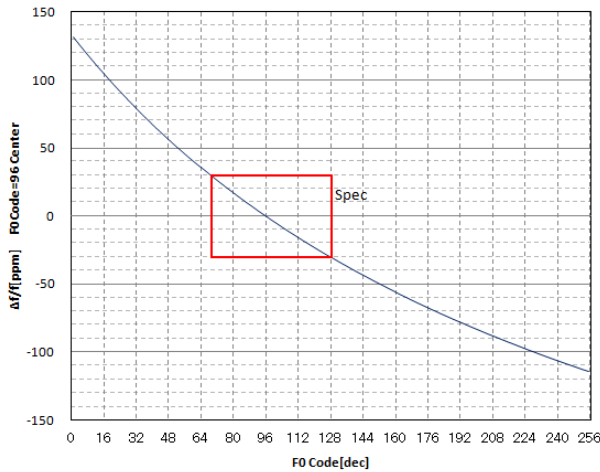
13.6. f0 Adjustment

[Measurement condition] $V_{DD}=3.3V, T_a=25^{\circ}C$

■ $f_{OUT}=40MHz, DEFCODE=00H$



■ $f_{OUT}=100MHz, DEFCODE=00H$



Notes

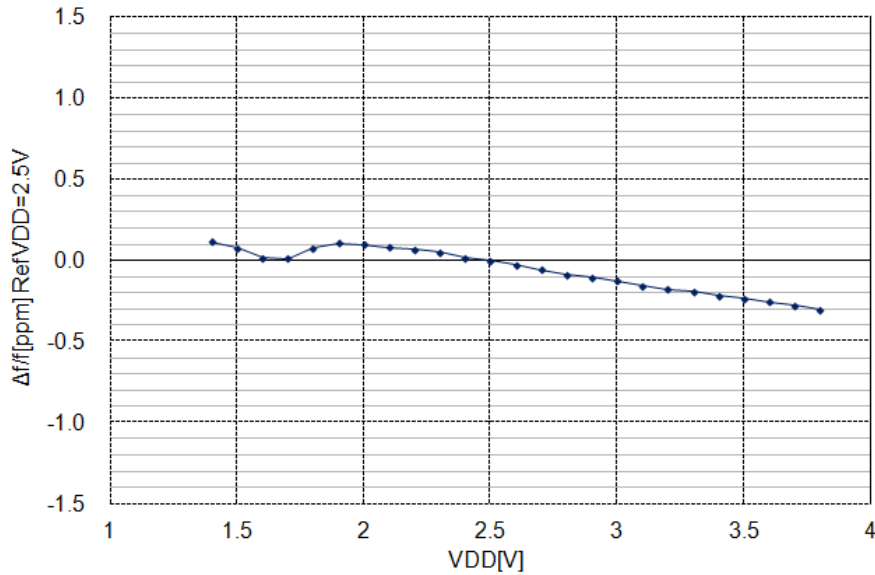
The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

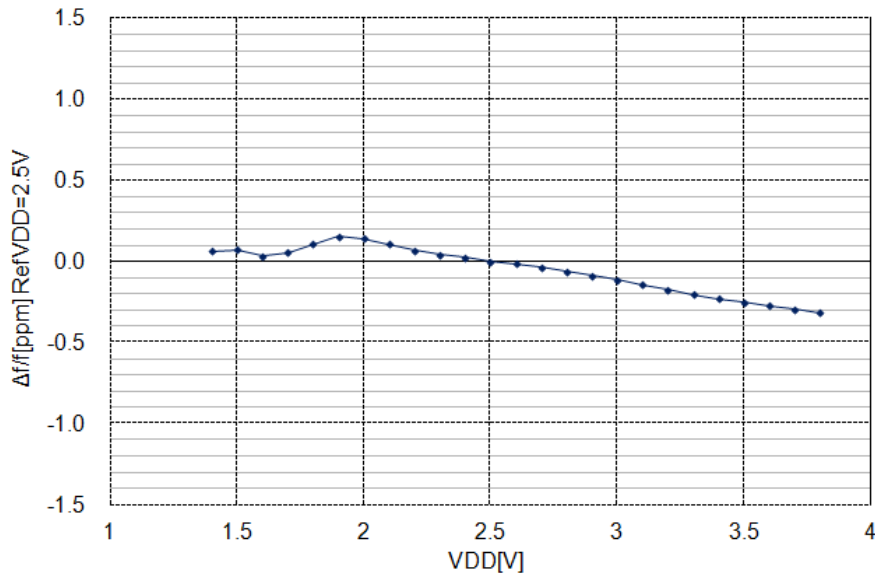
13.7. Frequency Deviation with Voltage

[Measurement condition] Ta=25°C

■ f_{osc}=40MHz, F0Code=00H, DEFCODE=00H



■ f_{osc}=100MHz, F0Code=00H, DEFCODE=00H



Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

14. MEASUREMENT CIRCUITS

These measurement circuits are used for the evaluation of the electrical and switching characteristics.

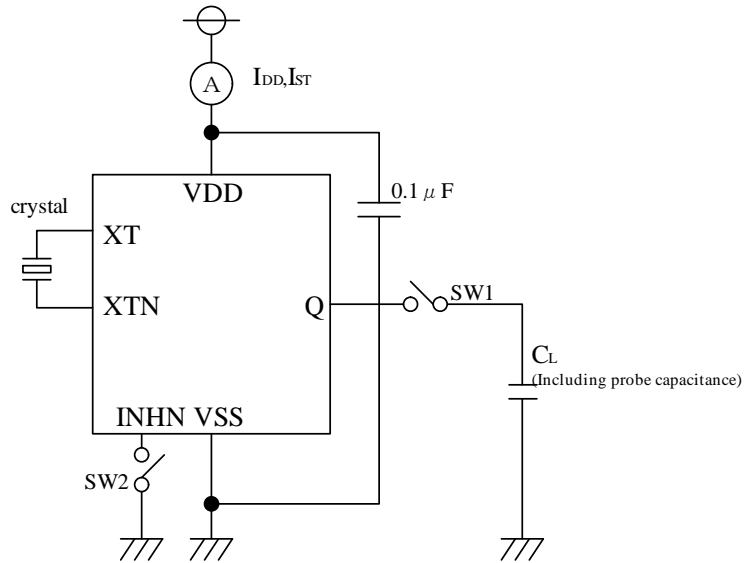
Notes

Connect the bypass capacitors, specified in the measurement circuits, VDD/-VSS.

Connect the bypass capacitors and load resistors with wiring pattern as short as possible (less than 3mm length).

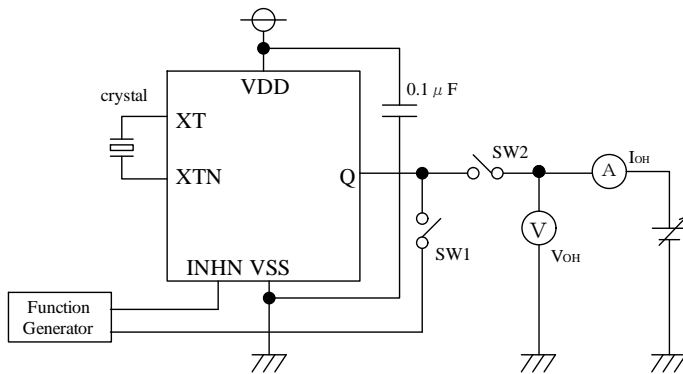
If the wiring pattern is too long, the desired characteristics cannot be obtained.

14.1. Measurement Circuit 1 I_{DD} , I_{ST} , DUTY, t_r , t_f



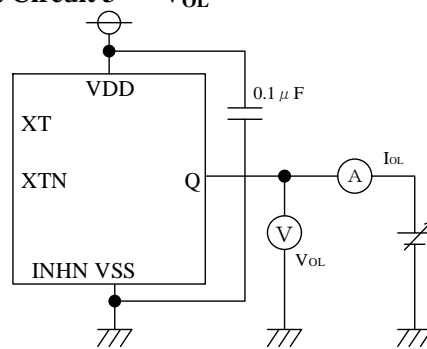
Measurement item	SW1	SW2
I_{DD}	OFF	OFF
I_{ST}	ON or OFF	ON
DUTY, t_r , t_f	ON	OFF

14.2. Measurement Circuit 2 V_{OH}

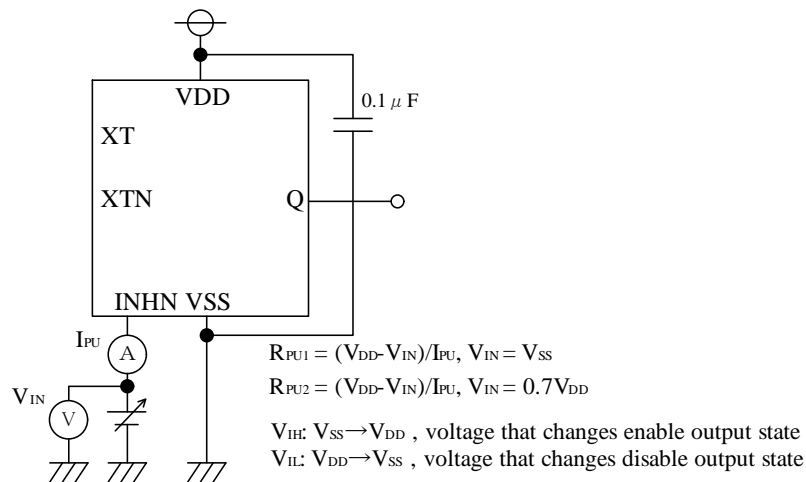


Step1: [SW1=ON, SW2=OFF] SIFMode AD=4H Write Data=07H
 Step2: [SW1=OFF, SW2=ON] V_{OH} Measure

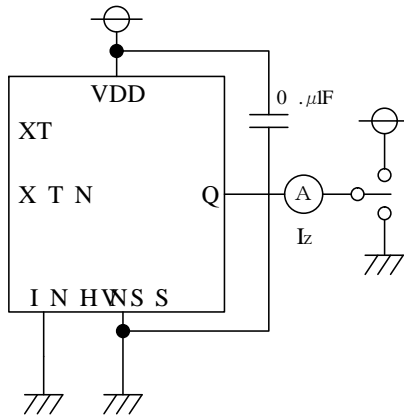
14.3. Measurement Circuit 3 V_{OL}



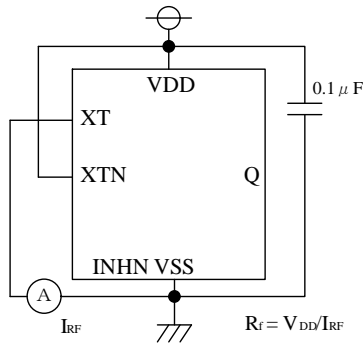
14.4. Measurement Circuit 4 R_{PU1} , R_{PU2} , V_{IH} , V_{IL}



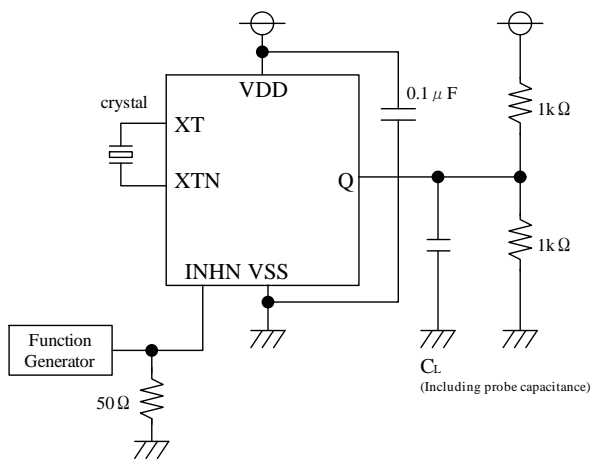
14.5. Measurement Circuit 5 I_z



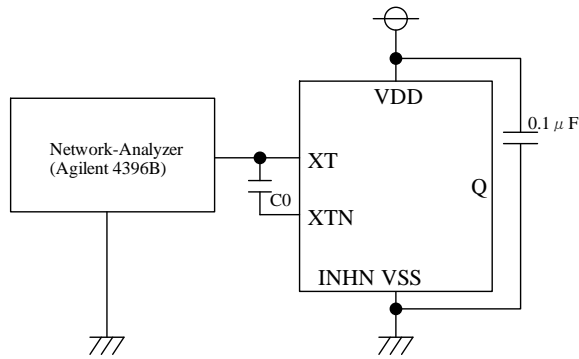
14.6. Measurement Circuit 6 R_f



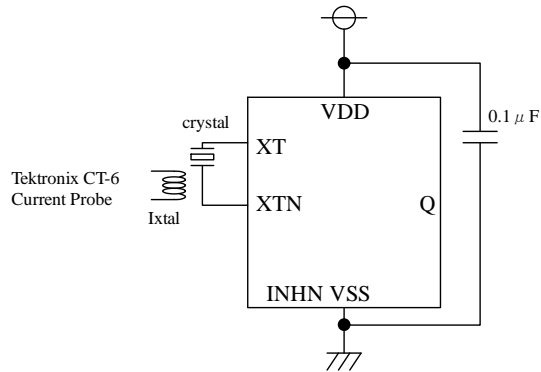
14.7. Measurement Circuit 7 V_{STR} , V_{STO} , t_{STA} , t_{OE} , t_{OD}



14.8. Measurement Circuit 8 NR



14.9. Measurement Circuit 9 DL

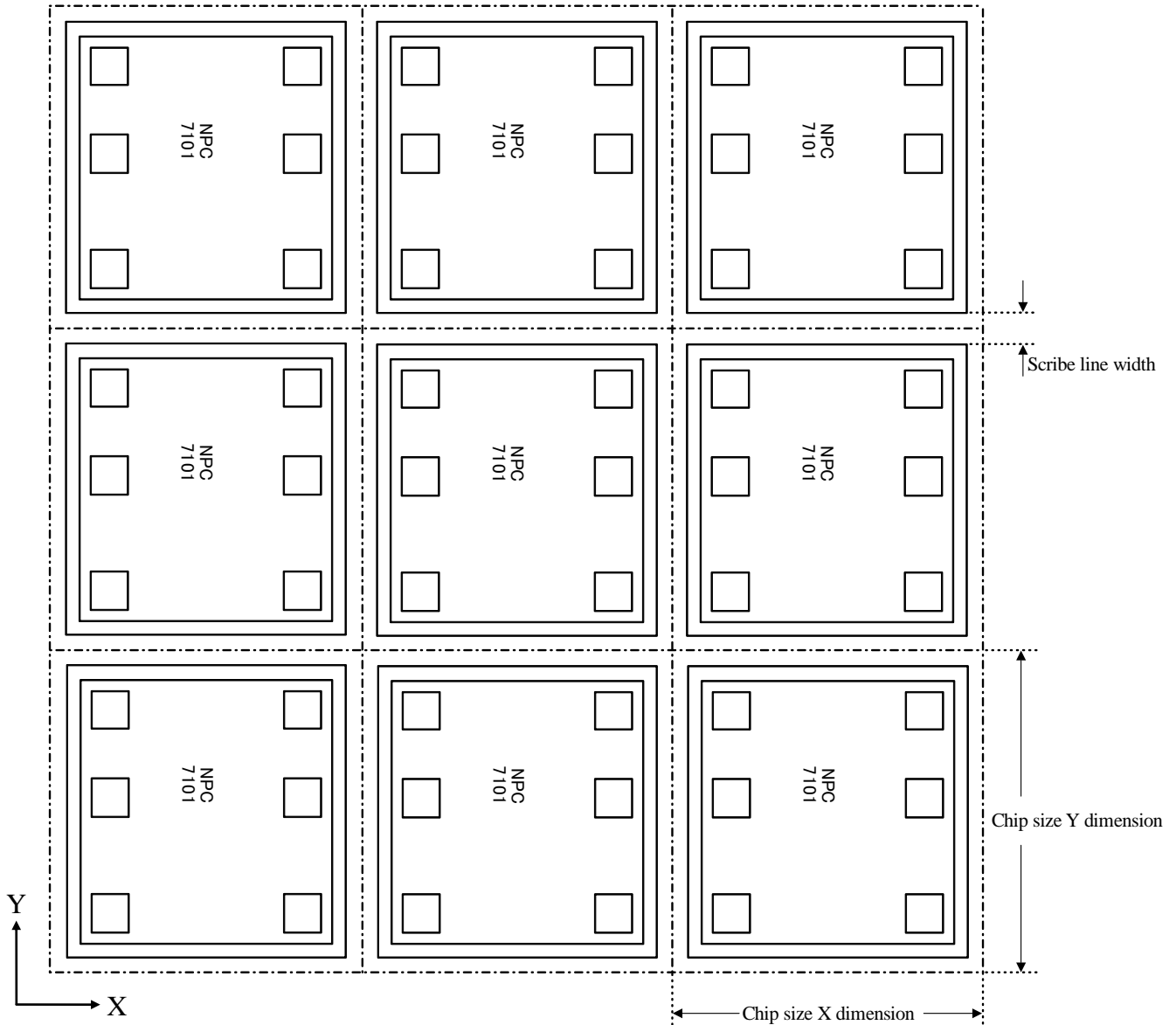
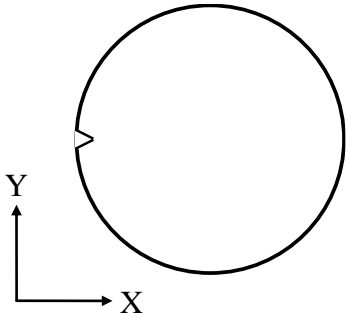


15. WAFER SURFACE ALIGNMENT DIAGRAM

Wafer size: 200mm ± 0.5mm

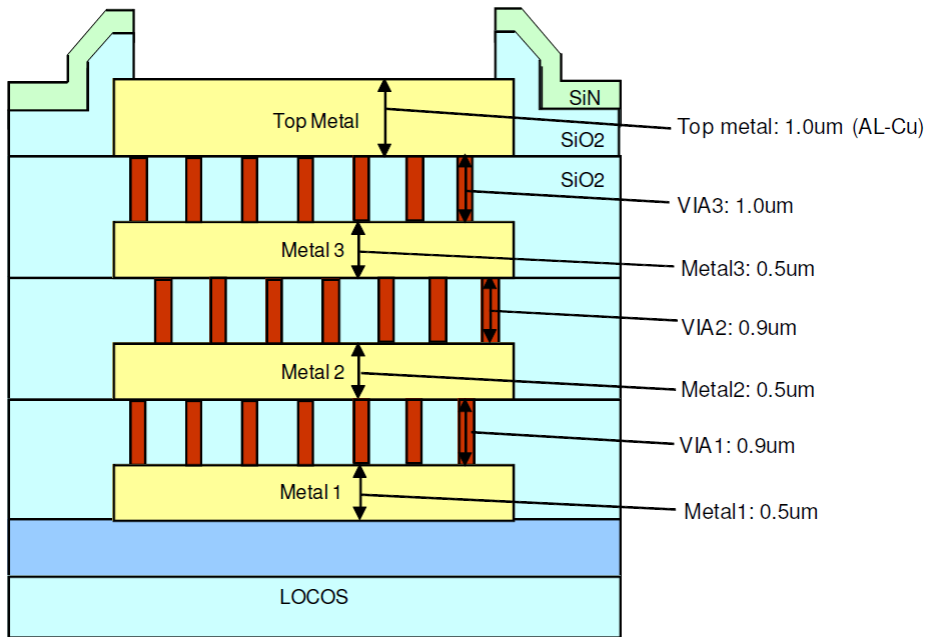
Scribe line width: 60µm

notch: left



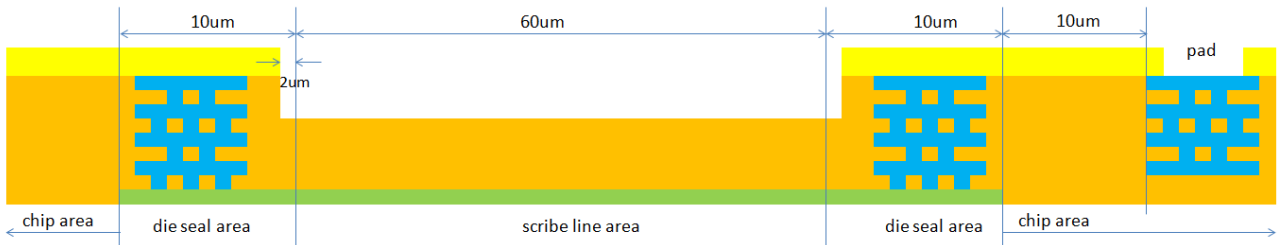
16. CROSS SECTION STRUCTURE

16.1. PAD Cross Section Structure



*Film thicknesses of mention is a value in the designs as above and is not the actual value in the chip.

16.2. Seal Ring and Scribe Line Cross Section Structure



*Widths of mention is a value in the designs as above and is not the actual value in the chip.

<Notes on UBM formation>

In UBM (Under Bump Metal) formation to the mounting pad electrode by electroless plating, UBM is similarly formed on the scribe line TEG and the metal exposed part of the accessory. So mask process covering the scribe line is required to prevent these effects.

17. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.

If you wish to use this product in equipment requiring extremely high level of reliability, please contact our sales department or representative in advance.

In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

Please pay your attention to the following points at time of using the products shown in this document.

1. The products shown in this document (hereinafter "Products") are designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools and measurement equipment. The Products are not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment. The Products are not designed and manufactured to be used for the apparatus that exerts harmful influence on the human lives due to the defects, failure or malfunction of the Products.
If you wish to use the Products in that apparatus, please contact our sales section in advance.
In the event that the Products are used in such apparatus without our prior approval, we assume no responsibility whatsoever for any damages resulting from the use of that apparatus.
2. NPC reserves the right to change the specifications of the Products in order to improve the characteristics or reliability thereof.
3. The information described in this document is presented only as a guide for using the Products. No responsibility is assumed by us for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of the third parties. Then, we assume no responsibility whatsoever for any damages resulting from that infringements.
4. The constant of each circuit shown in this document is described as an example, and it is not guaranteed about its value of the mass production products.
5. In the case of that the Products in this document falls under the foreign exchange and foreign trade control law or other applicable laws and regulations, approval of the export to be based on those laws and regulations are necessary. Customers are requested appropriately take steps to obtain required permissions or approvals from appropriate government agencies.



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DE170392E 2020.09