1. OVERVIEW

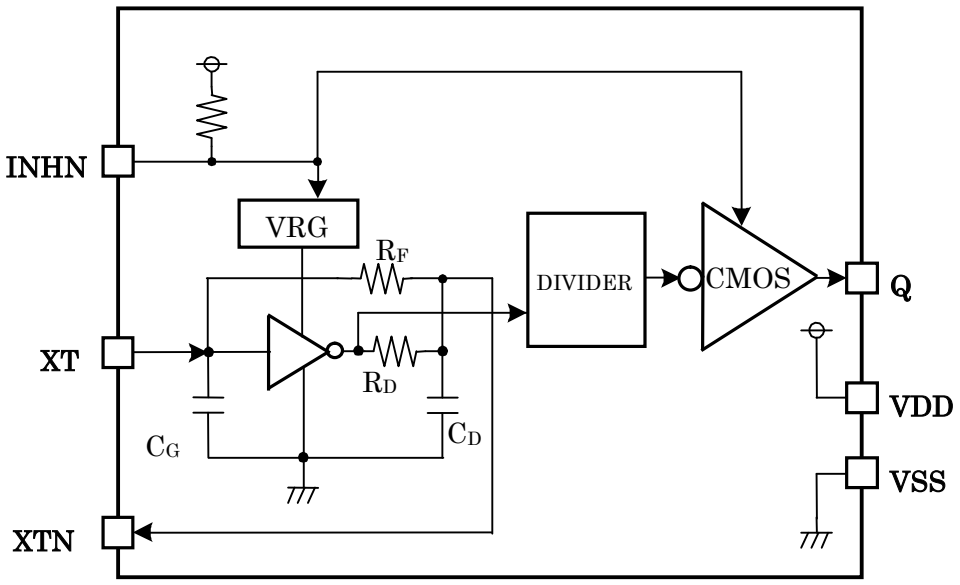
The CF7052Hxx/WF7052Hxx series are crystal oscillator module CMOS ICs for +125°C operation. They support 20MHz to 80MHz fundamental-frequency, and have an oscillator amplifier, voltage regulator circuit and output buffer.

The oscillator circuit stage has a voltage regulator drive, reducing current consumption and frequency deviation due to fluctuations in supply voltage.

2. FEATURES

- Operating supply voltage: 1.60V to 3.63V
- Recommended oscillation frequency (Fundamental-frequency): 20MHz to 60MHz (Hx1 to Hx5 ver.)
  40MHz to 80MHz (HxP ver.)
- Low current consumption by regulated voltage circuit drive in oscillator circuit stage:
  1.6mA typ. @ Hx1 ver. f_{OSC}=48MHz, V_{DD}=3.3V, no load
  2.3mA typ. @ HxP ver. f_{OSC}=80MHz, V_{DD}=3.3V, no load
- Operation temperature: -40 to +125°C
- Oscillator capacitors C_G, C_D built-in
- Output drive capability: ±4mA
- Output frequency: fosc (oscillator frequency), fosc/2, fosc/4, fosc/8, fosc/16
- Output 3-state function
- Low standby current (oscillator stopped, power saving pull-up resistor)
- Oscillation detection circuit built-in

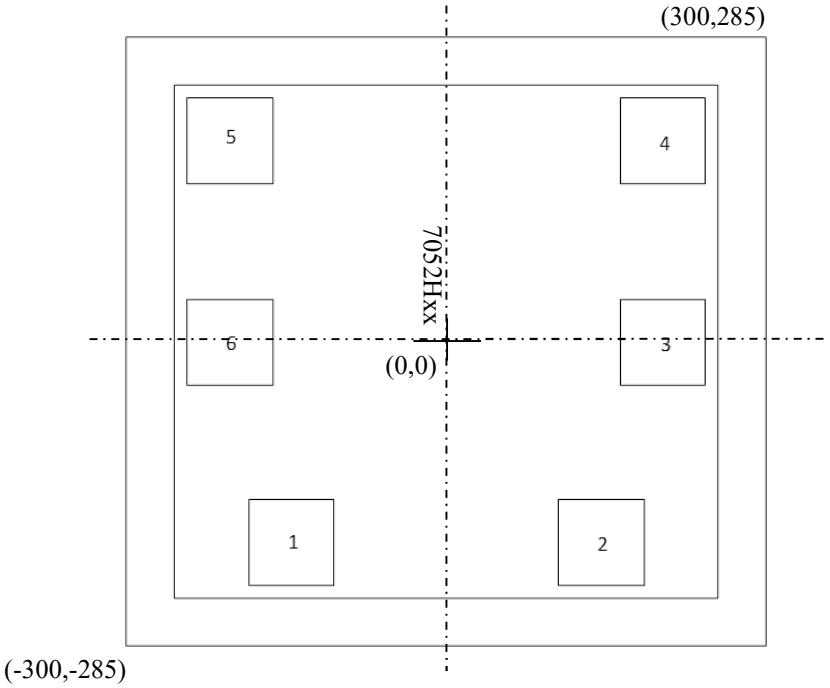
3. BLOCK DIAGRAM



4. PAD DIMENSIONS

(1) Chip size*1: X=0.60mm, Y=0.57mm
(2) Rear surface: V_{SS} potential
(3) Pad aperture size: 80um×80um
(4) Chip form

*1: The chip size is the value measured between scribe line centers.



Pad Dimensions Unit [μm]

No.	X	Y	Version name column 2		
			A	B	C
1	-145.2	-188.0	**XT**	**XTN**	**XT**
2	145.2	-188.0	**XTN**	**XT**	**XTN**
3	203.0	-0.6	**VDD**	**INHN**	**VSS**
4	203.0	188.0	**Q**	**VSS**	**Q**
5	-203.0	188.0	**VSS**	**Q**	**VDD**
6	-203.0	-0.6	**INHN**	**VDD**	**INHN**

5. PAD DESCRIPTION

Symbol	I/O	Name	Description
XT	I	Oscillator input pin	・Crystal element connection pins ・Connect crystal between XT and XTN pins.
XTN	O	Oscillator output pin	
VDD	-	(+) supply pin	
Q	O	Output pin	・fosc, fosc/2, fosc/4, fosc/8, fosc/16 frequency output ・High-impedance output in standby mode
VSS	-	(-) supply pin	
INHN	I	Output state control input (Inhibit) pin	・Oscillator is stopped in standby mode when LOW. ・Pull-up resistor built-in

I : input pin, O : output pin, f_{OSC} : oscillator frequency

6. 7052Hxx SERIES CONFIGURATION

Version name *1	Oscillator frequency (Reference value) *2	Oscillator capacitance (pF) *3		Output stage			Standby state	
		C_G	C_D	Output duty level	Frequency	Output current	Oscillator stopped	Output
7052Hx1	Fundamental-frequency oscillation: 20MHz to 60MHz	3.5	5.5	$1/2V_{DD}$	f_{OSC}	±4mA	Yes	Hi-Z
7052Hx2					f_{OSC} /2			
7052Hx3					f_{OSC} /4			
7052Hx4					f_{OSC} /8			
7052Hx5					f_{OSC} /16			
7052HxP	Fundamental-frequency oscillation: 40MHz to 80MHz	1.0	2.0		f_{OSC}			

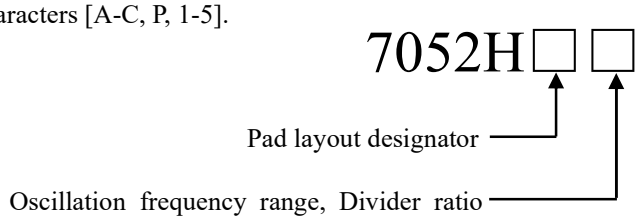
*1: Wafer form devices have designation WF7052Hxx and chip form devices have designation CF7052Hxx

*2: The recommended oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. The oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*3: Excluding parasitic capacitance

6.1. Version Name Format

The version name comprises 2 alphanumeric characters [A-C, P, 1-5].
The meaning of the character in each figure is:



(1) Pad layout designator
- A :Flip Chip Bonding
- B :Wire Bonding Type I
- C :Wire Bonding Type II

(2) Oscillation frequency range, Divider ratio
- 1 :20MHz to 60MHz, f_{OSC} output
- 2 :20MHz to 60MHz, f_{OSC} /2 output
- 3 :20MHz to 60MHz, f_{OSC} /4 output
- 4 :20MHz to 60MHz, f_{OSC} /8 output
- 5 :20MHz to 60MHz, f_{OSC} /16 output
- P :40MHz to 80MHz, f_{OSC} output

7. ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Supply voltage range	V_{DD}	Voltage between VDD and VSS	-0.3 to +4.5	V	*1
Input voltage range 1	V_{IN1}	INHN pin	-0.3 to V_{DD}+0.3	V	*1,*2
Input voltage range 2	V_{IN2}	XT pin	-0.3 ~ +2.5	V	*1,*2
Output voltage range 1	V_{OUT1}	Output pin	-0.3 to V_{DD}+0.3	V	*1,*2
Output voltage range 2	V_{OUT2}	XTN pin	-0.3 ~ +2.5	V	*1,*2
Output current	I_{OUT}	Q output	±20	mA	*3
Junction temperature	T_j		150	°C	*3
Storage temperature range	T_{STG}	Chip form wafer form	-55 to +150	°C	*4

*1: Absolute maximum ratings are the values that must never exceed even for a moment. This product may suffer breakdown if any one of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.
*2: V_{DD} is a V_{DD} value of recommended operating conditions.
*3: Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4: When stored alone in nitrogen or vacuum atmosphere.

8. RECOMMENDED OPERATING CONDITIONS

V_{SS}=0V

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Oscillator frequency *1	f_{OSC}	V_{DD}=1.6 to 3.63V	Hx1～Hx5 ver.	20		60	MHz
			HxP ver.	40		80	
Output frequency	f_{OUT}	V_{DD}=1.6 to 3.63V, C_{LOUT}≤15pF	Hx1～Hx5 ver.	1.25		60	MHz
			HxP ver.	40		80	
Operating supply voltage	V_{DD}	Voltage between VDD and VSS *2		1.60		3.63	V
Input voltage	V_{IN}	Input pins		V_{SS}		V_{DD}	V
Operating temperature	T_a			-40		+125	°C
Output load capacitance	C_{LOUT}	Q output				15	pF

*1: The oscillation frequency is a yardstick value and the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2: For stable operation of this product, please mount ceramic chip capacitor that is more than 0.01uF between VDD and VSS in close proximity to IC (within 3mm). Wiring pattern between IC and capacitor should be as thick as possible.

* Since it may influence the reliability if it is used out of the recommended operating conditions range, this product should be used within this range.

9. ELECTRICAL CHARACTERISTICS

9.1. DC Characteristics

V_{DD} = 1.60 to 3.63V, V_{SS} = 0V, T_a = -40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Q pin HIGH-level output voltage	V_{OH}	measurement circuit 3, I_{OH}=-4mA		V_{DD} -0.4		V_{DD}	V
Q pin LOW-level output voltage	V_{OL}	measurement circuit 3, I_{OL}=4mA		0		0.4	V
INHN pin HIGH-level input voltage	V_{IH}	measurement circuit 4		0.7V_{DD}			V
INHN pin LOW-level input voltage	V_{IL}	measurement circuit 4				0.3V_{DD}	V
Q pin Output leakage current	I_Z	measurement circuit 5, INHN=LOW	Q=V_{DD}			10	µA
			Q=V_{SS}	-10			
Current consumption *1 (Hx1 version: fundamental frequency output)	I_{DD1}_3.3V	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=48MHz, f_{OUT}=48MHz	V_{DD}=3.3V		1.6	2.8	mA
	I_{DD1}_2.5V		V_{DD}=2.5V		1.0	1.8	
	I_{DD1}_1.8V		V_{DD}=1.8V		0.8	1.4	
Current consumption *1 (Hx2 version: Divide-by-2 frequency output)	I_{DD2}_3.3V	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=48MHz, f_{OUT}=24MHz	V_{DD}=3.3V		1.3	2.4	mA
	I_{DD2}_2.5V		V_{DD}=2.5V		0.8	1.6	
	I_{DD2}_1.8V		V_{DD}=1.8V		0.6	1.2	
Current consumption *1 (Hx3 version: Divide-by-4 frequency output)	I_{DD3}_3.3V	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=48MHz, f_{OUT}=12MHz	V_{DD}=3.3V		1.1	2.0	mA
	I_{DD3}_2.5V		V_{DD}=2.5V		0.7	1.4	
	I_{DD3}_1.8V		V_{DD}=1.8V		0.5	1.0	
Current consumption *1 (Hx4 version: Divide-by-8 frequency output)	I_{DD4}_3.3V	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=48MHz, f_{OUT}=6MHz	V_{DD}=3.3V		1.0	2.0	mA
	I_{DD4}_2.5V		V_{DD}=2.5V		0.6	1.2	
	I_{DD4}_1.8V		V_{DD}=1.8V		0.5	1.0	
Current consumption *1 (Hx5 version: Divide-by-16 frequency output)	I_{DD5}_3.3V	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=48MHz, f_{OUT}=3MHz	V_{DD}=3.3V		1.0	1.8	mA
	I_{DD5}_2.5V		V_{DD}=2.5V		0.6	1.2	
	I_{DD5}_1.8V		V_{DD}=1.8V		0.4	0.8	
Current consumption *1 (HxP version: fundamental frequency output)	I_{DDP}_3.3V	Measurement circuit 1, INHN=OPEN, no load, f_{OSC}=80MHz, f_{OUT}=80MHz	V_{DD}=3.3V		2.3	4.8	mA
	I_{DDP}_2.5V		V_{DD}=2.5V		1.6	3.4	
	I_{DDP}_1.8V		V_{DD}=1.8V		1.2	2.6	
Standby current	I_{ST}	Measurement circuit 1, INHN=LOW	T_a=-40 to +85°C			10	µA
			T_a=-40 to +125°C			20	µA
INHN pin pull-up resistance	R_{PU1}	Measurement circuit 6		1	2	3	MΩ
	R_{PU2}	Measurement circuit 6		50	100	200	kΩ
Oscillator feedback resistance	R_f			50	100	200	kΩ
Oscillator capacitance (Hx1～Hx5 ver.)	C_G	Confirmed using monitor pattern on the wafer. Design value, excluding parasitic capacitance		2.8	3.5	4.2	pF
	C_D			4.4	5.5	6.6	
Oscillator capacitance (HxP ver.)	C_G	Confirmed using monitor pattern on the wafer. Design value, excluding parasitic capacitance		0.8	1.0	1.2	pF
	C_D			1.6	2.0	2.4	

*1: The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

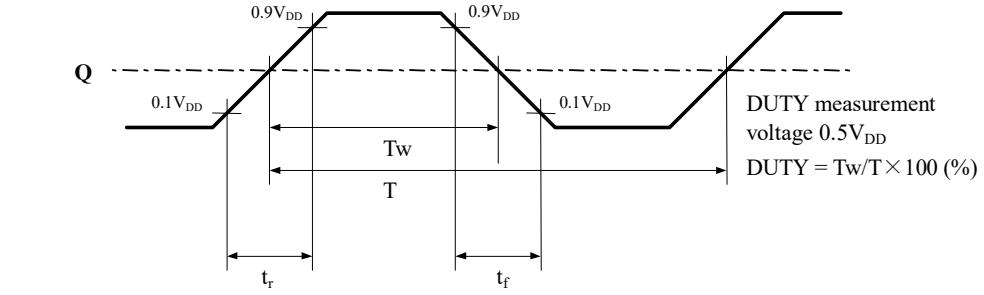
$$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA] + C_{LOUT}[pF] \times V_{DD}[V] \times f_{OUT}[MHz] \cdot 10^{-3}$$

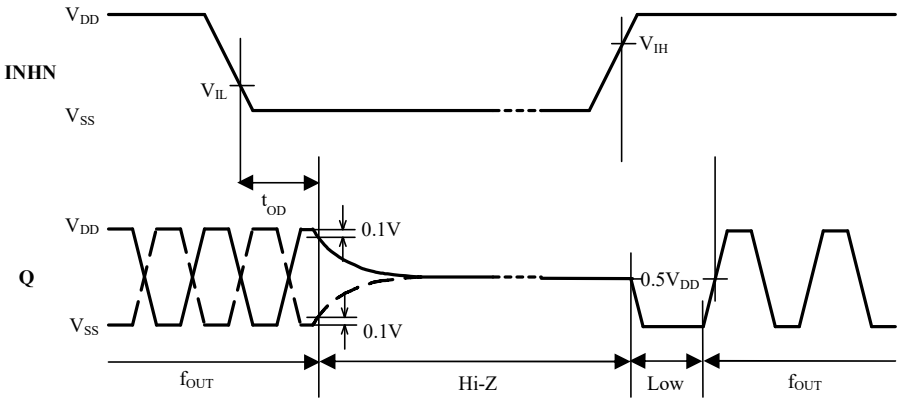
9.2. AC Characteristics

V_{DD} = 1.60 to 3.63V, V_{SS} = 0V, T_a = -40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Q pin Output rise time (Hx1～Hx5 ver.)	t_{r1}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=2.25 to 3.63V		1.4	5.0	ns
	t_{r2}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=1.60 to 2.25V		2.6	6.0	
Q pin Output fall time (Hx1～Hx5 ver.)	t_{f1}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=2.25 to 3.63V		1.4	5.0	ns
	t_{f2}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=1.60 to 2.25V		2.6	6.0	
Q pin Output rise time (HxP ver.)	t_{r1}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=2.25 to 3.63V		1.0	3.5	ns
	t_{r2}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=1.60 to 2.25V		2.0	5.0	
Q pin Output fall time (HxP ver.)	t_{f1}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=2.25 to 3.63V		1.0	3.5	ns
	t_{f2}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=1.60 to 2.25V		2.0	5.0	
Q pin Output duty cycle	DUTY	Measurement circuit 1, T_a=25°C, C_{LOUT}=15pF, V_{DD}=1.60 to 3.63V	45	50	55	%
Q pin Output disable delay time	t_{OD}	Measurement circuit 2, T_a=25°C, $C_{LOUT} \leq$15pF			200	ns

TIMING DIAGRAMS





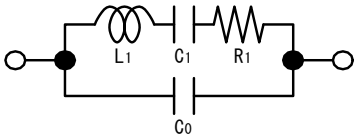
When INHN goes HIGH to LOW, the Q output becomes high impedance.
・When INHN goes LOW to HIGH, the Q output goes LOW once and then becomes normal output operation after having detected oscillation signals.

10. REFERENCE DATA (7052 TYPICAL CHARACTERISTICS)

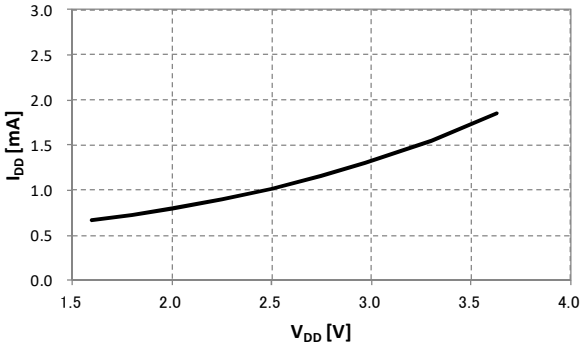
The following characteristics are measured using the crystal below.
Note that the characteristics will vary with the crystal used.

Crystal used for measurement

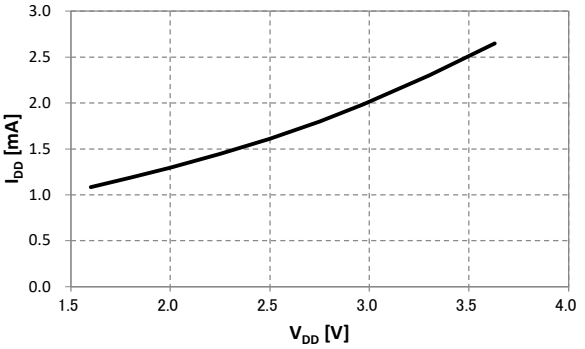
Parameter	48MHz	80MHz
C0(pF)	2.2	3.2
R1(Ω)	17.4	12.6



10.1. Current Consumption

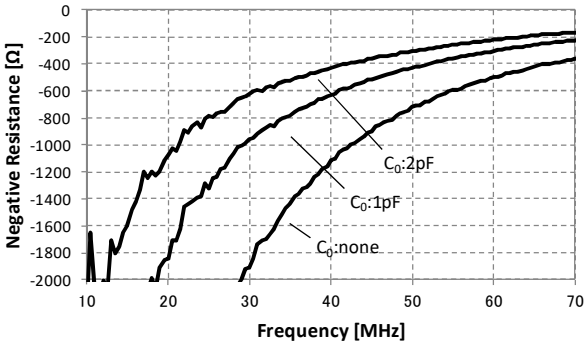


7052Hx1, f_{OSC}=48MHz, T_a=25℃, no load

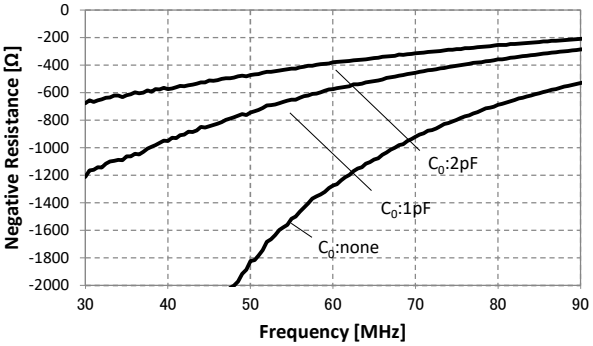


7052HxP, f_{OSC}=80MHz, T_a=25℃, no load

10.2. Negative Resistance



7052Hx1, V_{DD}=3.3V, T_a=25℃

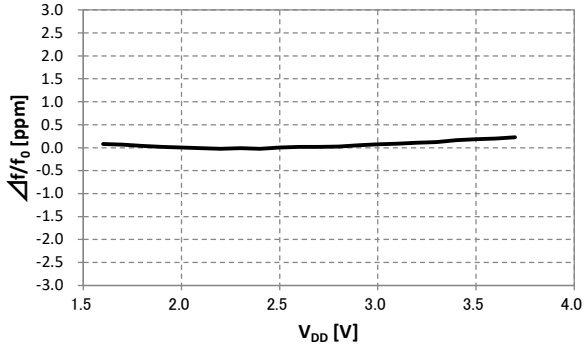


7052HxP, V_{DD}=3.3V, T_a=25℃

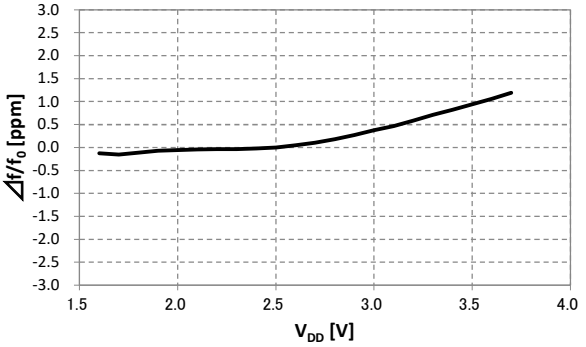
Measurement equipment: Agilent Impedance analyzer 4396B

The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XT and XTN pins. They were performed with Agilent 4396B using the NPC test jig.
They may vary in a measurement jig, and measurement environment.

10.3. Frequency Deviation with Voltage

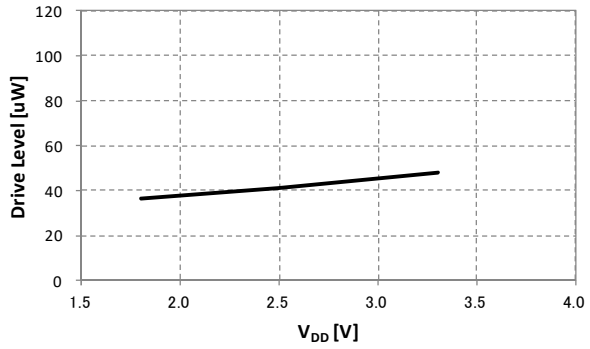


7052Hx1, f_{OSC}=48MHz, T_a=25℃, 2.5V std.

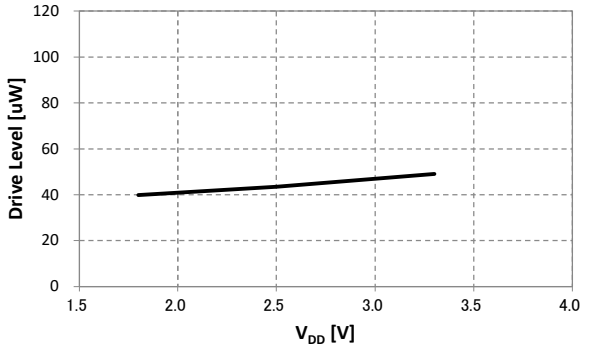


7052HxP, f_{OSC}=80MHz, T_a=25℃, 2.5V std.

10.4. Drive Level

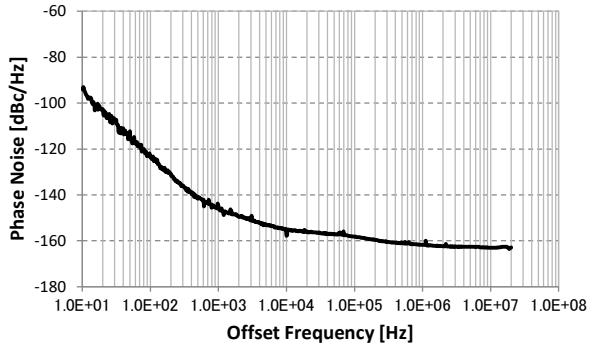


7052Hx1, f_{OSC}=48MHz, T_a=25℃

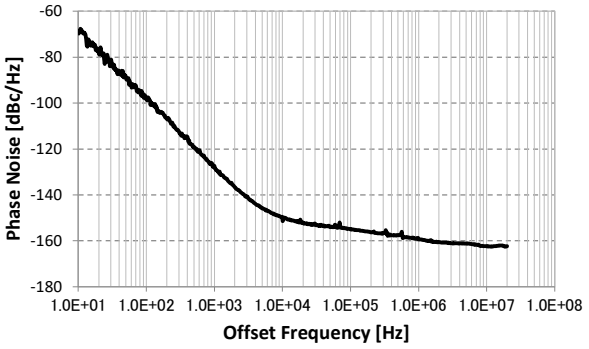


7052HxP, f_{OSC}=80MHz, T_a=25℃

10.5. Phase Noise



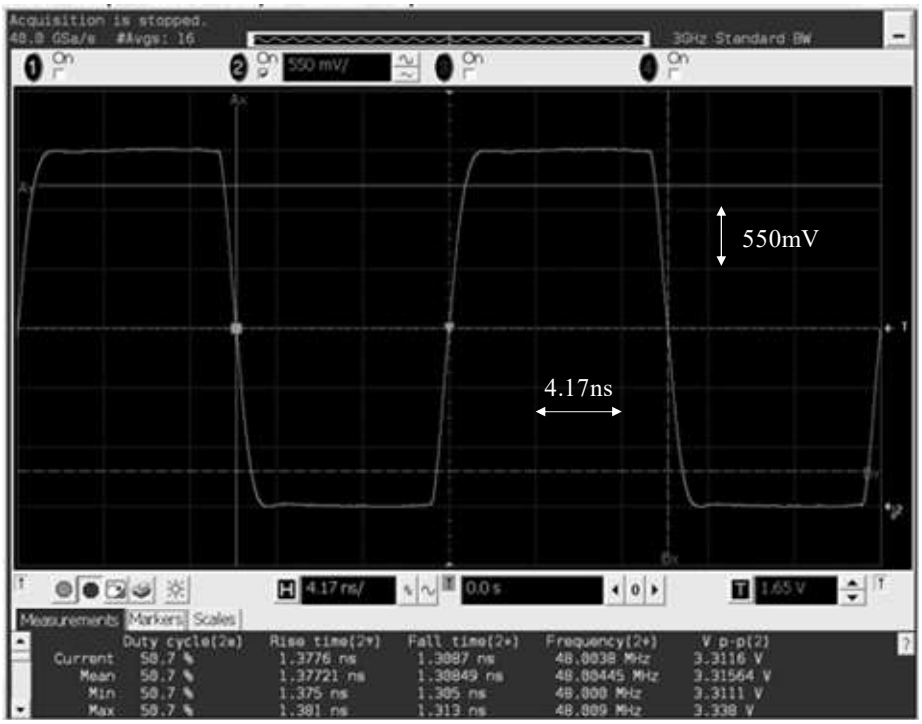
7052Hx1, f_{OSC}=48MHz, V_{DD}=3.3V, T_a=25℃



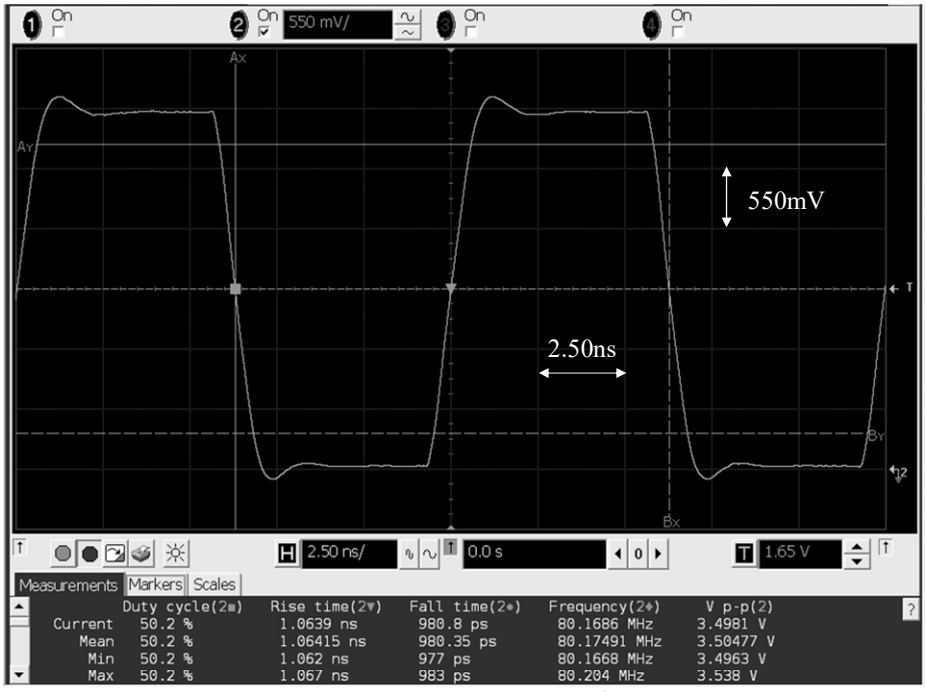
7052HxP, f_{OSC}=80MHz, V_{DD}=3.3V, T_a=25℃

Measurement equipment: Signal Source Analyzer Agilent E5052A

10.6. Output Waveform



7052Hx1, V_{DD}=3.3V, f_{OUT}=48MHz, C_{LOUT}=15pF, T_a=25℃



7052HxP, V_{DD}=3.3V, f_{OUT}=80MHz, C_{LOUT}=15pF, T_a=25℃
Measurement equipment: Oscilloscope Agilent DSO80604B

11. FUNCTIONAL DESCRIPTION

11.1. INHN Function

Q output is stopped and becomes high impedance.

INHN	Q	Oscillator
HIGH or Open	f_{OUT}	Operating
LOW	Hi-Z	Stopped

11.2. Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

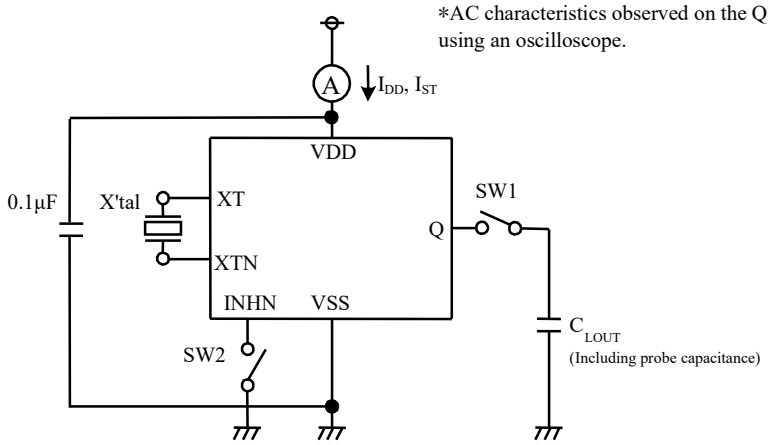
11.3. Oscillation Detection Function

The 7052 series have an oscillation detection circuit.

The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

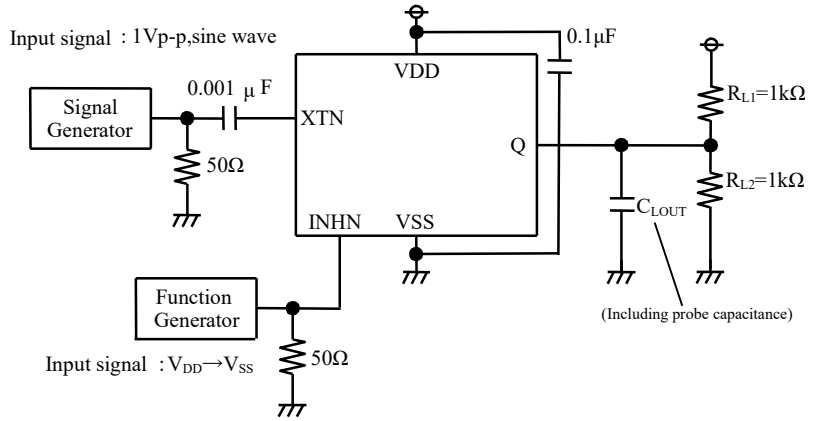
12. MEASUREMENT CIRCUITS

- Measurement circuit 1 Parameters: I_{DD}, I_{ST}, DUTY, t_r, t_f

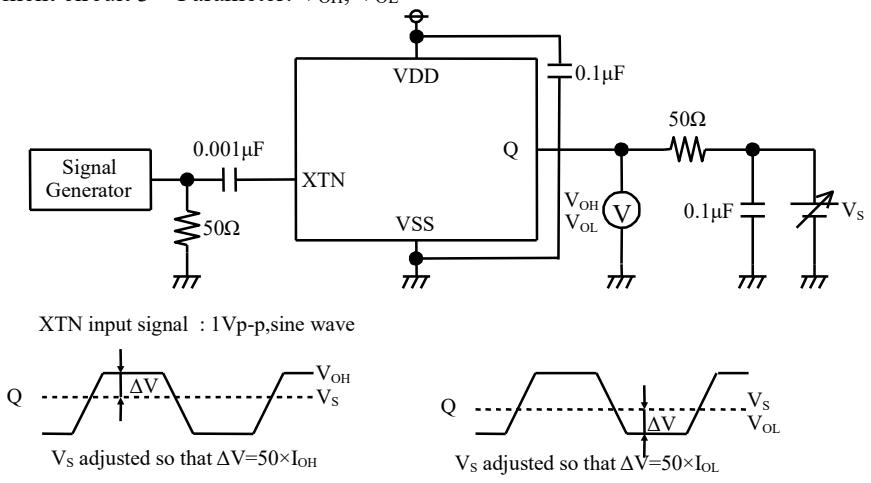


Parameter	SW1	SW2
I_{DD}	OFF	OFF
I_{ST}	ON or OFF	ON
DUTY,t_r,t_f	ON	OFF

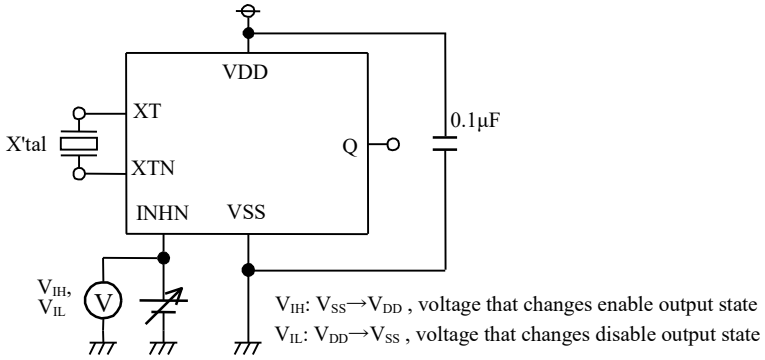
- Measurement circuit 2 Parameter: t_{OD}



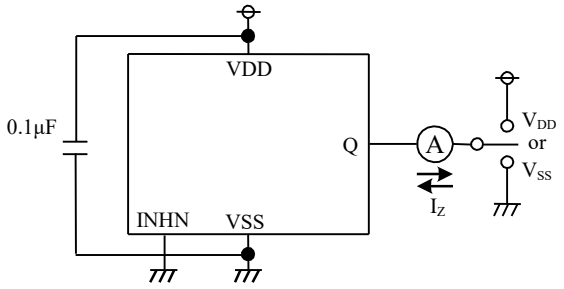
- Measurement circuit 3 Parameter: V_{OH}, V_{OL}



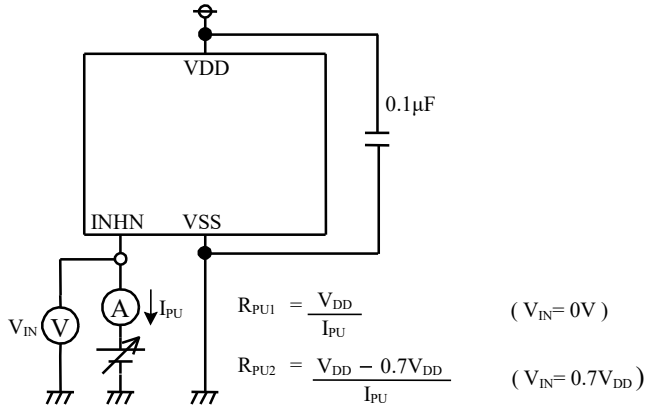
- Measurement circuit 4 Parameter: V_{IH}, V_{IL}



- Measurement circuit 5 Parameter: I_Z



- Measurement circuit 6 Parameter: R_{PU1}, R_{PU2}

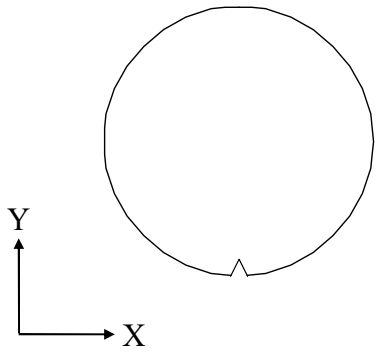


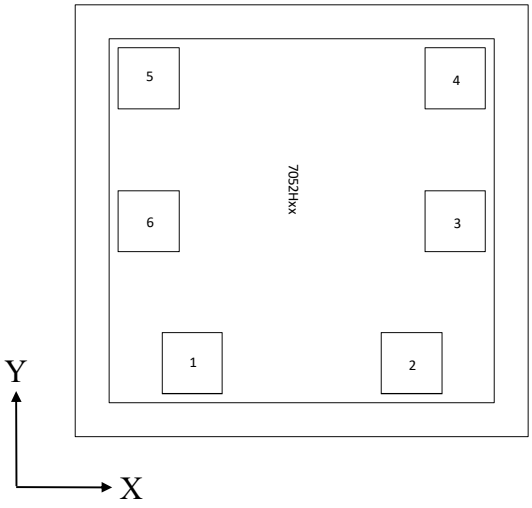
13. WAFER SURFACE ALIGNMENT DIAGRAM

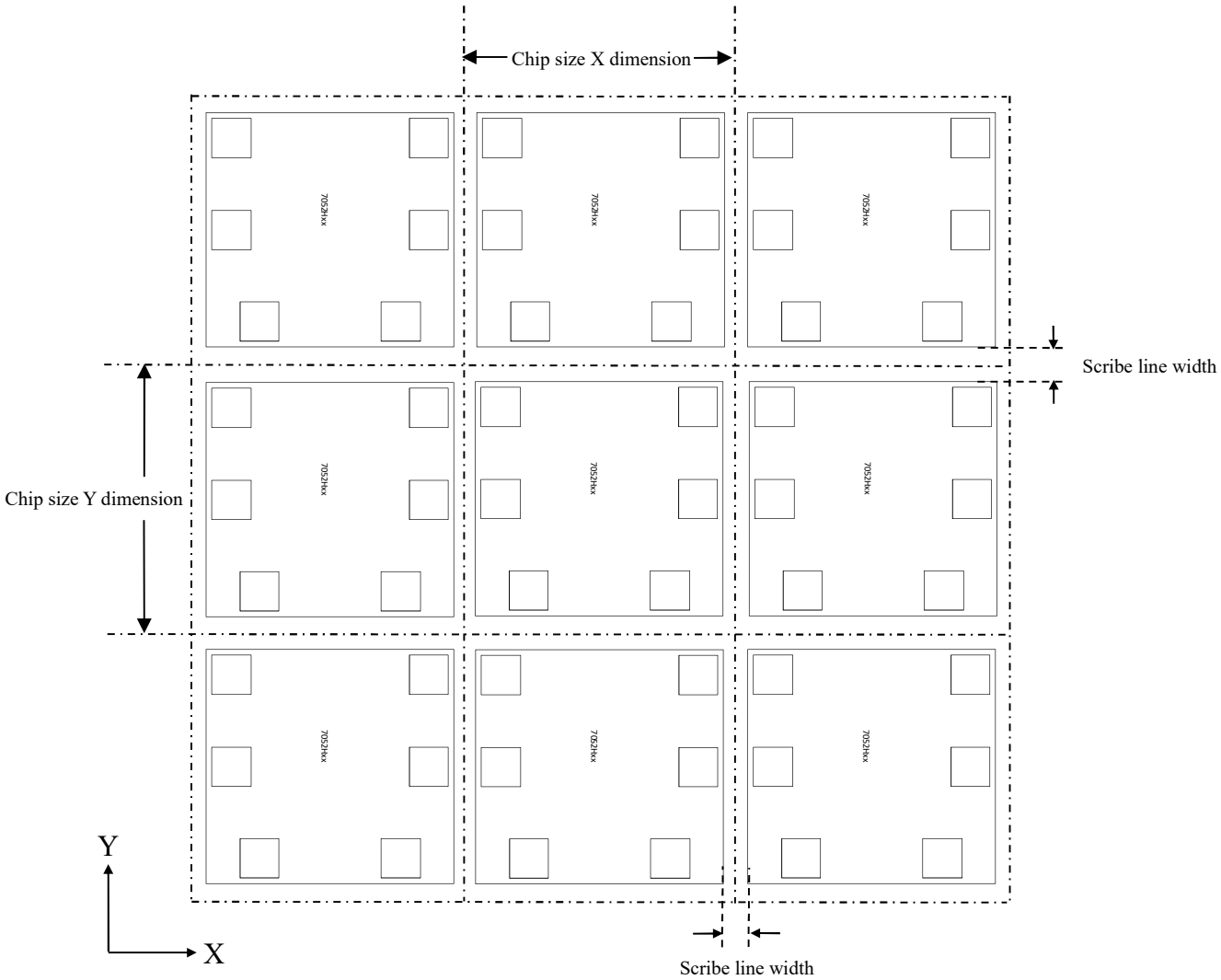
Wafer size:200mm±0.5mm

Scribe line width: 70μm

notch: Bottom

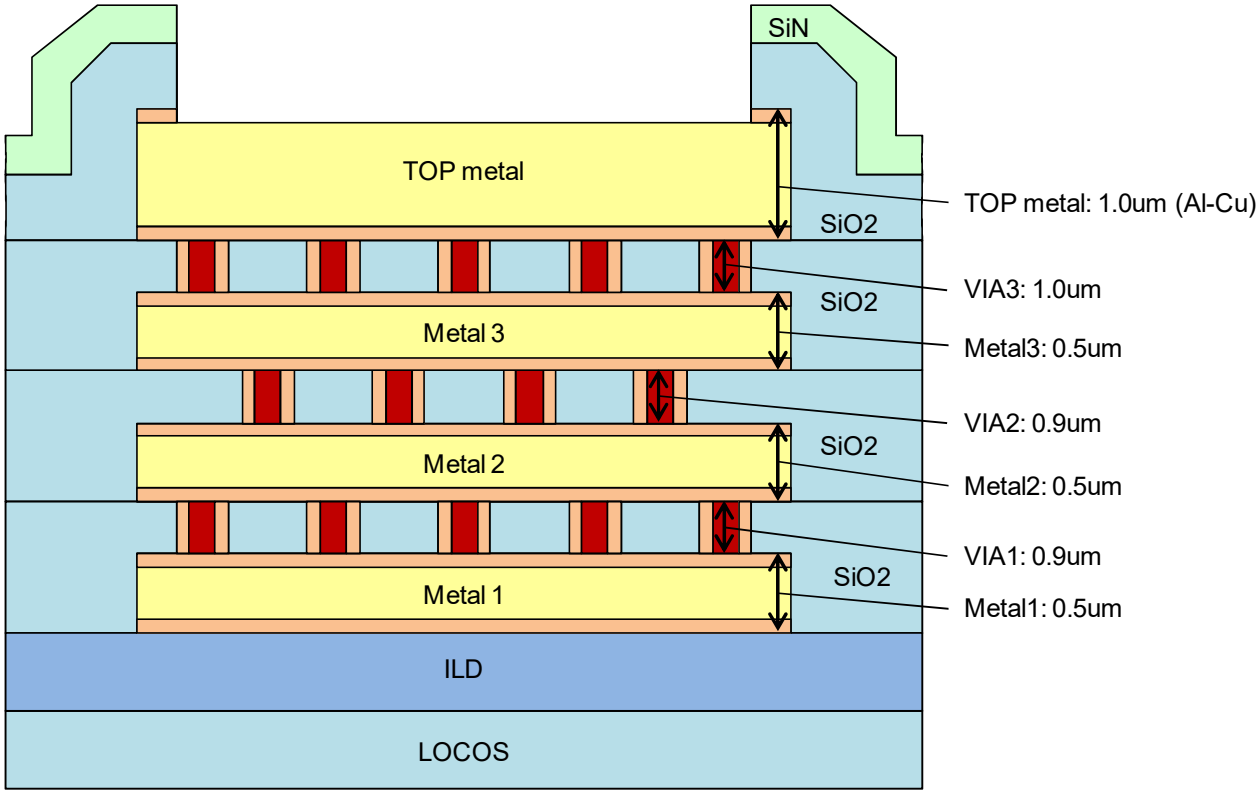






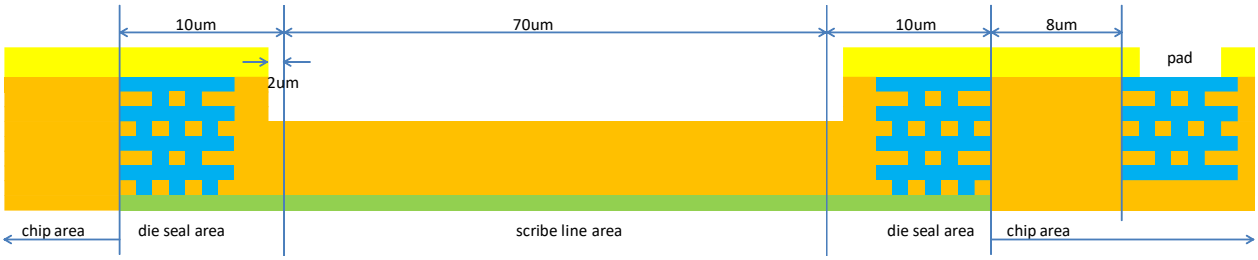
14. CROSS SECTION STRUCTURE

14.1. PAD Cross Section Structure



*Film thicknesses of mention is a value in the designs as above and is not the actual value in the chip.

14.2. Seal Ring and Scribe Line Cross Section Structure



*Widths of mention is a value in the designs as above and is not the actual value in the chip.

15. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.
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In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

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   If you wish to use the Products in that apparatus, please contact our sales section in advance.
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