5420 series

VCXO Module ICs with Built-in Varicap

OVERVIEW

The 5420 series are LV-PECL output VCXO ICs that provide a wide frequency pulling range. They employ bipolar oscillator circuit and recently developed varicap diode fabrication process that provides a low phase noise characteristic and a wide frequency pulling range without any external components. The 5420 series are ideal for wide pulling range, low phase noise, VCXO modules.

FEATURES

- VCXO with recently developed varicap diode built-in
- Oscillator: Fundamental frequency oscillation
- Output frequency: 100 to 250MHz
- Operating supply voltage range: 2.97 to 3.63V
- Oscillator frequency range (for fundamental oscillation):
  100 to 170MHz (B version)
  150 to 200MHz (C version)
  200 to 250MHz (D version)
- Wide frequency pulling range (typ)
  ±130ppm@B version, V_C=1.65±1.65V, f_{OUT}=122.88MHz (γ=330, C_0=1.6pF)
  ±120ppm@C version, V_C=1.65±1.65V, f_{OUT}=155.52MHz (γ=330, C_0=1.5pF)
  * D version: TBD
- Low phase noise (typ): -125dBc/Hz@B version, 1kHz Offset, f_{OUT}=122.88MHz (γ=330, C_0=1.6pF)
  -157dBc/Hz@B version, 10MHz Offset, f_{OUT}=122.88MHz
  -125dBc/Hz@C version, 1kHz Offset, f_{OUT}=155.52MHz (γ=330, C_0=1.5pF)
  -157dBc/Hz@C version, 10MHz Offset, f_{OUT}=155.52MHz
  * D version: TBD
- -40 to +105°C operating temperature range
- Differential LV-PECL output
- Output enable (OE) active selectable function
  Selectable Hi-Active or Low-Active by bonding wire

APPLICATIONS

Base station, SONET/SDH, Ethernet, Fibre Channel, LTE

SERIES CONFIGURATION

Version Name	Recommended operating frequency range (f_{OSC})*1 [MHz]	Output frequency (f_{OUT})
5420B	100MHz to 170MHz	f_{OSC}
5420C	150MHz to 200MHz	f_{OSC}
(5420D)*2	200MHz to 250MHz	f_{OSC}

*1. The recommended oscillation frequency is a yardstick value derived from the resonator used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to resonator characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
The recommended characteristics for the crystal element are:
R_1 < 20Ω, C_0 < 1.5pF

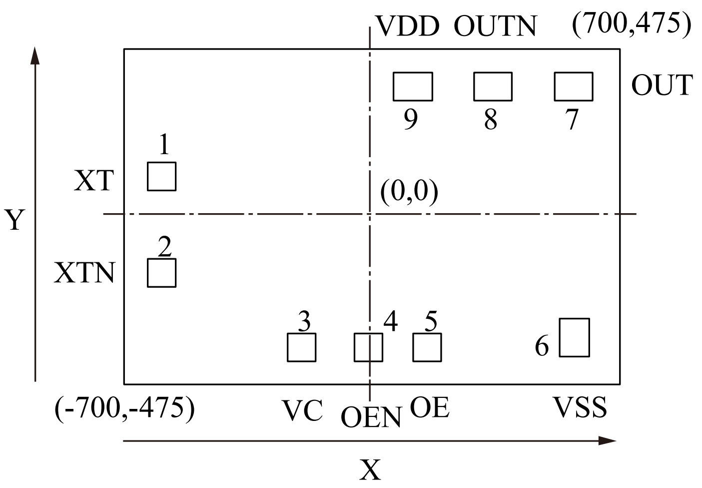
*2. The version name in parentheses has been developed.

ORDERING INFORMATION

Device	Package	Version name
WF5420x-4	Wafer form	WF5420□-4 Form WF: Wafer form CF: Chip(Die) form Oscillation frequency range
CF5420x-4	Chip form	

PAD LAYOUT

(Unit: µm)



Chip size: 1.4mm×0.95mm

Chip thickness: 130µm

PAD size: 80µm×80µm (PAD No.1, 2, 3, 4, 5 pins)
110µm×80µm (PAD No.7, 8, 9 pins)
80µm×110µm (PAD No.6 pins)

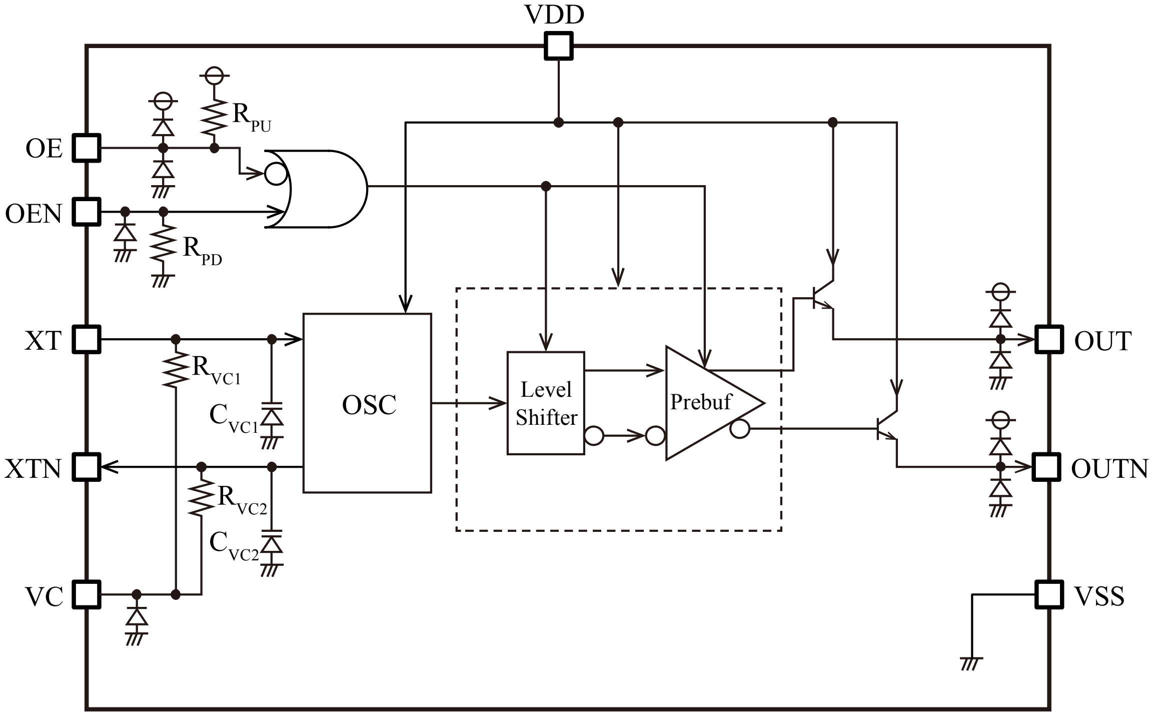
Chip base: V_{SS} potential

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O[*1]	Description	Pad Coordinates（Unit : µm）	
				X	Y
1	XT	I	Crystal connection pin	-595.0	116.0
2	XTN	O		-595.0	-159.0
3	VC	I	Control voltage input pin	-200.2	-370.0
4	OEN	I	Output enable input pin（built-in pull-down resistor）	-12.4	-370.0
5	OE	I	Output enable input pin（built-in pull-up resistor）	156.2	-370.0
6	VSS	-	(-) ground	595.0	-355.0
7	OUT	O	Clock output pin（differential output）	554.1	370.0
8	OUTN	O	Clock output pin（differential reversing output）	324.3	370.0
9	VDD	-	(+) supply voltage	99.5	370.0

*1.I: input, O: output

BLOCK DIAGRAM



The CF5420/WF5420 incorporated standard PECL output schemes, which are un-terminated emitters.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range*1	V_{DD}	VDD pins	-0.3 to +5.0	V
Input voltage range*1*2	V_{IN}	XT, OE, OEN, VC pins	-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	XTN, OUT, OUTN pins	-0.3 to V_{DD}+0.3	V
Junction temperature*3	T_j		+125	°C
Storage temperature range*4	T_{STG}	Wafer, Chip form	-55 to +125	°C

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Operating supply voltage	V_{DD}	Between VDD and VSS pins*2	2.97	3.3	3.63	V
Input voltage	V_{IN}	OE, OEN, VC pins	0		V_{DD}	V
Operating temperature	T_a		-40		+105	°C
Output load	R_L	Terminated to V_{DD}-2V	49.5	50.0	50.5	Ω
Oscillator frequency range*1	f_{OSC}	5420B	100		170	MHz
		5420C	150		200	
		5420D	200		250	
Output frequency range	f_{OUT}	5420B	100		170	MHz
		5420C	150		200	
		5420D	200		250	

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5420 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
B version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating MIN	Rating TYP	Rating MAX	Unit
Current consumption1	I_{DD1}	measurement circuit 1, terminated to V_{DD}-2V, OE,OEN=Open			68	90	mA
Current consumption2	I_{DD2}	measurement circuit 1, terminated to V_{DD}-2V, OE=Low or OEN=High oscillator: operating, output: disabled			2.3	3.5	mA
High-level output voltage (DC level)	V_{OH}	measurement circuit 2, OUT/OUTN pins	T_a=0 to +105°C	V_{DD} -1.025	V_{DD} -0.950	V_{DD} -0.880	V
			T_a=-40 to 0°C	V_{DD} -1.085	V_{DD} -1.005	V_{DD} -0.880	
Low-level output voltage (DC level)	V_{OL}	measurement circuit 2, OUT/OUTN pins		V_{DD} -1.810	V_{DD} -1.700	V_{DD} -1.620	V
Output leakage current	I_Z	measurement circuit 4, SW1,2=High or Low OE=Low or OEN=High OUT/OUTN pins, T_a=+25°C		-1		1	µA
High-level input voltage	V_{IH}	measurement circuit 3, OE/OEN pins		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 3, OE/OEN pins				0.3V_{DD}	V
Pull-up resistance	R_{PU}	measurement circuit 3, OE pin		50	100	200	kΩ
Pull-down resistance	R_{PD}	measurement circuit 3, OEN pin		50	100	200	kΩ
Oscillator block built-in resistance*1	R_{VC1}	Between VC and XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC and XTN, measurement circuit 5		100	200	300	
Input leakage resistance*1	R_{VIN}	VC pin, T_a=+25°C, measurement circuit 6		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Confirmed by acceptance sampling using wafer monitor pattern. Design value, excluding parasitic capacitance	V_C =0.3V	3.92	4.36	4.80	pF
			V_C =1.65V	2.35	2.76	3.17	
			V_C =3.0V	1.20	1.50	1.80	
	C_{VC2}	Confirmed by acceptance sampling using wafer monitor pattern. Design value, excluding parasitic capacitance	V_C =0.3V	5.88	6.53	7.18	pF
			V_C =1.65V	3.51	4.13	4.75	
			V_C =3.0V	1.80	2.25	2.70	
Maximum modulation frequency	F_M	-3dB frequency, T_a=+25°C, design value V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 9, Crystal : 122.88MHz		25	50		kHz

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC-XT or VC-XTN
Input leakage resistance: Resistance between VC-VDD or VC-VSS (DC characteristic)
Refer to "VC Terminal Input Impedance". (Page. 23)

C version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating			Unit
				MIN	TYP	MAX	
Current consumption1	I_{DD1}	measurement circuit 1, terminated to V_{DD}-2V, OE,OEN=Open			69	90	mA
Current consumption2	I_{DD2}	measurement circuit 1, terminated to V_{DD}-2V, OE=Low or OEN=High oscillator: operating, output: disabled			3.5	5.0	mA
High-level output voltage (DC level)	V_{OH}	measurement circuit 2, OUT/OUTN pins	T_a=0 to +105°C	V_{DD} -1.025	V_{DD} -0.950	V_{DD} -0.880	V
			T_a=-40 to 0°C	V_{DD} -1.085	V_{DD} -1.005	V_{DD} -0.880	
Low-level output voltage (DC level)	V_{OL}	measurement circuit 2, OUT/OUTN pins		V_{DD} -1.810	V_{DD} -1.700	V_{DD} -1.620	V
Output leakage current	I_Z	measurement circuit 4, SW1,2=High or Low OE=Low or OEN=High OUT/OUTN pins, T_a=+25°C		-1		1	µA
High-level input voltage	V_{IH}	measurement circuit 3, OE/OEN pins		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 3, OE/OEN pins				0.3V_{DD}	V
Pull-up resistance	R_{PU}	measurement circuit 3, OE pin		50	100	200	kΩ
Pull-down resistance	R_{PD}	measurement circuit 3, OEN pin		50	100	200	kΩ
Oscillator block built-in resistance*1	R_{VC1}	Between VC and XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC and XTN, measurement circuit 5		100	200	300	
Input leakage resistance*1	R_{VIN}	VC pin, T_a=+25°C, measurement circuit 6		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Confirmed by acceptance sampling using wafer monitor pattern. Design value, excluding parasitic capacitance	V_C =0.3V	3.92	4.36	4.80	pF
			V_C =1.65V	2.35	2.76	3.17	
			V_C =3.0V	1.20	1.50	1.80	
	C_{VC2}	Confirmed by acceptance sampling using wafer monitor pattern. Design value, excluding parasitic capacitance	V_C =0.3V	5.88	6.53	7.18	pF
			V_C =1.65V	3.51	4.13	4.75	
			V_C =3.0V	1.80	2.25	2.70	
Maximum modulation frequency	F_M	-3dB frequency, T_a=+25°C, design value V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 9, Crystal : 155.52MHz		25	50		kHz

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC-XT or VC-XTN
Input leakage resistance: Resistance between VC-VDD or VC-VSS (DC characteristic)
Refer to “VC Terminal Input Impedance” (Page. 23).

D version (TBD)

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating MIN	Rating TYP	Rating MAX	Unit
Current consumption1	I_{DD1}	measurement circuit 1, terminated to V_{DD}-2V, OE,OEN=Open			(73)	(94)	mA
Current consumption2	I_{DD2}	measurement circuit 1, terminated to V_{DD}-2V, OE=Low or OEN=High oscillator: operating, output: disabled			(5.6)	(8.0)	mA
High-level output voltage (DC level)	V_{OH}	measurement circuit 2, OUT/OUTN pins	T_a=0 to +105°C	V_{DD} -1.025	V_{DD} -0.950	V_{DD} -0.880	V
			T_a=-40 to 0°C	V_{DD} -1.085	V_{DD} -1.005	V_{DD} -0.880	
Low-level output voltage (DC level)	V_{OL}	measurement circuit 2, OUT/OUTN pins		V_{DD} -1.810	V_{DD} -1.700	V_{DD} -1.620	V
Output leakage current	I_Z	measurement circuit 4, SW1,2=High or Low OE=Low or OEN=High OUT/OUTN pins, T_a=+25°C		-1		1	μA
High-level input voltage	V_{IH}	measurement circuit 3, OE/OEN pins		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 3, OE/OEN pins				0.3V_{DD}	V
Pull-up resistance	R_{PU}	measurement circuit 3, OE pin		50	100	200	kΩ
Pull-down resistance	R_{PD}	measurement circuit 3, OEN pin		50	100	200	kΩ
Oscillator block built-in resistance*1	R_{VC1}	Between VC and XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC and XTN, measurement circuit 5		100	200	300	
Input leakage resistance*1	R_{VIN}	VC pin, T_a=+25°C, measurement circuit 6		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Confirmed by acceptance sampling using wafer monitor pattern. Design value, excluding parasitic capacitance	V_C =0.3V	(3.92)	(4.36)	(4.80)	pF
			V_C =1.65V	(2.35)	(2.76)	(3.17)	
			V_C =3.0V	(1.20)	(1.50)	(1.80)	
	C_{VC2}	Confirmed by acceptance sampling using wafer monitor pattern. Design value, excluding parasitic capacitance	V_C =0.3V	(5.88)	(6.53)	(7.18)	pF
			V_C =1.65V	(3.51)	(4.13)	(4.75)	
			V_C =3.0V	(1.80)	(2.25)	(2.70)	
Maximum modulation frequency	F_M	-3dB frequency, T_a=+25°C, design value V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 9, Crystal : 245.76MHz		25	50		kHz

Values in parentheses ( ) are temporary.

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC-XT or VC-XTN
Input leakage resistance: Resistance between VC-VDD or VC-VSS (DC characteristic)
Refer to "VC Terminal Input Impedance" (TBD) (Page. 23).

Switching Characteristics

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions		Rating			Unit
				MIN	TYP	MAX	
Duty cycle	Duty1	Measured at output cross point T_a=25°C, V_{DD}=3.3V, measurement circuit 7		45	50	55	%
	Duty2	Measured at 50% of output amplitude T_a=25°C, V_{DD}=3.3V, measurement circuit 7		45	50	55	%
Output amplitude	V_{OPP}	Peak to peak of output waveform Single-ended output signal, measurement circuit 7		0.4			V
Output rise time*1	t_r	20% to 80% of output amplitude Single-ended output signal, measurement circuit 7	-40 to 90°C		0.3	0.5	ns
			90 to 105°C			0.7	
Output fall time*1	t_f	80% to 20% of output amplitude Single-ended output signal, measurement circuit 7	-40 to 90°C		0.3	0.5	ns
			90 to 105°C			0.7	
Output enable propagation delay*2	t_{OE}	T_a=25°C, design value, measurement circuit 8				20	µs
Output disable propagation delay	t_{OD}	T_a=25°C, design value, measurement circuit 8				200	ns

*1. Output rise time and output fall time may vary depending on measurement environment.
*2. Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

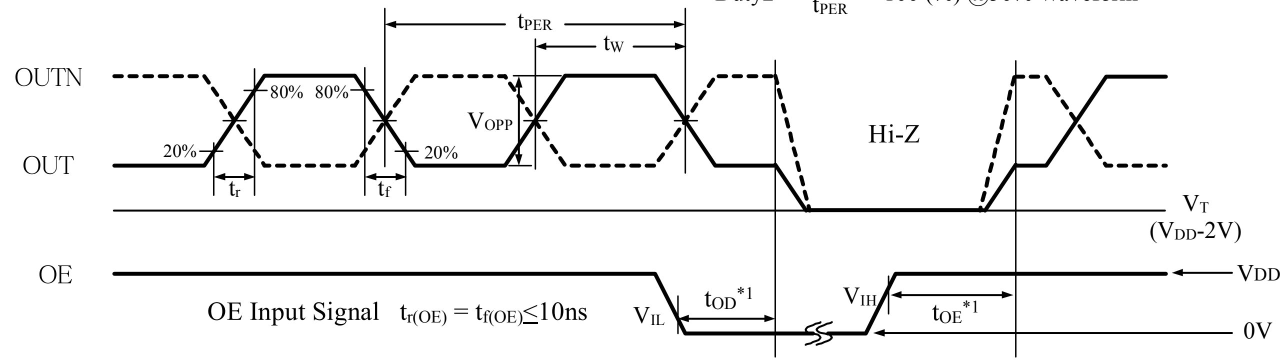
Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated.
The recommended crystal element characteristics are R_1 < 20Ω and C_0 < 1.5pF.

Timing chart

[Used OE pin]

$$\text{Duty1} = \frac{t_W}{t_{PER}} \times 100\ (\%)\ \text{@Crossing Point}$$

$$\text{Duty2} = \frac{t_W}{t_{PER}} \times 100\ (\%)\ \text{@50\% Waveform}$$

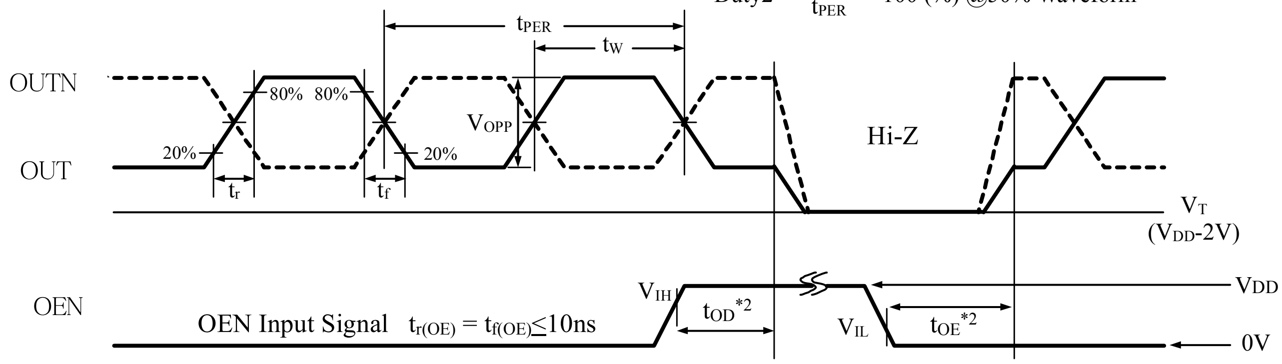


*1. On an OE falling edge, the outputs go high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) has elapsed. When this occurs, the output signal is pulled down to V_T (termination voltage) by the load resistance. On an OE rising edge, the output starts after the output enable propagation delay (t_{OE}) has elapsed.

[Used OEN pin]

$$\text{Duty1} = \frac{t_W}{t_{PER}} \times 100\ (\%)\ \text{@Crossing Point}$$

$$\text{Duty2} = \frac{t_W}{t_{PER}} \times 100\ (\%)\ \text{@50\% Waveform}$$



*2: On an OEN rising edge, the outputs go high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) has elapsed. When this occurs, the output signal is pulled down to V_T (termination voltage) by the load resistance. On an OEN falling edge, the output starts after the output enable propagation delay (t_{OE}) has elapsed.

FUNCTIONAL DESCRIPTION

OE Function

OE pin (built-in pull-up resistor)	Oscillator	Output
High/Open	Operating	Operating
Low	Operating	Disabled (Hi-Z)

OEN Function

OEN pin (built-in pull-down resistor)	Oscillator	Output
Low/Open	Operating	Operating
High	Operating	Disabled (Hi-Z)

When OE goes LOW and OEN goes HIGH, OUT and OUTN output DC Level (NPC test mode).

Oscillation Start-up Detector Function

An oscillator startup detection circuit is built-in. The circuit disables the OUT/OUTN outputs (high impedance) until the oscillator starts. This function prevents unstable oscillation and other problems, which can occur when power is applied, from appearing at the output.

Boot Function

At the time of oscillation starting, XTN pin potential is made into the V_{DD} level. It makes negative resistance enlarged and it becomes easy to start oscillation. Beware that a current flows into VC pin until it starts oscillation, when XTN pin is V_{DD} level and the voltage below V_{DD} level is being applied to VC pin.

A boot function is canceled after an oscillation start.

MEASUREMENT CIRCUITS

These are measurement circuits for electrical characteristics and switching characteristics.

■ Note: Bypass capacitors specified in each measurement circuit below should be connected between VDD, V_T and VSS. Load resistance specified in each measurement circuit below should be connected to OUT and OUTN pins (excluding measurement circuit 4, 5, 6).

Circuit wiring of bypass capacitors and load resistance should be connected as short as possible (within approximately 3mm). If the circuit wiring is long, the required characteristics may not be realized. Also, if the values of bypass capacitors and load resistance differ from the description in this document or are not connected, the required characteristics may not be realized.

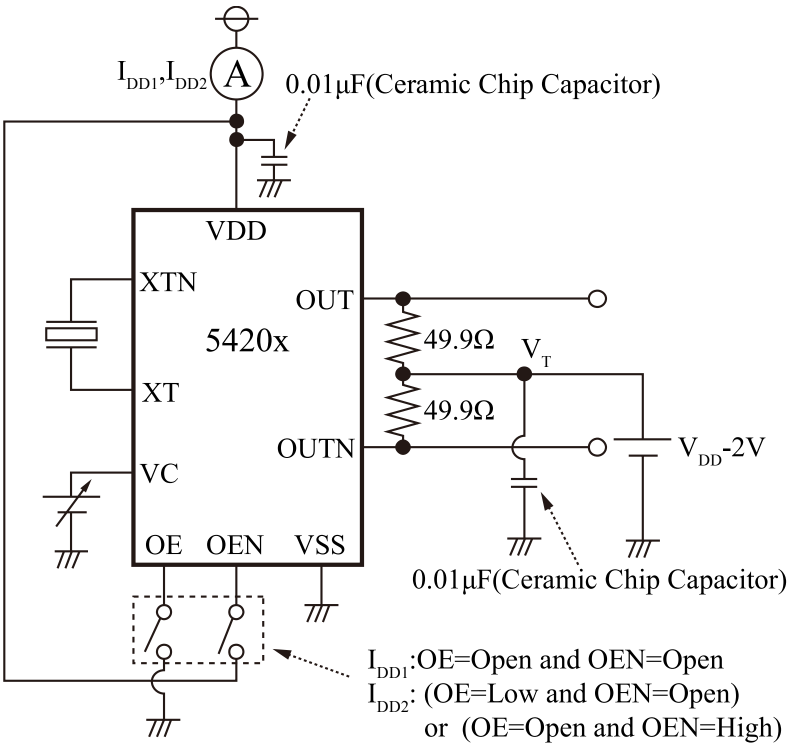
Capacitor and resistor values used by NPC

Capacitors: 0.01µF GRM188B11H103K (Murata Manufacturing Co., Ltd.)

Resistors: 49.9Ω RN732ATTD49R9B25 (KOA Corporation)

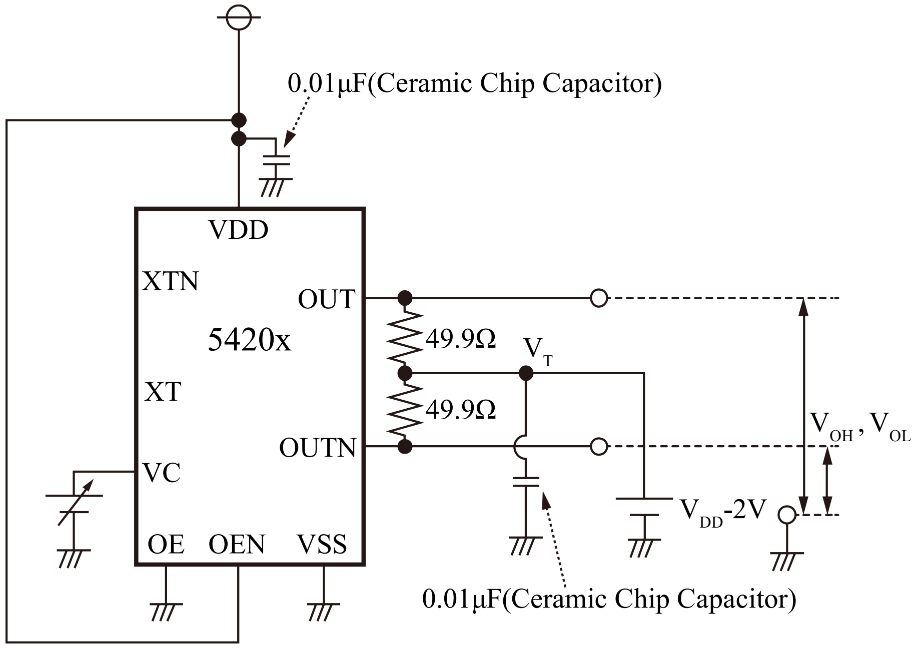
MEASUREMENT CIRCUIT 1

Measurement Parameters: I_{DD1}, I_{DD2}



MEASUREMENT CIRCUIT 2

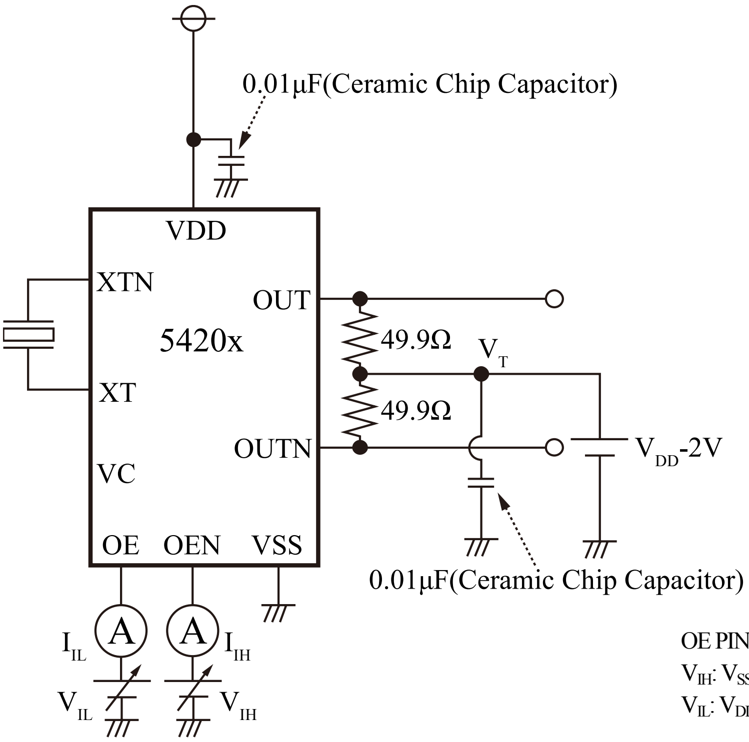
Measurement Parameters: V_{OH}, V_{OL}



VC=High:OUT=V_{OL}, OUTN=V_{OH}
VC=Low:OUT=V_{OH}, OUTN=V_{OL}

MEASUREMENT CIRCUIT 3

Measurement Parameters: R_{PU}, R_{PD}, V_{IH}, V_{IL}



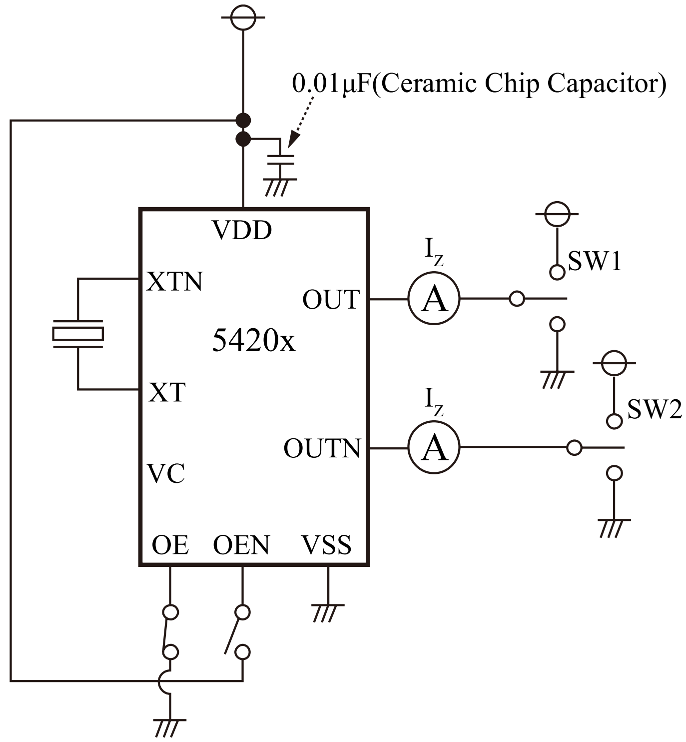
$R_{PU}=V_{IL}/I_{IL}$
$R_{PD}=V_{IH}/I_{IH}$

OE PIN
V_{IH}: $V_{SS}\rightarrow V_{DD}$, voltage that changes enable output state
V_{IL}: $V_{DD}\rightarrow V_{SS}$, voltage that changes disable output state

OEN PIN
V_{IH}: $V_{SS}\rightarrow V_{DD}$, voltage that changes disable output state
V_{IL}: $V_{DD}\rightarrow V_{SS}$, voltage that changes enable output state

MEASUREMENT CIRCUIT 4

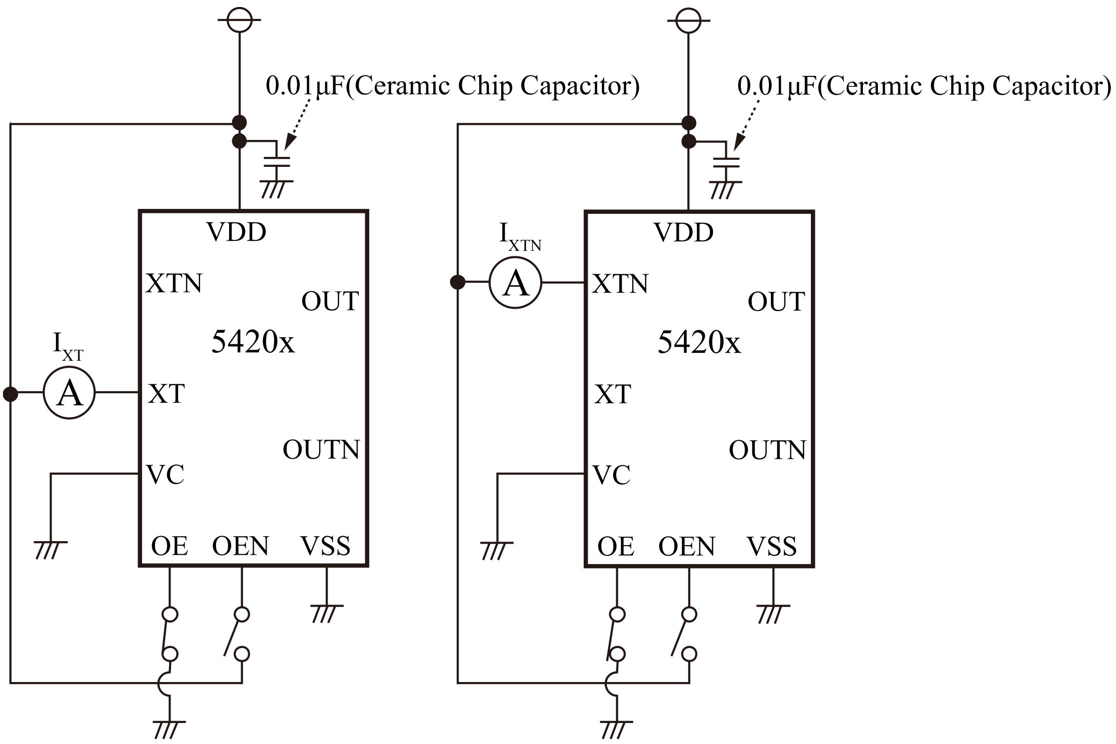
Measurement Parameters: I_Z



(OE=Low and OEN=Open) or (OE=Open and OEN=High)

MEASUREMENT CIRCUIT 5

Measurement Parameters: R_{VC1}, R_{VC2}

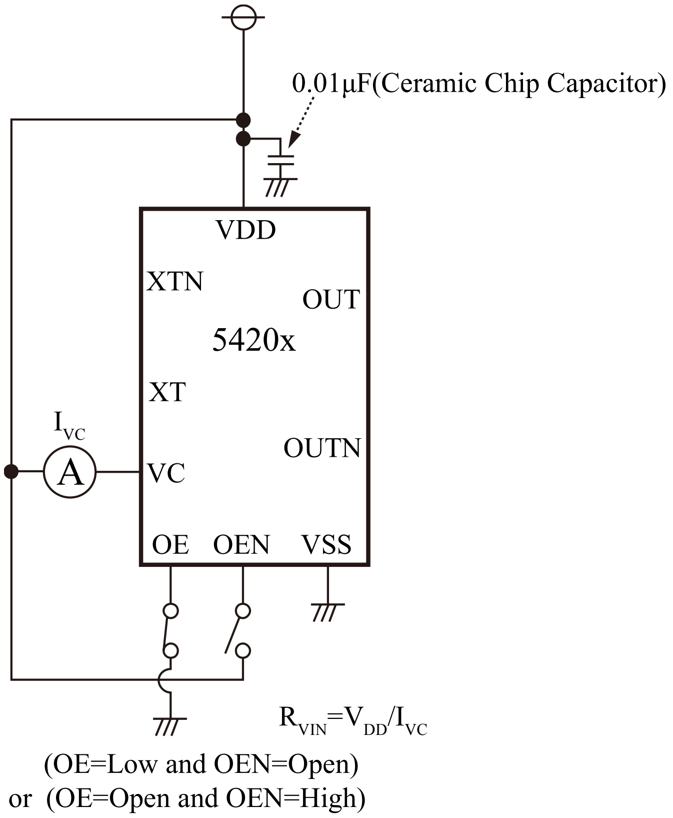


$R_{VC1}=V_{DD}/I_{XT}$ $R_{VC2}=V_{DD}/I_{XTN}$

(OE=Low and OEN=Open) or (OE=Open and OEN=High)

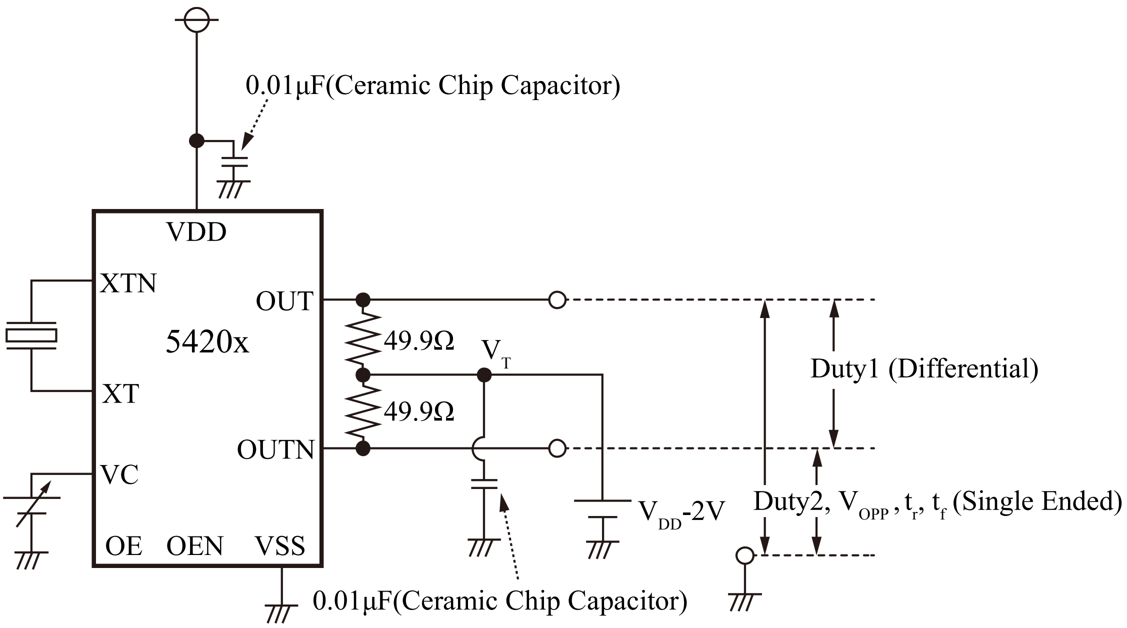
MEASUREMENT CIRCUIT 6

Measurement Parameters: R_{VIN}



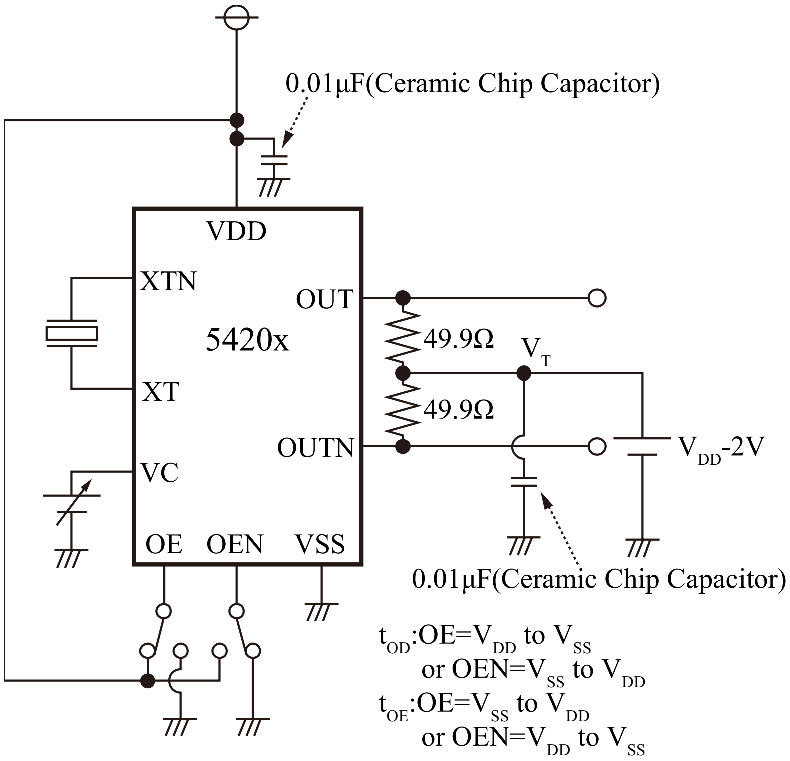
MEASUREMENT CIRCUIT 7

Measurement Parameters: Duty1, Duty2, V_{OPP}, t_r, t_f



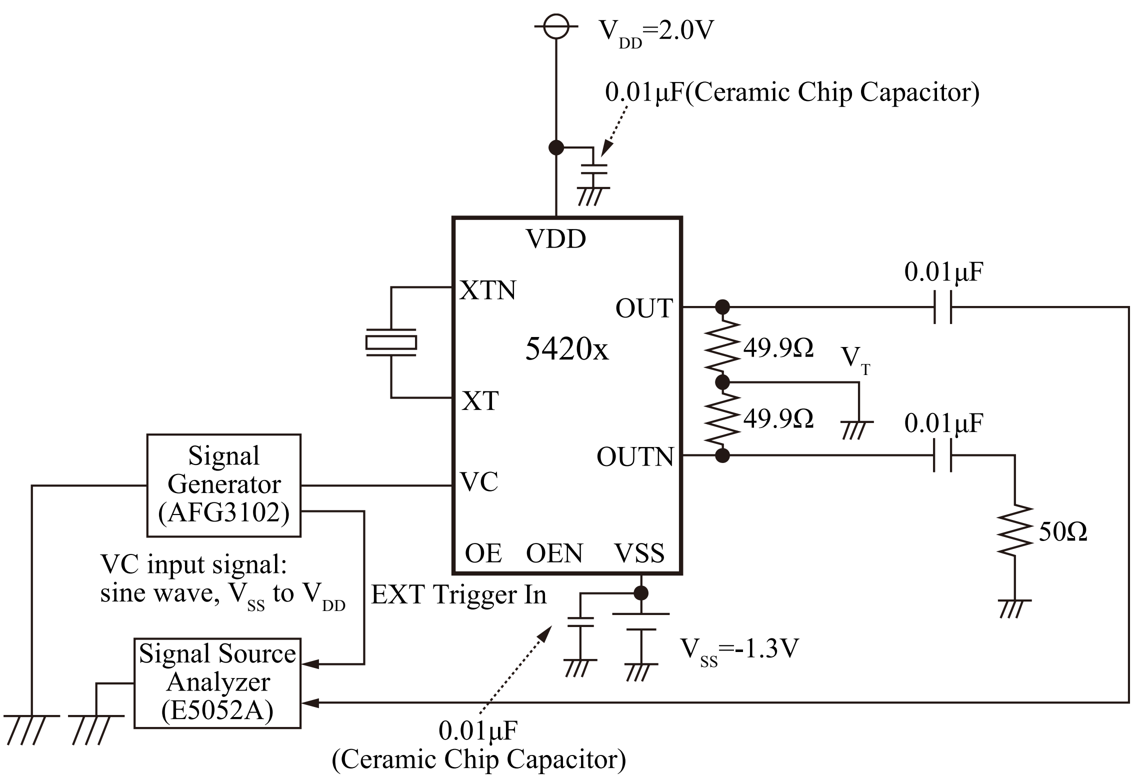
MEASUREMENT CIRCUIT 8

Measurement Parameters: t_{OE}, t_{OD}



MEASUREMENT CIRCUIT 9

Measurement Parameters: F_M



REFERENCE DATA

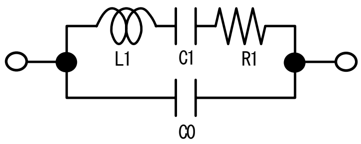
The characters given below were measured using an NPC standards jig and standard crystal element, and do not represent a guarantee of device characteristics.

Note that the characteristics will vary due to measurement environment and the oscillator element used.

Crystal used for measurement

Parameter	B	C	D
f_{OSC}(MHz)	122.88MHz	155.52MHz	TBD
C0(pF)	1.6	1.5	TBD
γ(=C0/C1)	330	330	TBD
R1(Ω)	9	8	TBD

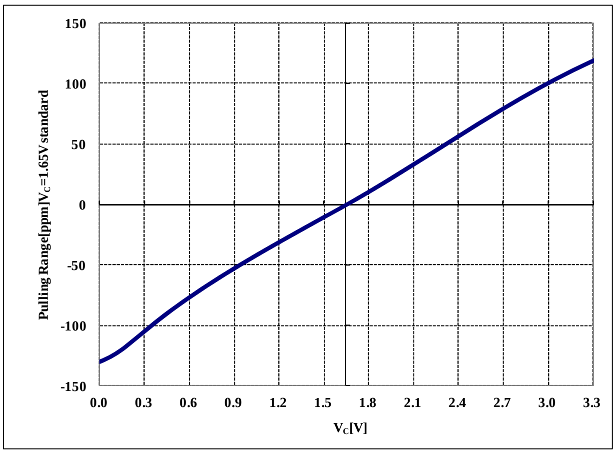
Crystal parameters



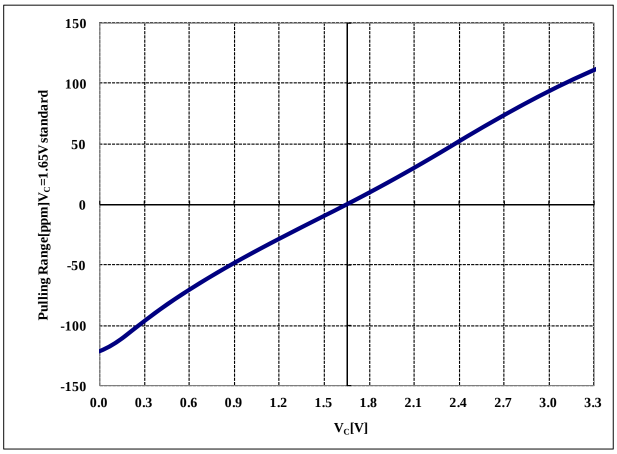
Pulling Range

[Measurement conditions] V_{DD}= +2.0V, V_{SS}= -1.3V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



[5420C] f_{OSC}=155.52MHz

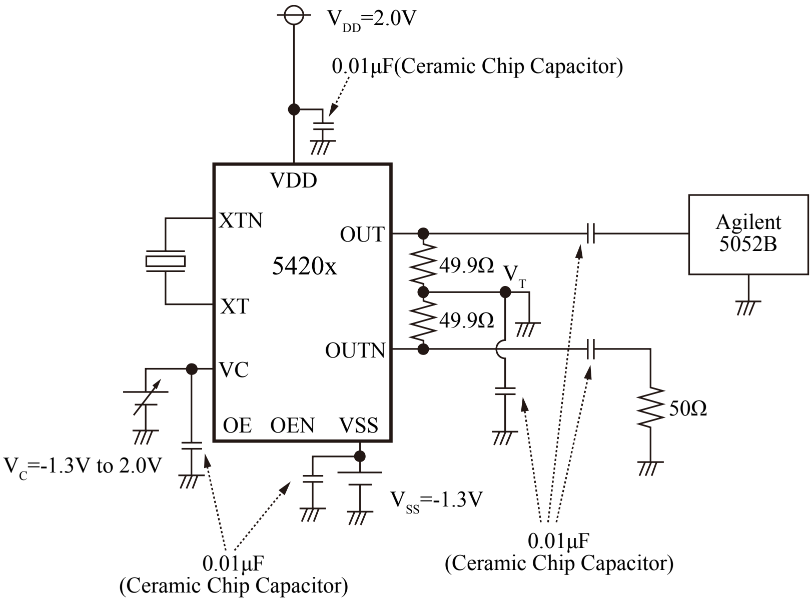


* V_C voltage in the graphs is adjusted to V_{SS}= 0V.

[5420D] f_{OSC}=245.76MHz

(TBD)

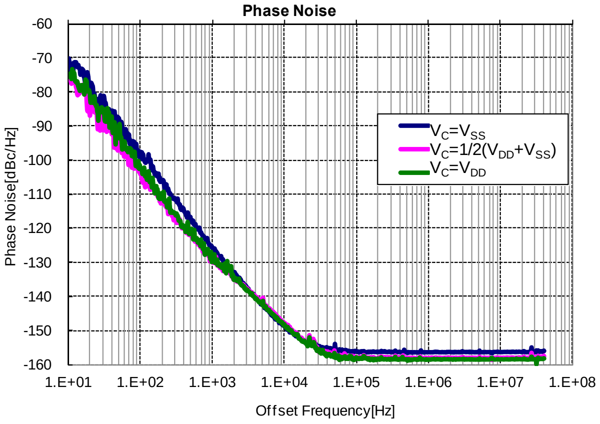
[Measurement circuit diagram]



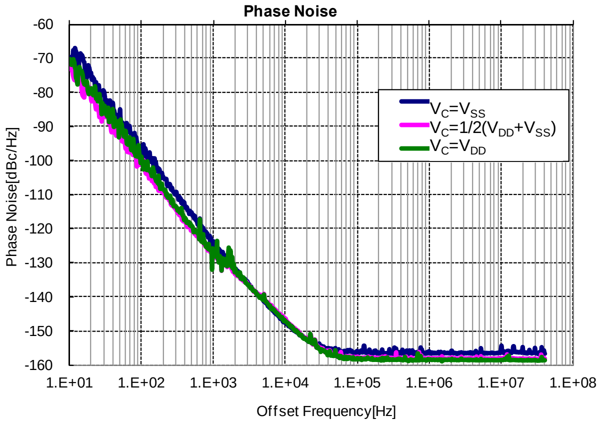
Phase Noise

[Measurement conditions] V_{DD}= +2.0V, V_{SS}= -1.3V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



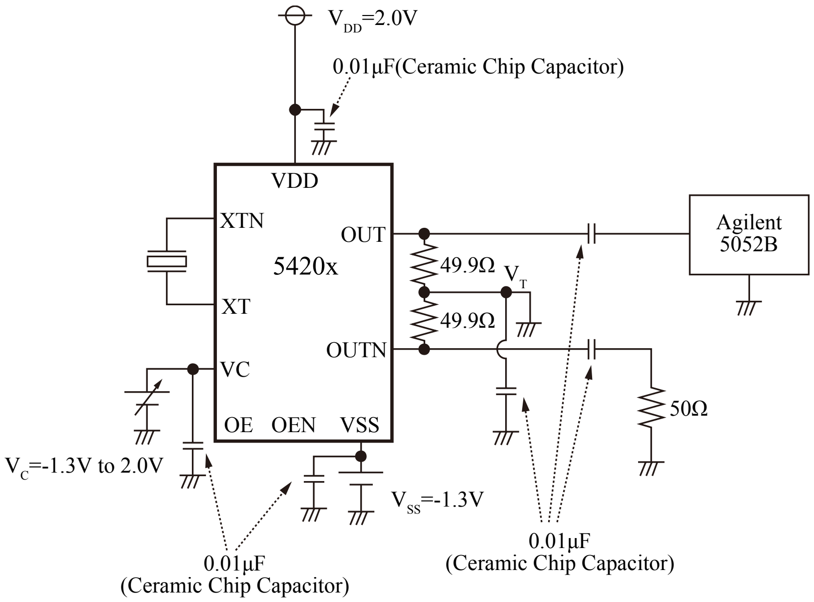
[5420C] f_{OSC}=155.52MHz



[5420D] f_{OSC}=245.76MHz

(TBD)

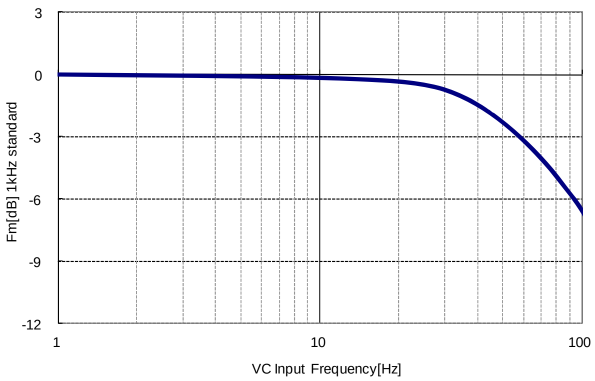
[Measurement circuit diagram]



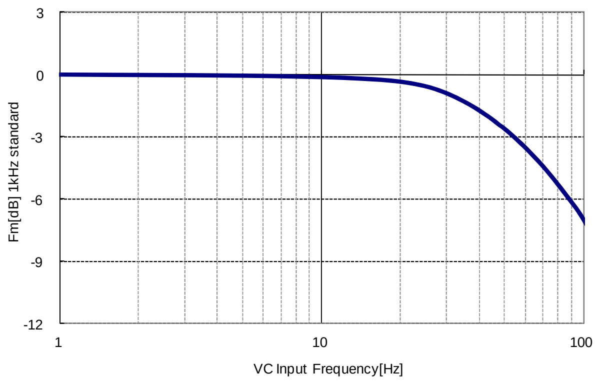
Modulation Bandwidth

[Measurement conditions] V_{DD}= +2.0V, V_{SS}= -1.3V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



[5420C] f_{OSC}=155.52MHz



[5420D] f_{OSC}=245.76MHz

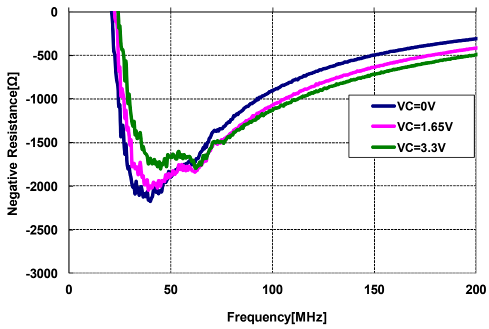
(TBD)

[Measurement circuit diagram] Measurement circuit 9

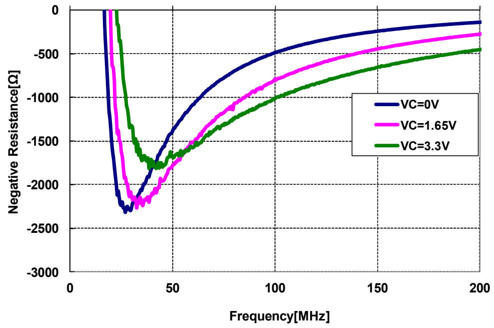
Negative Resistance

[Measurement conditions] V_{DD}= +3.3V, T_a= -25°C, C_0= 0pF

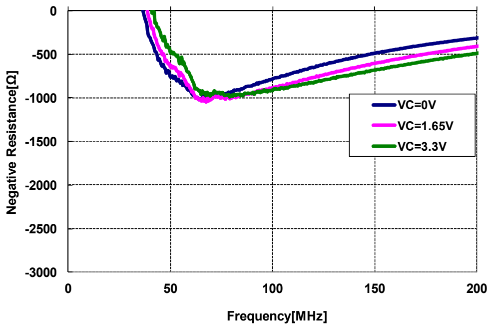
[5420B] When in "Boot" function



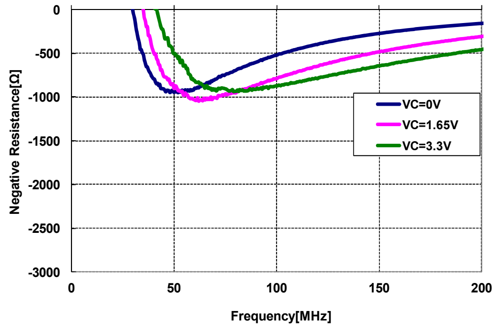
[5420B] After release "Boot" function



[5420C] When in "Boot" function



[5420C] After release "Boot" function



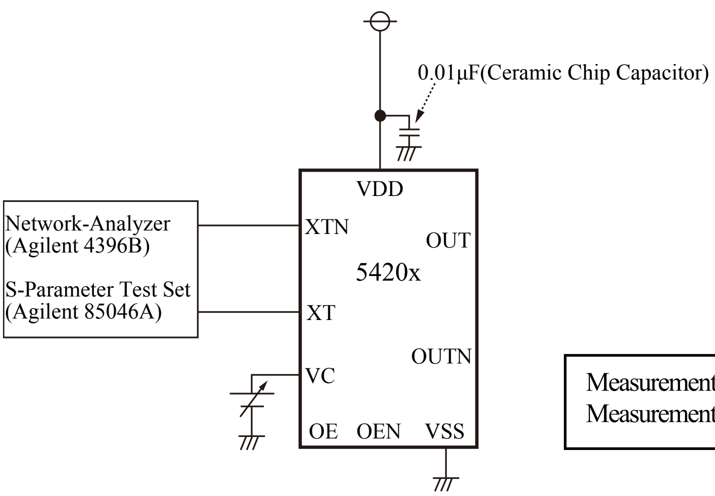
[5420D] When in "Boot" function

(TBD)

[5420D] After release "Boot" function

(TBD)

[Measurement circuit diagram]

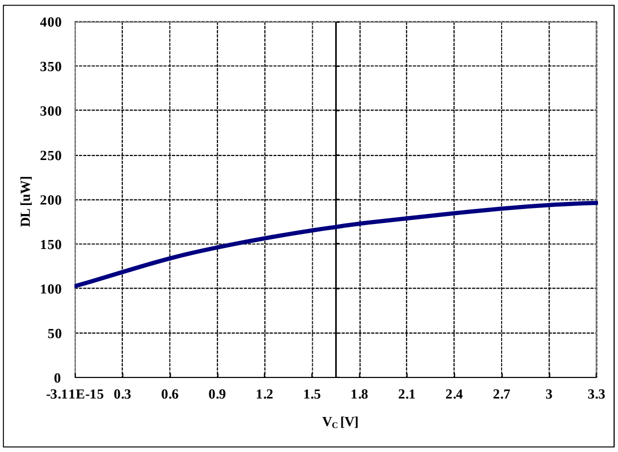


Measurement results using 4396B Agilent analyzer on NPC test jig.
Measurements will vary with test jig and measurement environment.

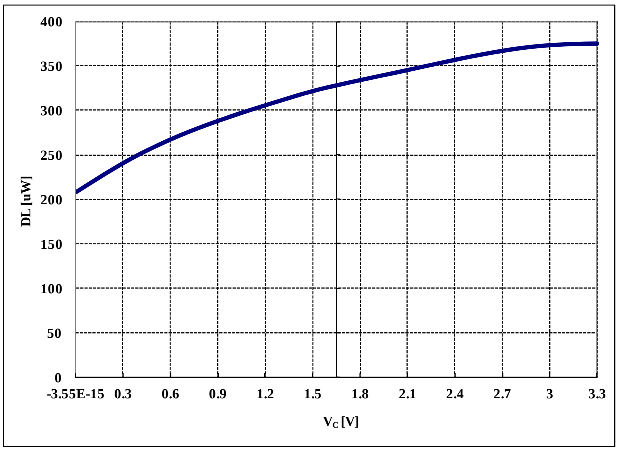
Drive Level

[Measurement conditions] V_{DD}= +3.3V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



[5420C] f_{OSC}=155.52MHz

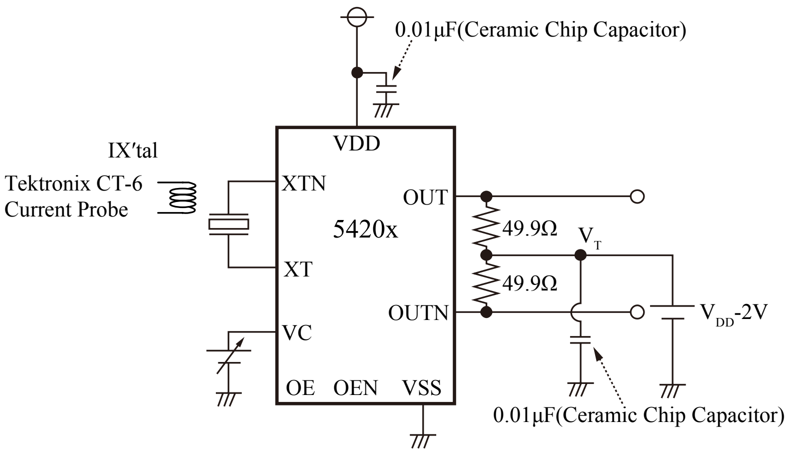


* V_C voltage in the graphs is adjusted to V_{SS}= 0V.

[5420D] f_{OSC}=245.76MHz

(TBD)

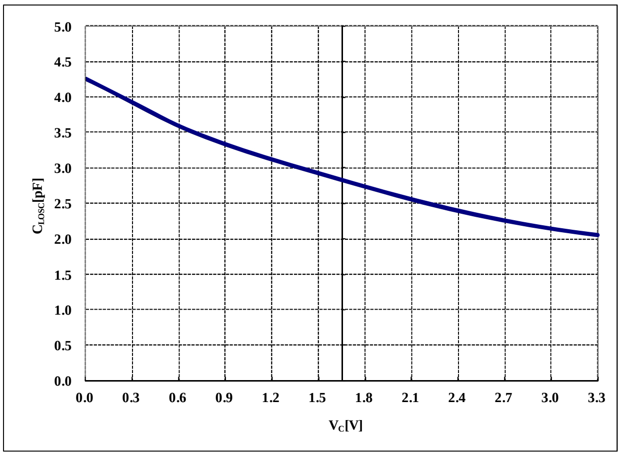
[Measurement circuit diagram]



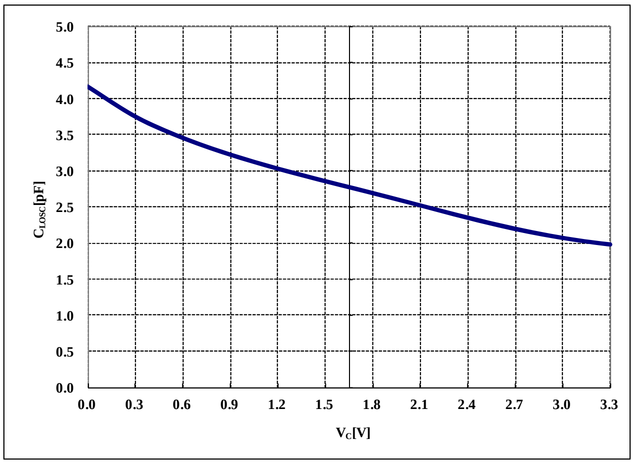
Oscillator CL Characteristics

[Measurement conditions] V_{DD}= +2.0V, V_{SS}= -1.3V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



[5420C] f_{OSC}=155.52MHz

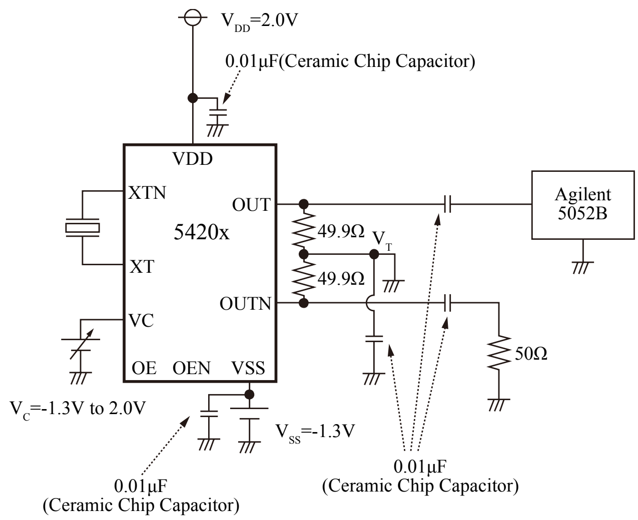


* V_C voltage in the graphs is adjusted to V_{SS}= 0V.

[5420D] f_{OSC}=245.76MHz

(TBD)

[Measurement circuit diagram]



CL_{OSC}: Oscillator circuit equivalent capacitance determined by oscillator frequency

$$CLosc = \frac{C_1}{\left(\frac{f_{OSC}}{fs}\right)^2 - 1} - C_0$$

C_1: Crystal element equivalent series capacitance

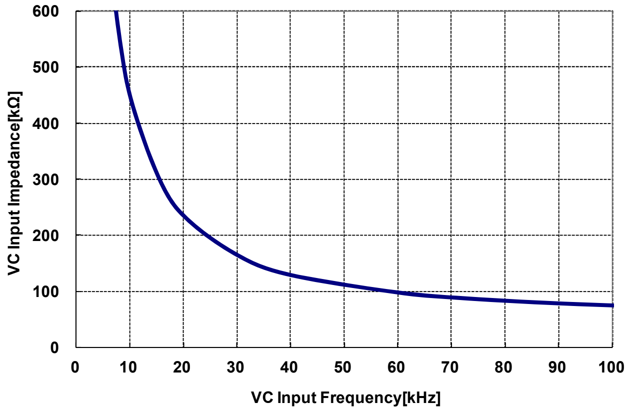
C_0: Crystal element equivalent parallel capacitance

fs: Crystal element series resonance frequency

VC Terminal Input Impedance

[Measurement conditions] T_a= +25°C, V_C= 0V

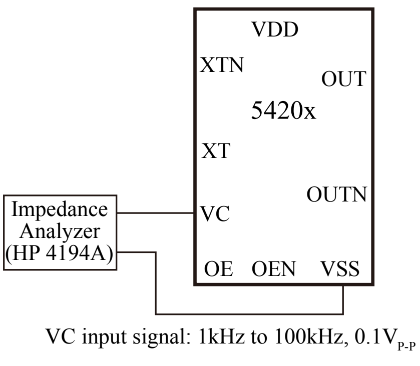
[5420B, C]



[5420D]

(TBD)

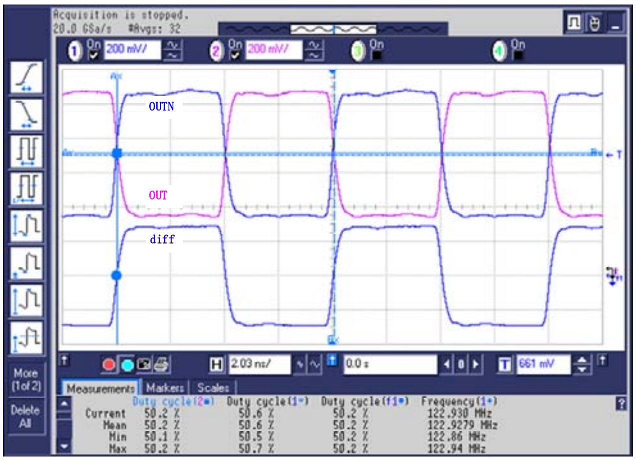
[Measurement circuit diagram]



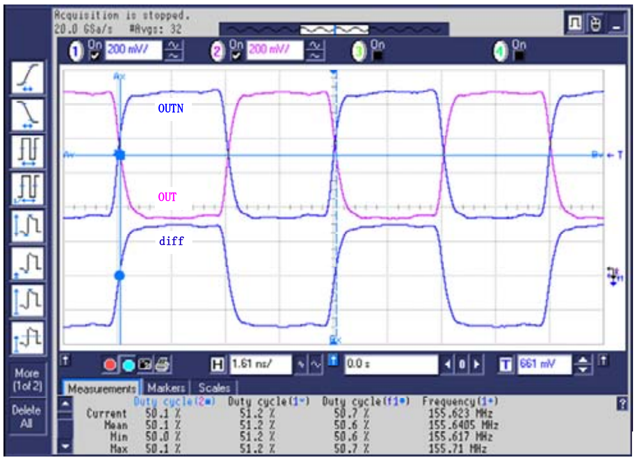
Output Waveform

[Measurement conditions] V_{DD}= +3.3V, V_C= +1.65V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



[5420C] f_{OSC}=155.52MHz



[5420D] f_{OSC}=245.76MHz

(TBD)

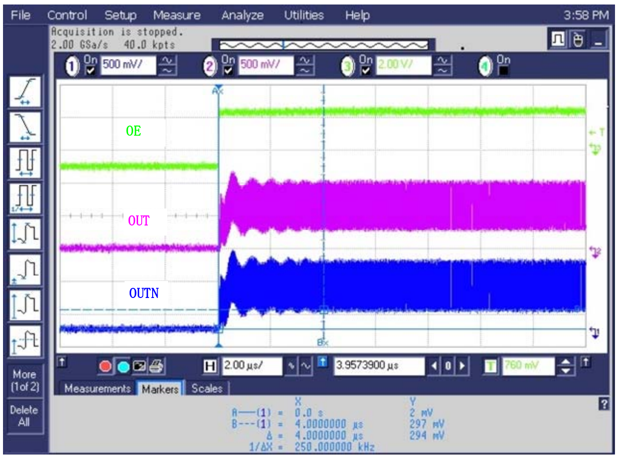
[Measurement circuit diagram] Measurement circuit 7

Measurement equipment: Oscilloscope DSO80604B (Agilent), Differential probe 1134A (Probe head E2678A)

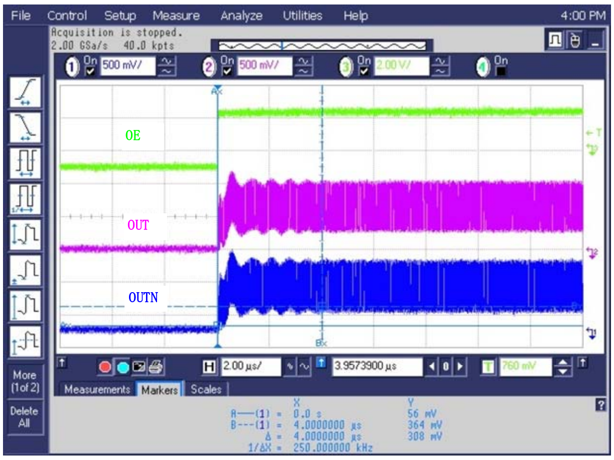
Output Enable Propagation Delay

[Measurement conditions] V_{DD}= +3.3V, V_C= +1.65V, T_a= +25°C

[5420B] f_{OSC}=122.88MHz



[5420C] f_{OSC}=155.52MHz



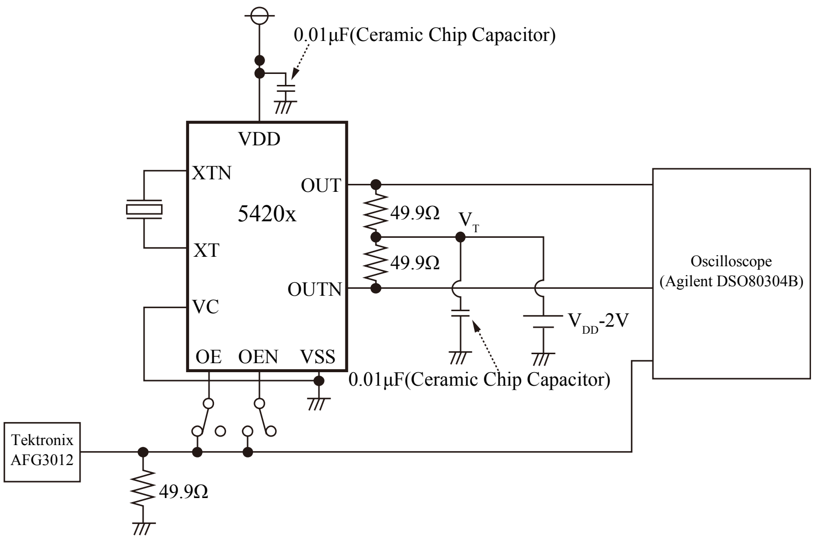
[5420D] f_{OSC}=245.76MHz

(TBD)

* t_{OE} is the time required for the output level to stabilize, and which varies depending on the power supply used, bypass capacitor values, and other factors.

Measurement equipment: Power supply voltage PW18-1.8AQYB (KENWOOD)

[Measurement circuit diagram]



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