OVERVIEW

5079 series is a 60 to 200MHz oscillator frequency, LVDS output, VCXO module IC.

It incorporates a bipolar oscillator circuit and a newly developed varicap diode built-in for low phase noise characteristic and wide frequency pulling range.

FEATURES

- VCXO with varicap diode built-in
- Output Type: Differential LVDS
- Oscillator: Fundamental frequency oscillation
- Output frequency (f_{OUT}): 60 to 200MHz
- Oscillator frequency: 60 to 100MHz (5079A1, AP version)
  100 to 170MHz (5079B1, BP version)
  150 to 200MHz (5079C1 version)
- Operating supply voltage range: 2.375 to 2.625V (5079xP version), 2.97 to 3.63V (5079x1 version)
- -40 to +105°C operating temperature range
- Output enable (OE) active selectable function: Selectable Hi-Active or Low-Active by bonding wire
- Wide frequency pulling range (typ): ±130ppm@B1 version, V_C=1.65±1.65V, f_{OUT}=122.88MHz (γ=330, C_0=1.6pF)
- Low phase noise (typ): -125dBc/Hz@B1 version, 1kHz Offset, f_{OUT}=122.88MHz (γ=330, C_0=1.6pF)
  -160dBc/Hz@B1 version, 10MHz Offset, f_{OUT}=122.88MHz

APPLICATIONS

Base station, SONET/SDH, Ethernet, Fibre Channel, LTE

SERIES CONFIGURATION

Recommended operating frequency range (f_{OSC})*1 [MHz]	Version Name	Operating supply voltage (V_{DD})
60 ～ 100	5079A1	3.3±10%
	5079AP	2.5±5%
100 ～ 170	5079B1	3.3±10%
	5079BP	2.5±5%
150 ～ 200	5079C1	3.3±10%

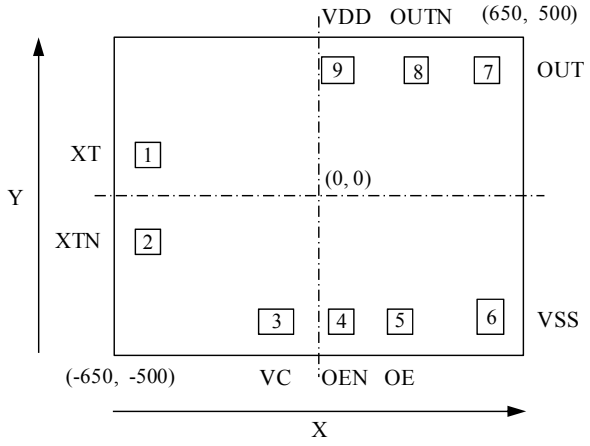
*1. Recommended values based on IC characteristics.
The oscillator characteristics are determined by the combination of crystal element and the IC,
hence the actual oscillator is not limited to these values. Always conduct thorough circuit evaluation beforehand.
The recommended characteristics for the crystal element are R_1 < 20Ω, C_0 < 1.5pF.

ORDERING INFORMATION

Device	Package	Version name
WF5079xx-4	Wafer form	WF5079□□-4 Form WF: Wafer form CF: Chip (Die) form Output frequency 1, P: f_{OSC} 2, Q: f_{OSC}/2 Oscillation frequency A: 60～100MHz B:100～170MHz C:150～200MHz
CF5079xx-4	Chip form	

PAD LAYOUT

(Unit: µm)



Chip size[*1]: 1.3mm×1.0mm

*1. Chip size is the distance between the scribe line centers.

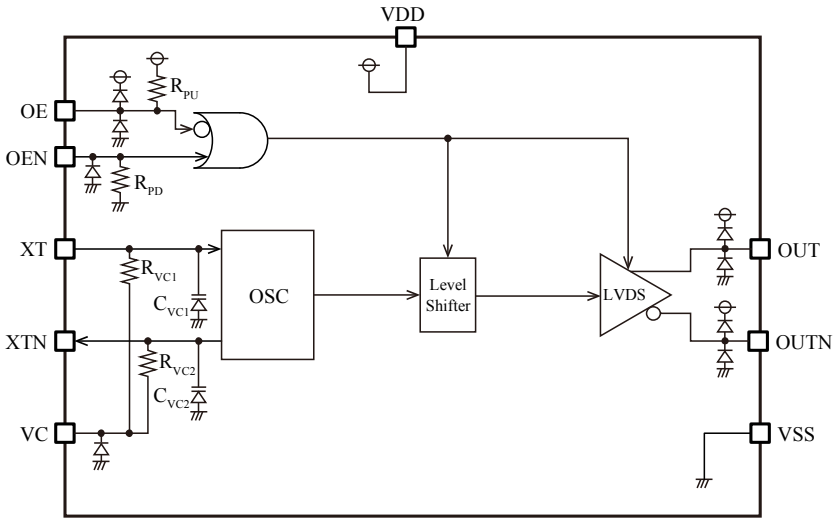
Chip thickness: 130µm

PAD size: 80µm × 80µm (PAD No. 1, 2, 4, 5,7,8 pins)
110µm × 80µm (PAD No. 3, 9 pins)
80µm × 110µm (PAD No. 6 pins)

Chip base: VSS potential

* The origin at chip center is pad coordinate (0, 0) .

BLOCK DIAGRAM



PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O[*1]	Description	Pad Coordinates (Unit : µm)	
				X	Y
1	XT	I	Crystal element connection terminals.	-545.0	129.8
2	XTN	O		-545.0	-145.2
3	VC	I	Control voltage input.	-135.2	-395.0
4	OEN	I	Output enable input. With pull-down built-in. Refer to page 11 OEN function.	67.6	-395.0
5	OE	I	Output enable input. With pull-up built-in. Refer to page 11 for OE function.	255.4	-395.0
6	VSS	-	Ground	545.0	-380.0
7	OUT	O	Clock output (differential output), Stand-by state: Hi-Z	531.9	395.0
8	OUTN	O	Clock output (differential inverted output), Stand-by state: Hi-Z	307.7	395.0
9	VDD	-	Supply voltage	61.4	395.0

*1.I: input, O: output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range*1	V_{DD}	VDD pins	-0.3 to +5.0	V
Input voltage range*1*2	V_{IN}	XT, OE, OEN, VC pins	-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	XTN, OUT, OUTN pins	-0.3 to V_{DD}+0.3	V
Junction temperature*3	T_j		+125	°C
Storage temperature range*4	T_{STG}	Wafer, Chips	-55 to +125	°C

*1. Parameters must not exceed ratings, not even momentarily. If a rating is exceeded, there is a risk of IC failure, deterioration in characteristics, and decrease in reliability.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. Parameter should not exceed rating. If a rating is exceeded, there is a risk of deterioration in characteristics and decrease in reliability.

*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating supply voltage	V_{DD}	Between VDD and VSS pins*2	x1 version	2.97	3.3	3.63	V
			xP version	2.375	2.5	2.625	V
Input voltage	V_{IN}	OE, OEN, VC pins		0	-	V_{DD}	V
Operating temperature	T_a			-40	-	+105	°C
Output load	R_L	Between OUT and OUTN		99	100	101	Ω
Oscillator frequency*1	f_{OSC}	5079A1, AP version		60	-	100	MHz
		5079B1, BP version		100	-	170	
		5079C1 version		150	-	200	
Output frequency*1	f_{OUT}	5079A1, AP version		60	-	100	MHz
		5079B1, BP version		100	-	170	
		5079C1 version		150	-	200	

*1. The characteristics will vary greatly depending on the crystal element characteristics and mounting conditions. Use only after thorough evaluation of the oscillator characteristics.

*2. For stable device operation, connect 0.01μF or larger ceramic chip capacitors between VDD and VSS, mounted as close as possible to the IC (within approximately 3mm). Also, use as thick a wiring pattern as possible between the IC and the capacitors.

Note. Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

Electrical Characteristics

A1, B1, C1 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Current consumption 1 (A1 version)	I_{DD1}	Measurement circuit 1, OE/OEN=Open, f_{OSC}= 77.76MHz	V_{DD}=3.3V	-	16	24	mA
Current consumption 1 (B1 version)		Measurement circuit 1, OE/OEN=Open, f_{OSC}= 122.88MHz	V_{DD}=3.3V	-	17	27	
Current consumption 1 (C1 version)		Measurement circuit 1, OE/OEN=Open f_{OSC}= 155.52MHz	V_{DD}=3.3V	-	20	30	
Current consumption 2 (A1 version)	I_{DD2}	Measurement circuit 1, OE=LOW or OEN=HIGH, oscillator operating, outputs disabled		-	1.2	2.5	mA
Current consumption 2 (B1 version)				-	2.1	3.5	
Current consumption 2 (C1 version)				-	3.5	5.0	
HIGH-level output voltage (DC level)	V_{OH}	Measurement circuit 2 OUT/OUTN		-	1.43	1.60	V
LOW-level output voltage (DC level)	V_{OL}	Measurement circuit 2 OUT/OUTN		0.90	1.10	-	V
Differential output voltage	V_{OD}	Measurement circuit 2, OUT/OUTN		247	350	454	mV
Differential output voltage error	ΔV_{OD}	Measurement circuit 2		-	-	50	mV
Offset voltage	V_{OS}	Measurement circuit 2, at the midpoint between OUT and OUTN		1.125	1.250	1.375	V
Offset voltage error	ΔV_{OS}	Measurement circuit 2		-	-	50	mV
Output leakage current	I_Z	Measurement circuit 4, SW1/2=HIGH or LOW, OE=LOW or OEN=HIGH, OUT/OUTN, T_a=25°C		-1	-	1	µA
HIGH-level input voltage	V_{IH}	Measurement circuit 3, OE/OEN		0.7V_{DD}	-	-	V
LOW-level input voltage	V_{IL}	Measurement circuit 3, OE/OEN		-	-	0.3V_{DD}	V
Pull-up resistance	R_{PU}	Measurement circuit 3, OE		50	100	200	kΩ
Pull-down resistance	R_{PD}	Measurement circuit 3, OEN		50	100	200	kΩ
Oscillator internal resistance*1	R_{VC1}	Between VC-XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC-XTN, measurement circuit 5		100	200	300	
Input leakage resistance*1	R_{VIN}	VC, T_a=25°C, measurement circuit 6		10	-	-	MΩ

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC-XT or VC-XTN
Input leakage resistance: Resistance between VC-VDD or VC-VSS (DC characteristic)
Refer to "VC Terminal Input Impedance". (Page. 23)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Maximum modulation frequency (A1 version)	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=3.3V, V_C=1.65 ± 1.65V, measurement circuit 9, f_{OSC}=77.76MHz		20	50	-	kHz
Maximum modulation frequency (B1 version)	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=3.3V, V_C=1.65 ± 1.65V, measurement circuit 9, f_{OSC}=122.88MHz		20	50	-	kHz
Maximum modulation frequency (C1 version)	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=3.3V, V_C=1.65 ± 1.65V, measurement circuit 9, f_{OSC}=155.52MHz		20	50	-	kHz
Oscillator capacitance (A1 version)	C_{VC1}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0.3V	5.88	6.53	7.18	pF
			V_C=1.65V	3.51	4.13	4.75	
			V_C=3.0V	1.80	2.25	2.70	
	C_{VC2}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0.3V	8.82	9.80	10.78	pF
			V_C=1.65V	5.27	6.20	7.13	
			V_C=3.0V	2.70	3.38	4.06	
Oscillator capacitance (B1 ver. C1 ver.)	C_{VC1}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0.3V	3.92	4.36	4.80	pF
			V_C=1.65V	2.35	2.76	3.17	
			V_C=3.0V	1.20	1.50	1.80	
	C_{VC2}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0.3V	5.88	6.53	7.18	pF
			V_C=1.65V	3.51	4.13	4.75	
			V_C=3.0V	1.80	2.25	2.70	

AP, BP version

V_{DD}=2.375 to 2.625V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Current consumption 1 (AP version)	I_{DD1}	Measurement circuit 1, OE/OEN=Open, f_{OSC}= 77.76MHz	V_{DD}=2.5V	-	13	19	mA
Current consumption 1 (BP version)		Measurement circuit 1, OE/OEN=Open, f_{OSC}= 122.88MHz	V_{DD}=2.5V	-	16	23	
Current consumption 2 (AP version)	I_{DD2}	Measurement circuit 1, OE=LOW or OEN=HIGH, oscillator operating, outputs disabled		-	1.8	3.6	mA
Current consumption 2 (BP version)				-	2.4	4.8	
HIGH-level output voltage (DC level)	V_{OH}	Measurement circuit 2 OUT/OUTN		-	1.43	1.60	V
LOW-level output voltage (DC level)	V_{OL}	Measurement circuit 2 OUT/OUTN		0.90	1.10	-	V
Differential output voltage	V_{OD}	Measurement circuit 2, OUT/OUTN		247	350	454	mV
Differential output voltage error	ΔV_{OD}	Measurement circuit 2		-	-	50	mV
Offset voltage	V_{OS}	Measurement circuit 2, OUT/OUTN at the midpoint between OUT and OUTN		1.125	1.250	1.375	V
Offset voltage error	ΔV_{OS}	Measurement circuit 2		-	-	50	mV
Output leakage current	I_Z	Measurement circuit 4, SW1/2=HIGH or LOW, OE=LOW or OEN=HIGH, OUT/OUTN, T_a= +25°C		-1	-	1	µA
HIGH-level input voltage	V_{IH}	Measurement circuit 3, OE/OEN		0.7V_{DD}	-	-	V
LOW-level input voltage	V_{IL}	Measurement circuit 3, OE/OEN		-	-	0.3V_{DD}	V
Pull-up resistance	R_{PU}	Measurement circuit 3, OE		50	100	200	kΩ
Pull-down resistance	R_{PD}	Measurement circuit 3, OEN		50	100	200	kΩ
Oscillator internal resistance*1	R_{VC1}	Between VC-XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC-XTN, measurement circuit 5		100	200	300	
Input leakage resistance*1	R_{VIN}	VC, T_a=25°C, measurement circuit 6		10	-	-	MΩ

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC-XT or VC-XTN
Input leakage resistance: Resistance between VC-VDD or VC-VSS (DC characteristic)
Refer to "VC Terminal Input Impedance". (Page. 23)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Maximum modulation frequency (AP version)	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=2.5V, V_C=1.25 ± 1.25V, measurement circuit 9, f_{OSC}=77.76MHz		20	47	-	kHz
Maximum modulation frequency (BP version)	F_M	-3dB frequency, T_a=25°C, design value, V_{DD}=2.5V, V_C=1.25 ± 1.25V, measurement circuit 9, f_{OSC}=122.88MHz		20	40	-	kHz
Oscillator capacitance (AP version)	C_{VC1}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0V	6.6	7.5	8.2	pF
			V_C=1.25V	3.9	4.7	5.4	
			V_C=2.5V	2.3	2.9	3.5	
	C_{VC2}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0V	9.9	11.2	12.3	pF
			V_C=1.25V	5.8	7.0	8.1	
			V_C=2.5V	3.5	4.4	5.3	
Oscillator capacitance (BP version)	C_{VC1}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0V	5.0	5.6	6.1	pF
			V_C=1.25V	3.1	3.5	3.9	
			V_C=2.5V	1.8	2.2	2.6	
	C_{VC2}	Confirmed using wafer monitor pattern, design value, excluding parasitic capacitance	V_C=0V	7.2	8.1	8.9	pF
			V_C=1.25V	4.5	5.1	5.6	
			V_C=2.5V	2.7	3.2	3.7	

Switching Characteristics

A1, B1, C1 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Duty cycle	Duty	Measurement circuit 7,Measured at 0V crossover point of differential output signal	45	-	55	%
Output amplitude	V_{OPP}	Measurement circuit 7, Differential output signal	0.4	-	-	V
Output rise time	t_r	Measurement circuit 7, Measured between 20% and 80% amplitude of differential output signal	-	0.4	0.7	ns
Output fall time	t_f	Measurement circuit 7, Measured between 80% and 20% amplitude of differential output signal	-	0.4	0.7	ns
Output enable propagation delay*1	t_{OE}	Measurement circuit 8, T_a= +25°C, design value,	-	-	20	µs
Output disable propagation delay	t_{OD}	Measurement circuit 8, T_a= +25°C, design value	-	-	200	ns

*1. Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.
Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.
The recommended crystal element characteristics are R_1 < 20Ω and C_0 < 1.5pF.

AP, BP version

V_{DD}=2.375 to 2.625V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Duty cycle	Duty	Measurement circuit 7,Measured at 0V crossover point of differential output signal	45	-	55	%
Output amplitude	V_{OPP}	Measurement circuit 7, Differential output signal	0.4	-	-	V
Output rise time	t_r	Measurement circuit 7, Measured between 20% and 80% amplitude of differential output signal	-	0.4	0.7	ns
Output fall time	t_f	Measurement circuit 7, Measured between 80% and 20% amplitude of differential output signal	-	0.4	0.7	ns
Output enable propagation delay*1	t_{OE}	Measurement circuit 8, Ta=25°C, design value	-	-	20	µs
Output disable propagation delay	t_{OD}	Measurement circuit 8, Ta=25°C, design value	-	-	200	ns

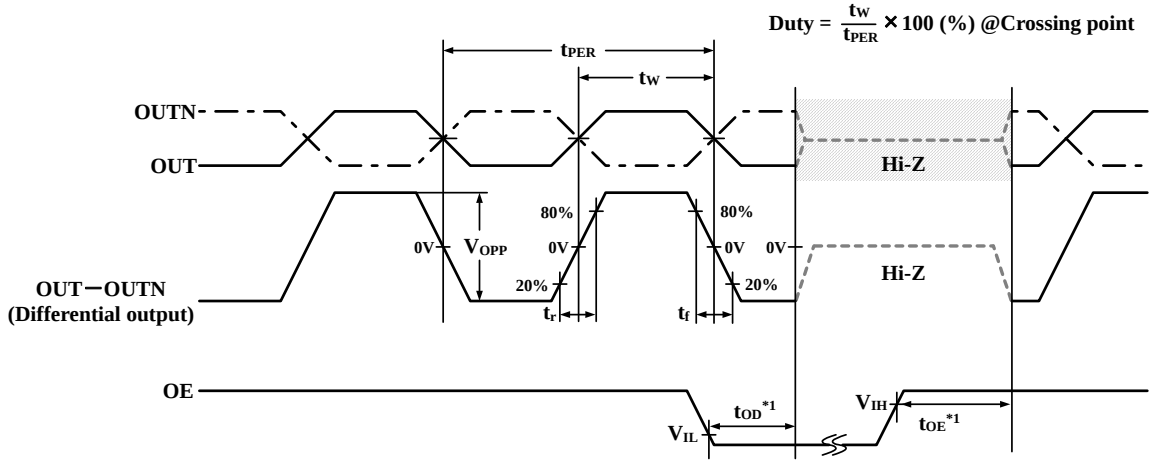
*1. Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

Notes

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.
Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.
The recommended crystal element characteristics are R_1 < 20Ω and C_0 < 1.5pF.

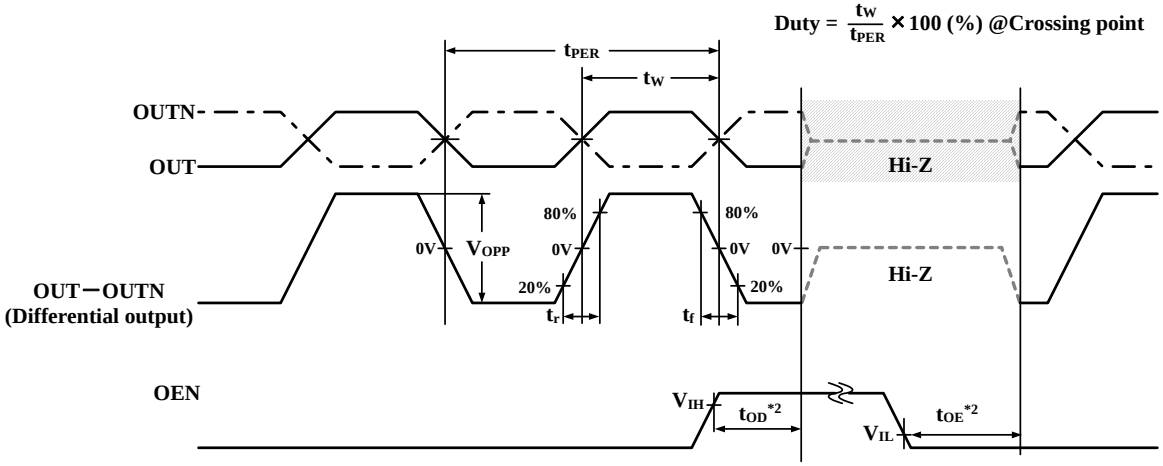
Timing chart

[Using OE]



*1. On an OE falling edge, the output signals become high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) time.
On an OE rising edge, the output signals become operating mode after the output enable propagation delay (t_{OE}) time.

[Using OEN]



*2. On an OEN rising edge, the output signals become high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) time.
On an OEN falling edge, the output signals become operating mode after the output enable propagation delay (t_{OE}) time.

FUNCTIONAL DESCRIPTION

OE Function

OE (pull-up resistance built-in)	OEN (pull-down resistance built-in)	Oscillator	Output stage
High/Open	Low/Open	Operating	Operating
LOW	Open	Operating	Disabled (Hi-Z)
Open	HIGH	Operating	Disabled (Hi-Z)
LOW	HIGH	Not used for normal operation. NPC test mode (V_{OH},V_{OL} measurement)	

Oscillation Start-up Detector Function

An oscillator startup detection circuit is built-in. The circuit disables the OUT/OUTN outputs (high impedance) until the oscillator starts. This function prevents unstable oscillation and other problems, which can occur when power is applied, from appearing at the output.

Boot Function

At the time of oscillation starting, XTN pin potential is made into the V_{DD} level. It makes negative resistance enlarged and it becomes easy to start oscillation. Beware that a current flows into VC pin until it starts oscillation, when XTN pin is V_{DD} level and the voltage below V_{DD} level is being applied to VC pin.

A boot function is canceled after an oscillation start.

MEASUREMENT CIRCUITS

These measurement circuits are used for the evaluation of the electrical and switching characteristics.

Notes:

Connect the bypass capacitors, specified in the measurement circuits, between VDD-VSS.

Connect the load resistors, specified in the measurement circuits, to the OUT and OUTN outputs (excluding measurement circuits 4, 5, and 6).

Connect the bypass capacitors and load resistors with wiring pattern as short as possible (less than 3mm length). If the wiring pattern is too long, the desired characteristics cannot be obtained.

Note that if bypass capacitors and load resistors other than the specified values are connected, or if the components are not connected at all, the desired characteristics cannot be obtained.

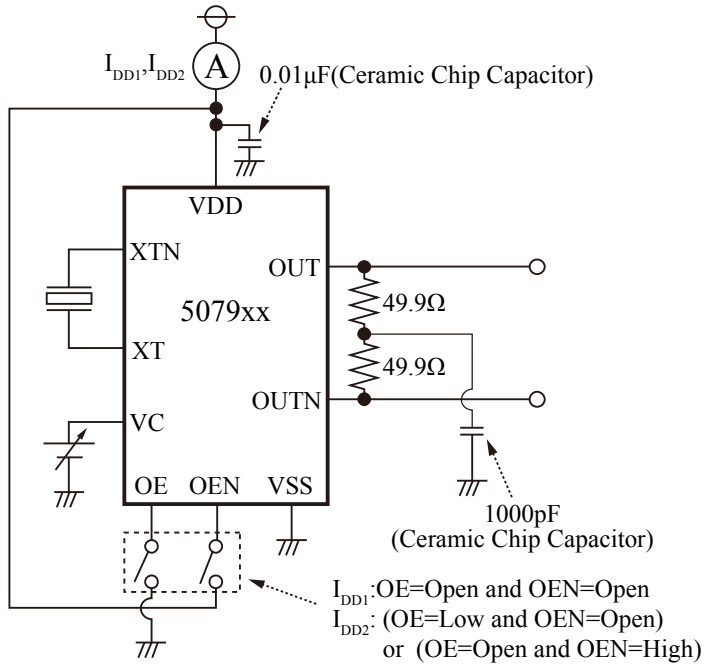
Capacitor and resistor values used by NPC

Capacitors: 0.01µF GRM188B11H103K (Murata Manufacturing Co., Ltd.)

Resistors: 49.9Ω RN732ATTD49R9B25 (KOA Corporation)

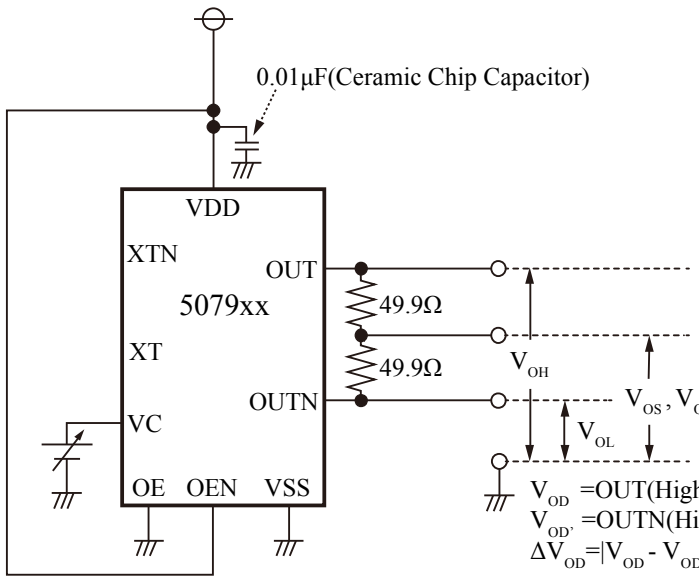
MEASUREMENT CIRCUIT 1

Measurement Parameters: I_{DD1}, I_{DD2}



MEASUREMENT CIRCUIT 2

Measurement Parameters: V_{OH}, V_{OL}, V_{OD}, V_{OS}



V_{OH}

V_{OS}, $V_{OS'}$

V_{OL}

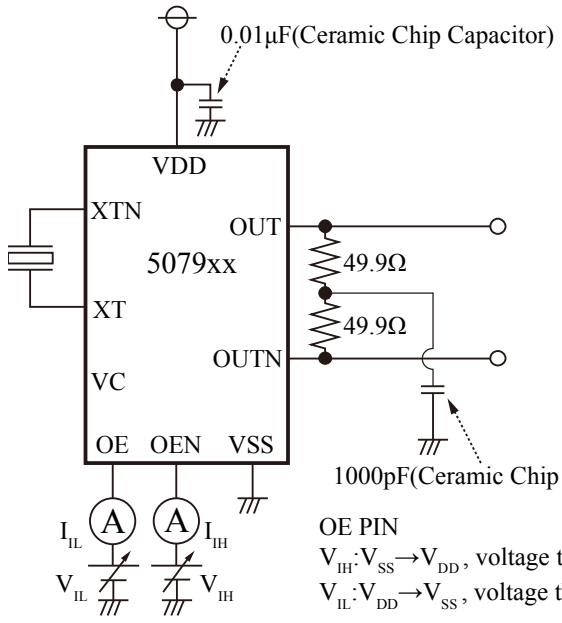
V_C = High:OUT=V_{OL}, OUTN=V_{OH}
V_C = Low:OUT=V_{OH}, OUTN=V_{OL}

V_{OD} =OUT(High) - OUTN(Low)
$V_{OD'}$ =OUTN(High) - OUT(Low)
ΔV_{OD}=|V_{OD} - $V_{OD'}$ |

V_{OS} =(OUT(High) + OUTN(Low))/2
$V_{OS'}$ =(OUT(Low) + OUTN(High))/2
ΔV_{OS}=|V_{OS} - $V_{OS'}$ |

MEASUREMENT CIRCUIT 3

Measurement Parameters: R_{PU}, R_{PD}, V_{IH}, V_{IL}



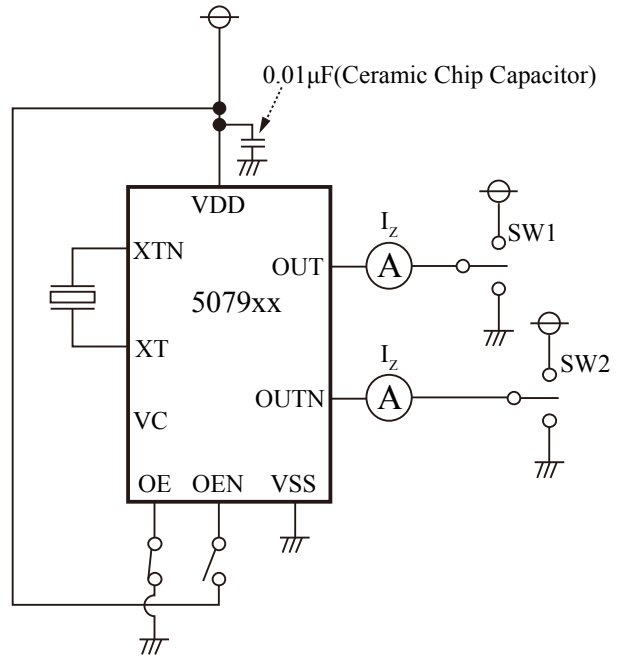
I_{IL} I_{IH} V_{IL} V_{IH}

OE PIN
V_{IH}:V_{SS}→V_{DD}, voltage that changes enable output state
V_{IL}:V_{DD}→V_{SS}, voltage that changes disable output state

OEN PIN
V_{IH}:V_{SS}→V_{DD}, voltage that changes disable output state
V_{IL}:V_{DD}→V_{SS}, voltage that changes enable output state

MEASUREMENT CIRCUIT 4

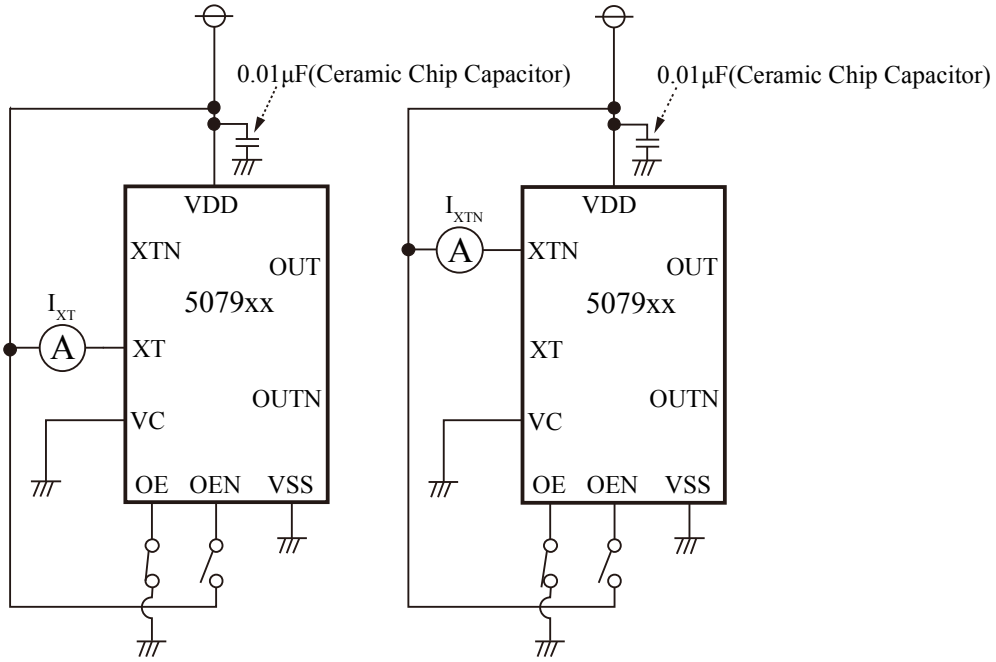
Measurement Parameters: I_Z



(OE=Low and OEN=Open) or (OE=Open and OEN=High)

MEASUREMENT CIRCUIT 5

Measurement Parameters: R_{VC1}, R_{VC2}



(OE=Low and OEN=Open) or (OE=Open and OEN=High)

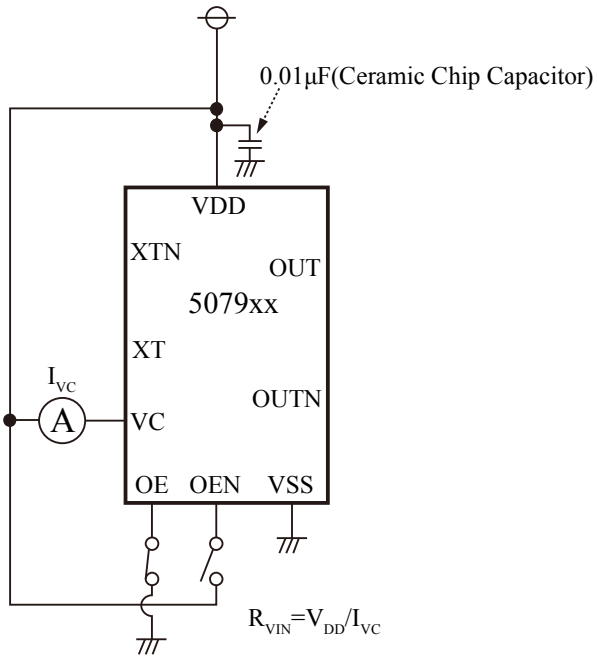
$R_{VC1}=V_{DD}/I_{XT}$

(OE=Low and OEN=Open) or (OE=Open and OEN=High)

$R_{VC2}=V_{DD}/I_{XTN}$

MEASUREMENT CIRCUIT 6

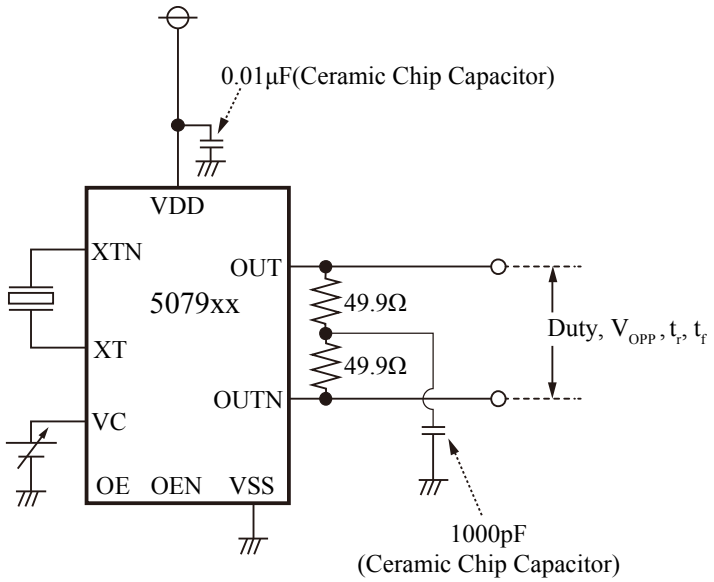
Measurement Parameters: R_{VIN}



(OE=Low and OEN=Open)
or (OE=Open and OEN=High)

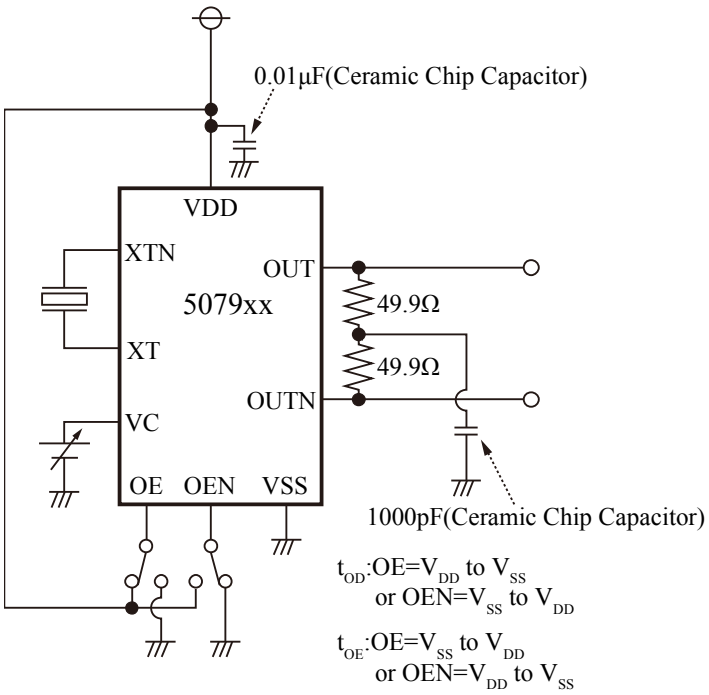
MEASUREMENT CIRCUIT 7

Measurement Parameters: Duty, V_{OPP}, t_r, t_f



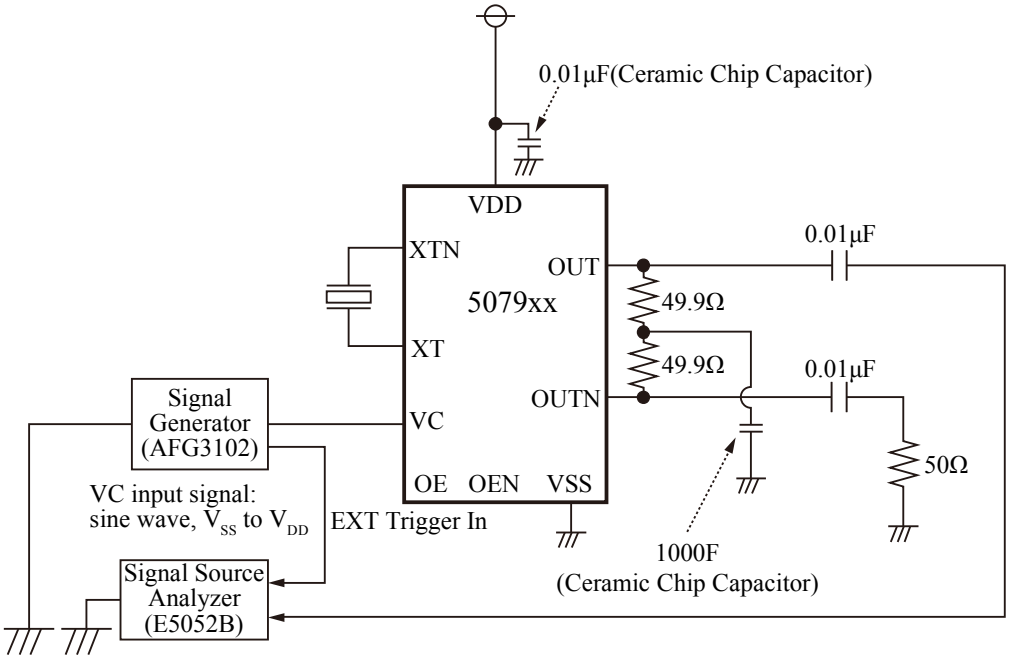
MEASUREMENT CIRCUIT 8

Measurement Parameters: t_{OE}, t_{OD}



MEASUREMENT CIRCUIT 9

Measurement Parameters: F_M



REFERENCE CHARACTERISTICS EXAMPLE (5079A1, B1, C1 Typical Characteristics)

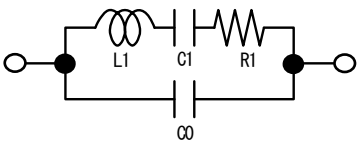
The characters given below were measured using an NPC standards jig and standard crystal element, and do not represent a guarantee of device characteristics.

Note that the characteristics will vary due to measurement environment and the oscillator element used.

Crystal used for measurement

Parameter	A	B	C
f_{OSC}(MHz)	77.76	122.88	155.52
C_0(pF)	2.7	1.6	1.5
$\gamma(=C_0/C_1)$	330	330	330
$R_1(\Omega)$	7	9	8

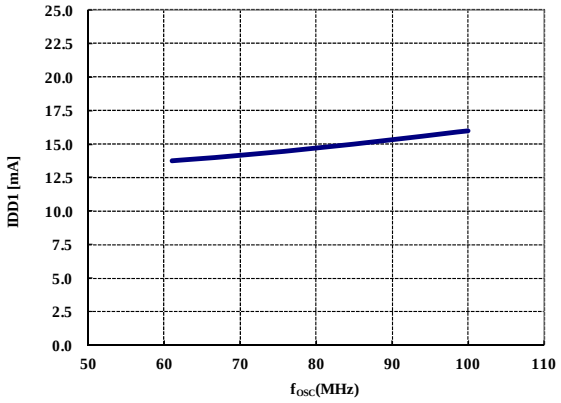
Crystal parameters



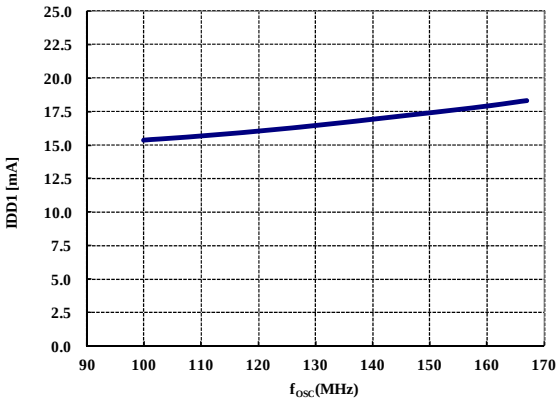
Current consumption 1

[Measurement conditions] V_{DD}= +3.3V, V_{SS}= 1.65V, T_a= +25°C

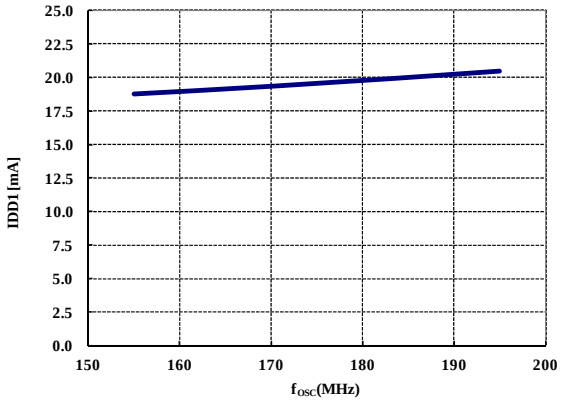
[5079A1]



[5079B1]



[5079C1]



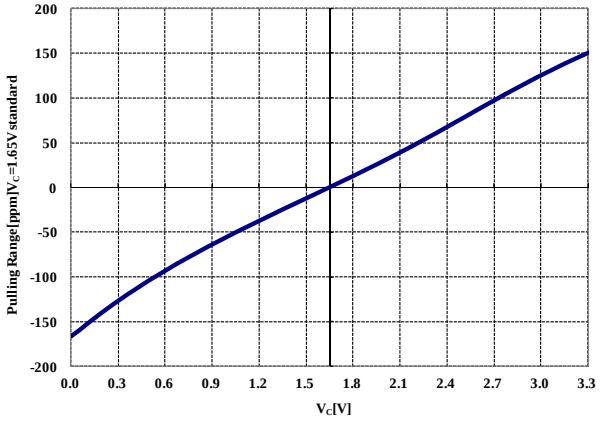
[Measurement circuit diagram]

Measurement circuit 1

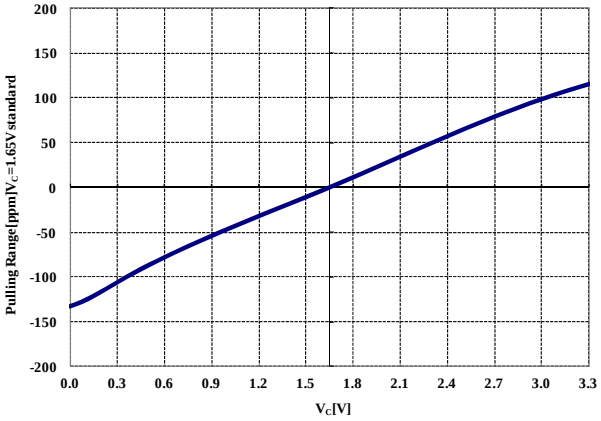
Pulling Range

[Measurement conditions] V_{DD}= +3.3V, T_a= +25°C

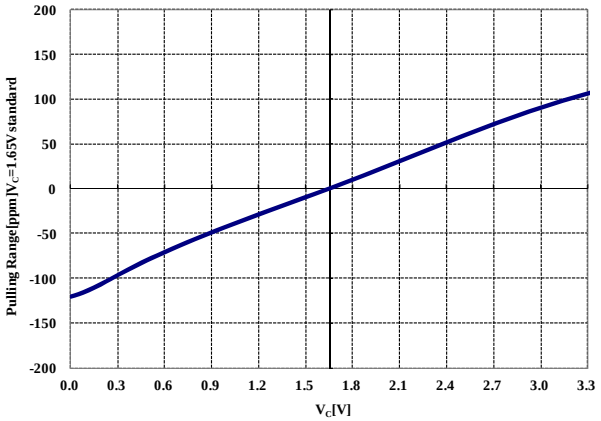
[5079A1] f_{OSC}=77.76MHz



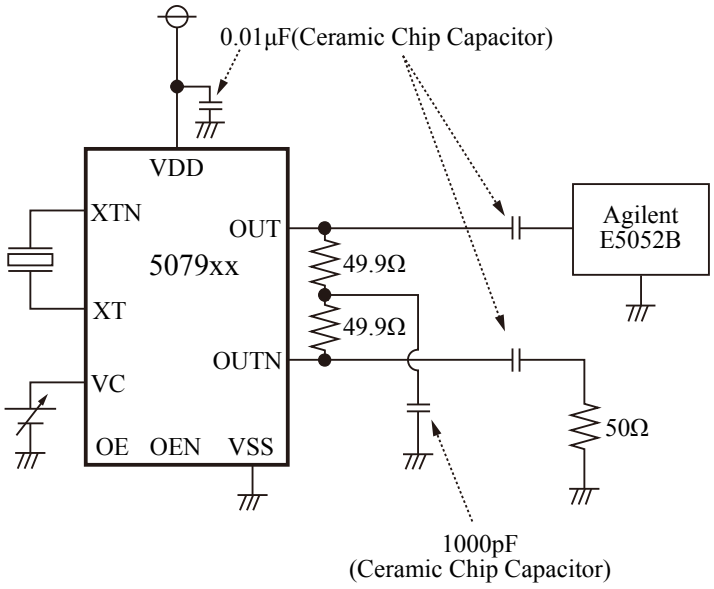
[5079B1] f_{OSC}=122.88MHz



[5079C1] f_{OSC}=155.52MHz



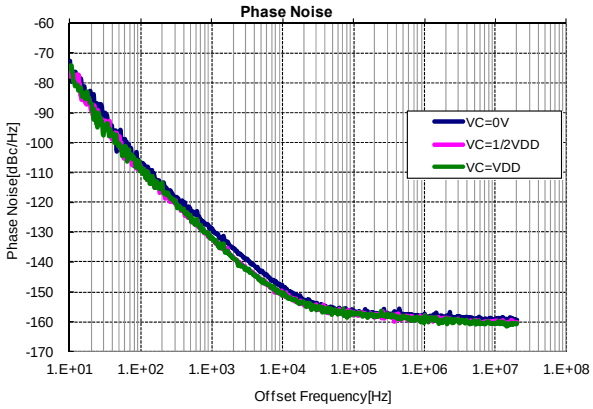
[Measurement circuit diagram]



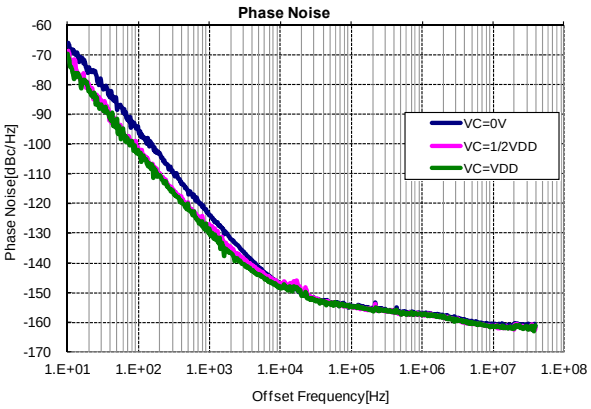
Phase Noise

[Measurement conditions] V_{DD}= +3.3V, T_a= +25°C

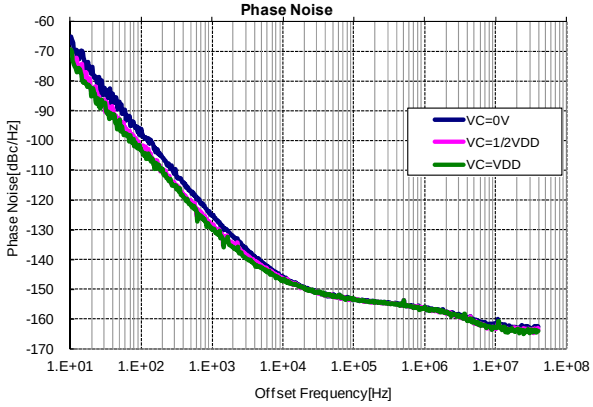
[5079A1] f_{OSC}=77.76MHz



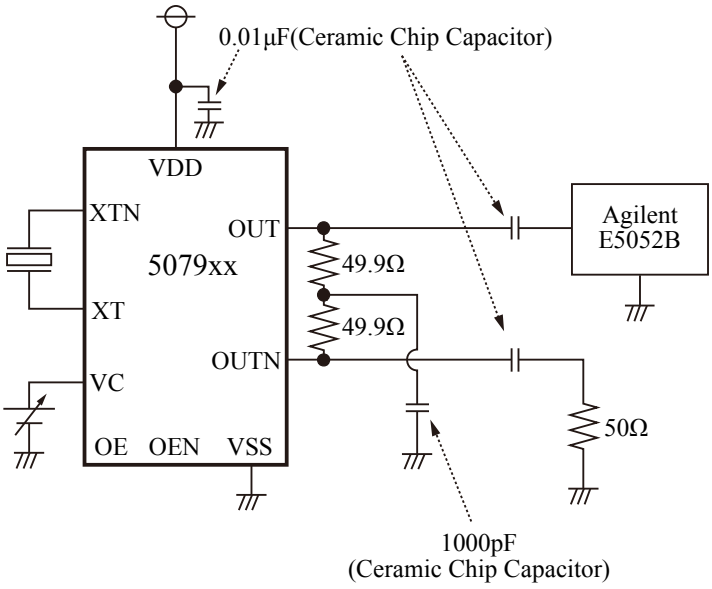
[5079B1] f_{OSC}=122.88MHz



[5079C1] f_{OSC}=155.52MHz



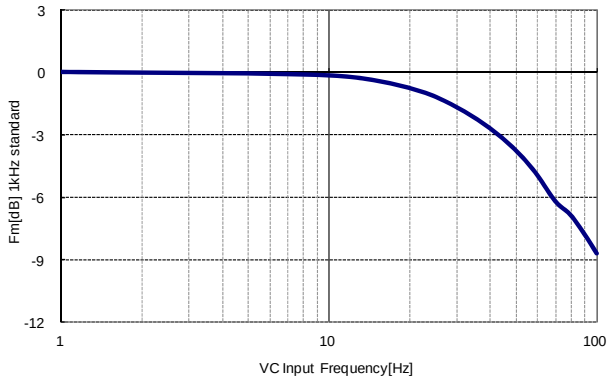
[Measurement circuit diagram]



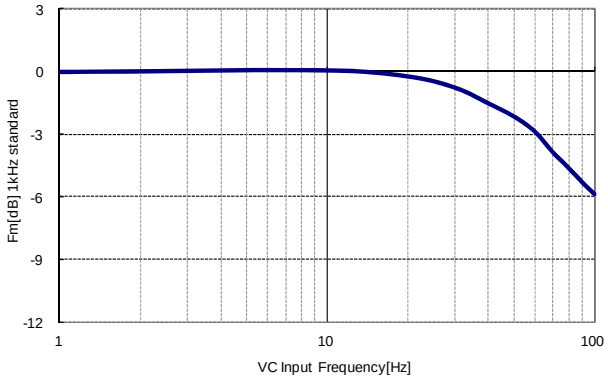
Modulation Bandwidth

[Measurement conditions] V_{DD}= +3.3V, T_a= +25°C

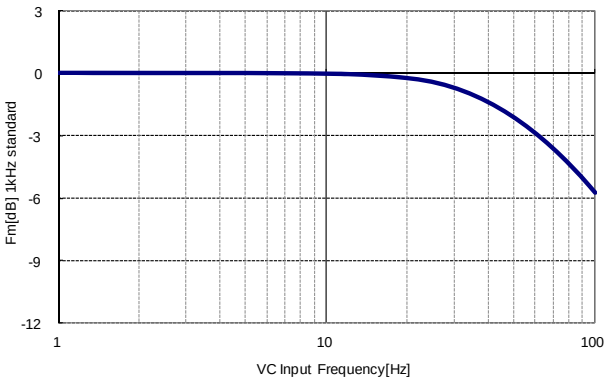
[5079A1] f_{OSC}=77.76MHz



[5079B1] f_{OSC}=122.88MHz



[5079C1] f_{OSC}=155.52MHz



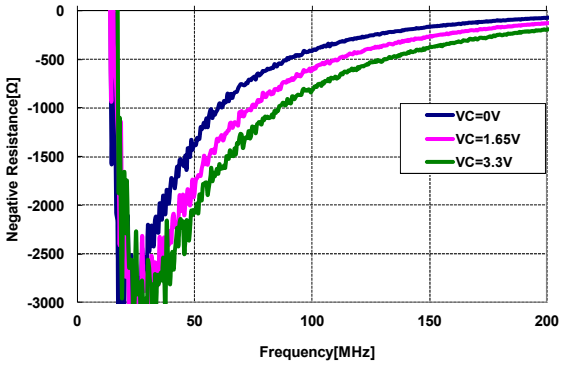
[Measurement circuit diagram]

Measurement circuit 9

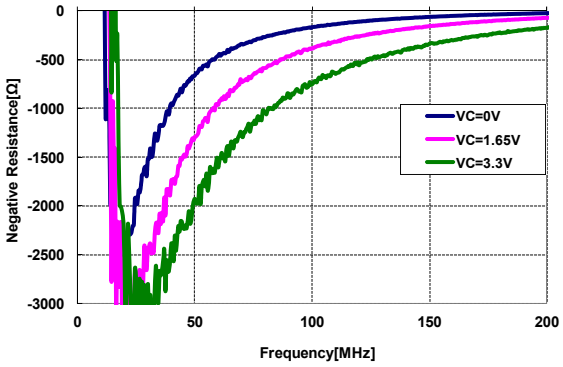
Negative Resistance

[Measurement conditions] V_{DD}= +3.3V, T_a= +25°C, C_0= 0pF

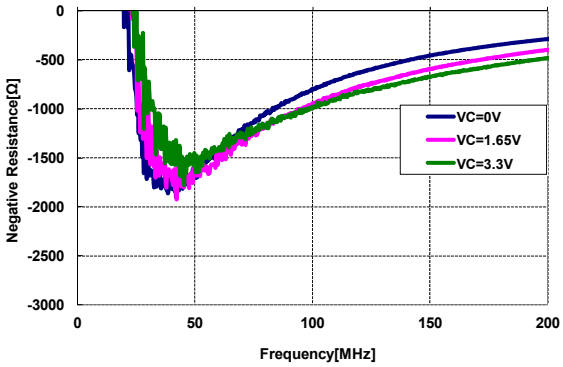
[5079A1] When in "Boot" function



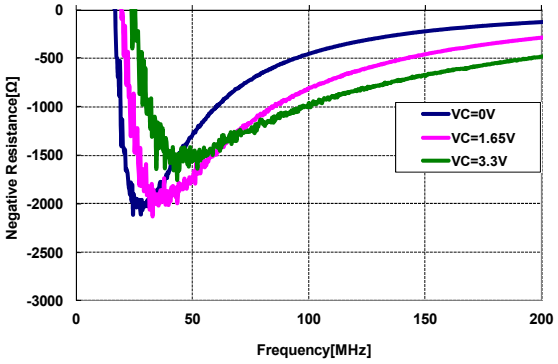
[5079A1] After release "Boot" function



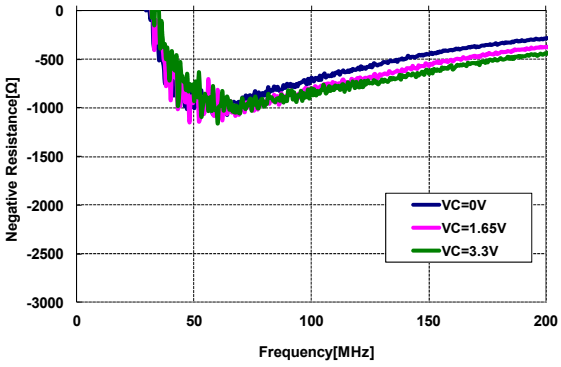
[5079B1] When in "Boot" function



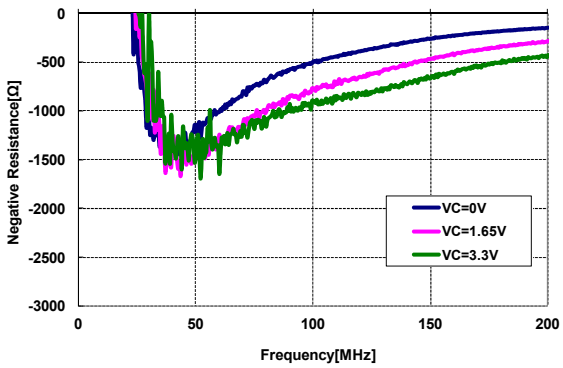
[5079B1] After release "Boot" function



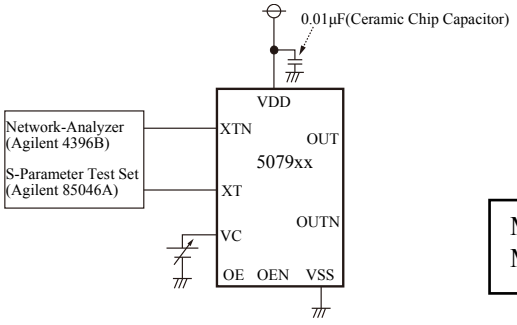
[5079C1] When in "Boot" function



[5079C1] After release "Boot" function



[Measurement circuit diagram]

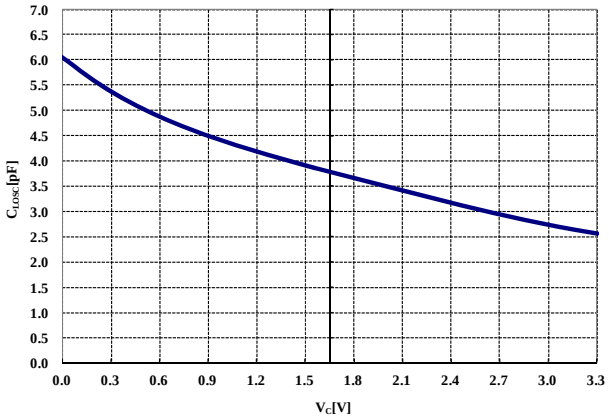


Measurement results using 4396B Agilent analyzer on NPC test jig.
Measurements will vary with test jig and measurement environment.

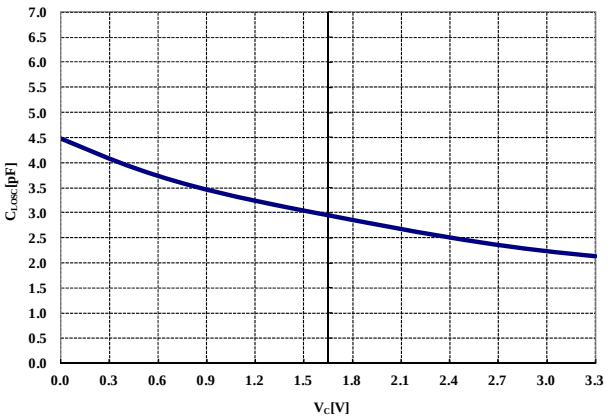
Oscillator CL Characteristics

[Measurement condition] V_{DD}=3.3V, Ta=+25℃

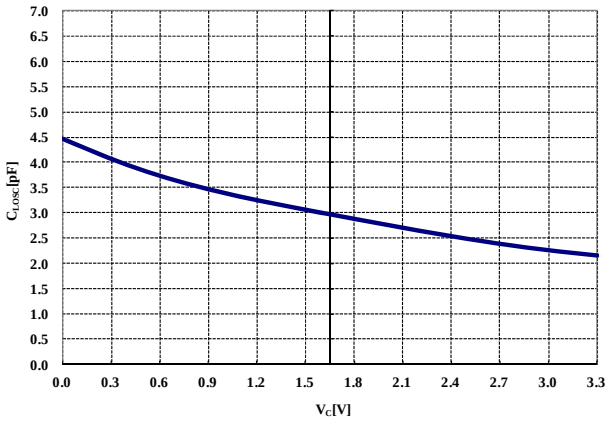
[5079A1] f_{OSC}=77.76MHz



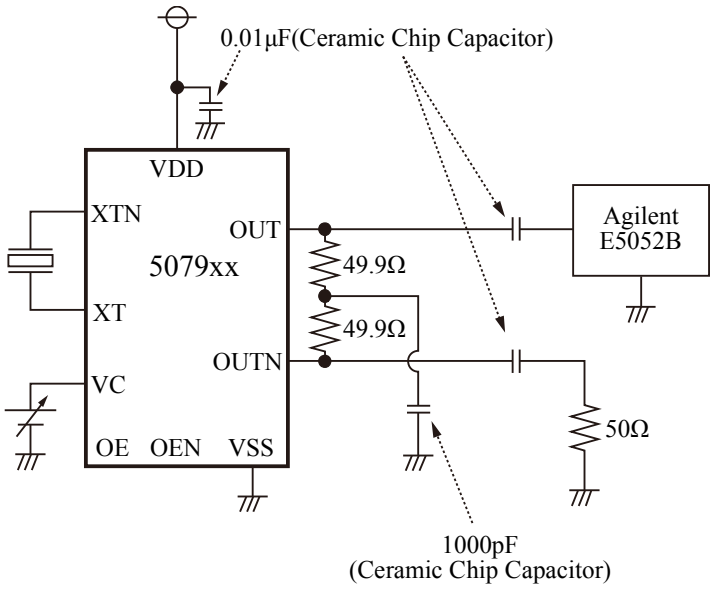
[5079B1] f_{OSC}=122.88MHz



[5079C1] f_{OSC}=155.52MHz



[Measurement circuit diagram]



CL_{OSC}: Oscillator circuit equivalent capacitance determined by oscillator frequency

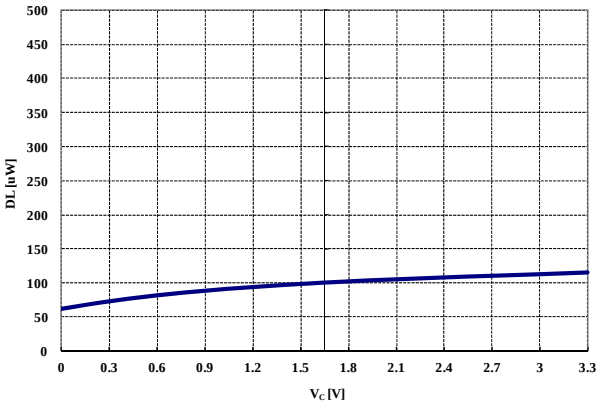
$$CLosc = \frac{C_1}{\left(\frac{f_{OSC}}{fs}\right)^2} - C_0$$

C_1: Crystal element equivalent series capacitance
C_0: Crystal element equivalent parallel capacitance
fs: Crystal element series resonance frequency

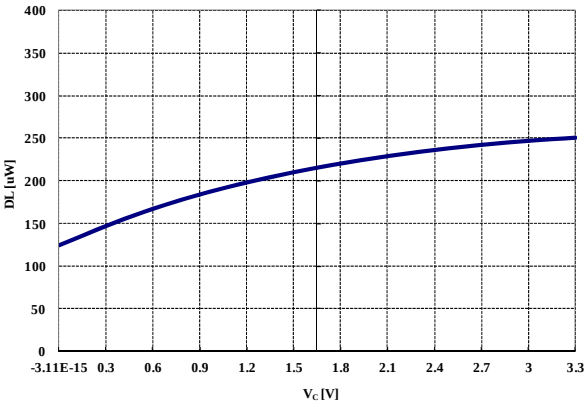
Drive Level

[Measurement conditions] V_{DD}= +3.3V, T_a= +25°C

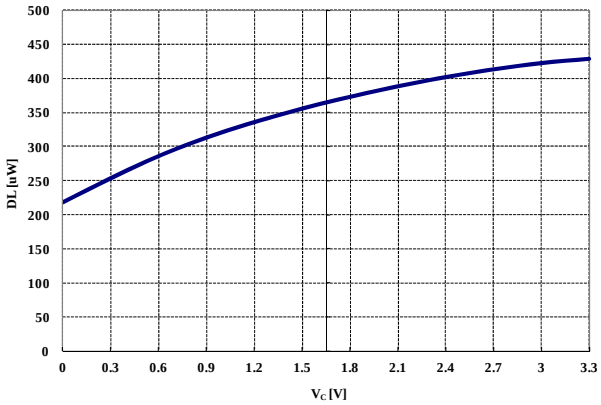
[5079A1] f_{OSC}=77.76MHz



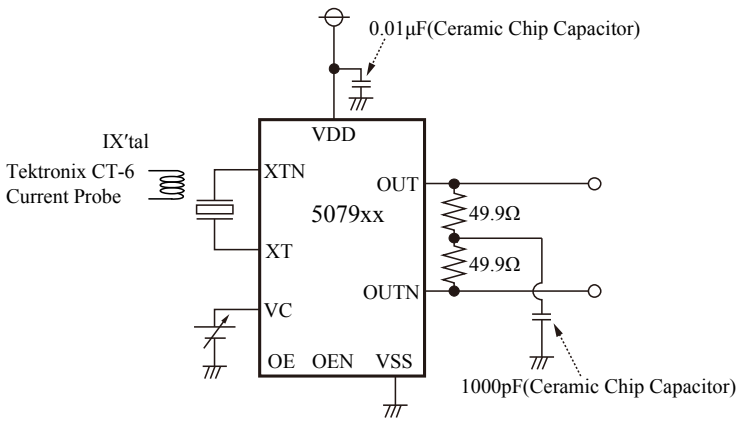
[5079B1] f_{OSC}=122.88MHz



[5079C1] f_{OSC}=155.52MHz



[Measurement circuit diagram]



$$DL = IXtal^2 \cdot Re$$

$$Re = R_1 \cdot \left(1 + \frac{C_0}{CLosc}\right)^2$$

CL_{OSC}: Oscillator circuit equivalent capacitance determined by oscillator frequency

$$CLosc = \frac{C_1}{\left(\frac{f_{OSC}}{fs}\right)^2} - C_0$$

C_1: Crystal element equivalent series capacitance

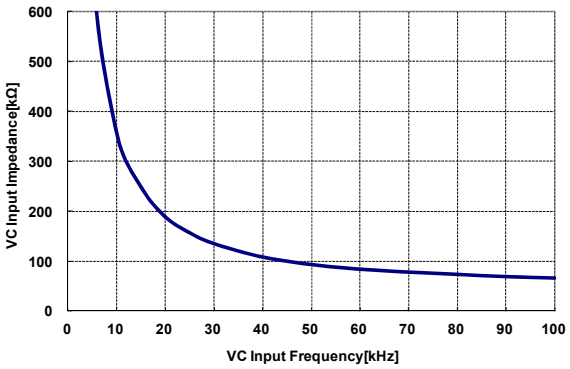
C_0: Crystal element equivalent parallel capacitance

fs: Crystal element series resonance frequency

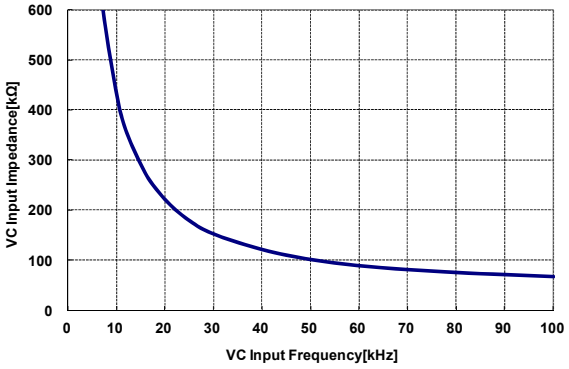
VC Terminal Input Impedance

[Measurement conditions] T_a= +25°C, V_C= 0V

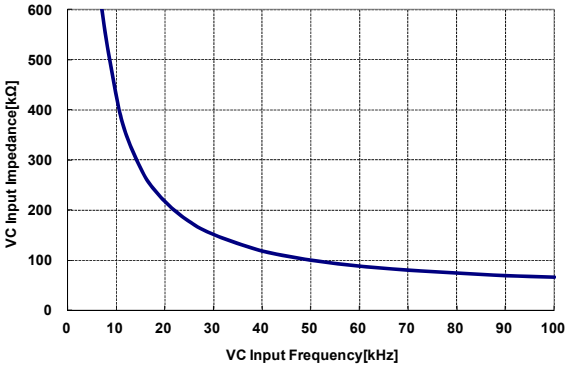
[5079A1]



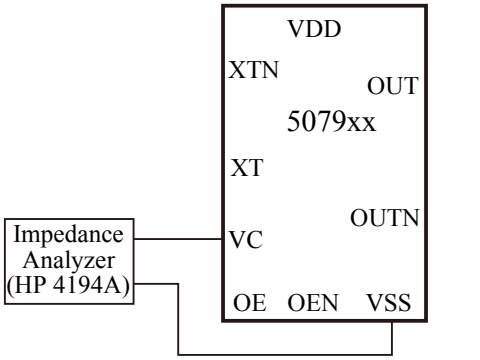
[5079B1]



[5079C1]



[Measurement circuit diagram]

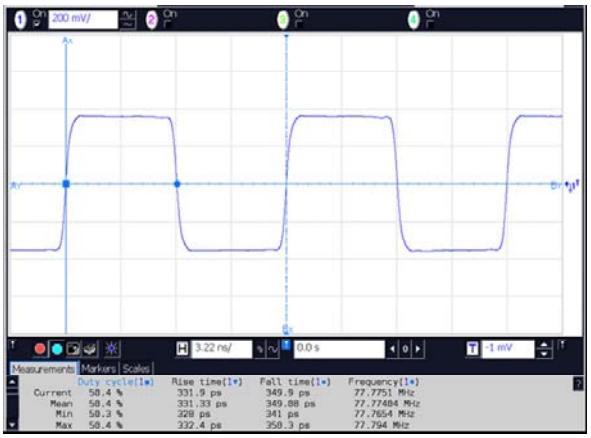


VC input signal: 1kHz to 100kHz, 0.1V_{P-P}

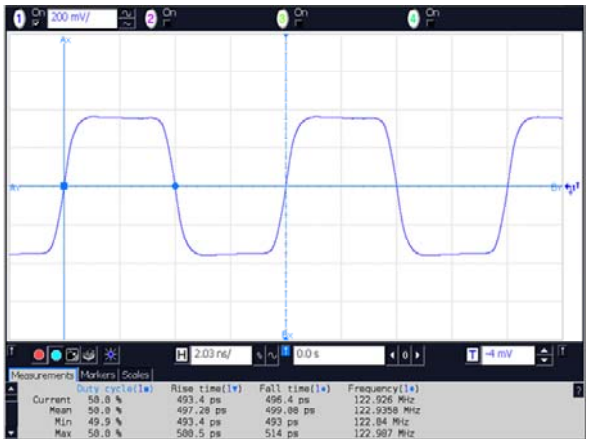
Output Waveform

[Measurement conditions] V_{DD}= +3.3V, V_C= +1.65V, T_a= +25°C

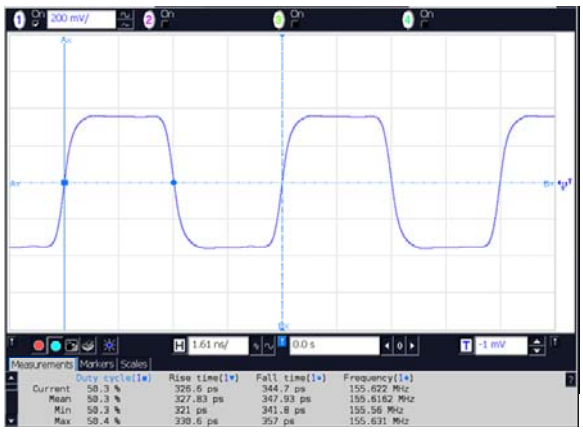
[5079A1] f_{OSC}=77.76MHz



[5079B1] f_{OSC}=122.88MHz



[5079C1] f_{OSC}=155.52MHz



[Measurement circuit diagram]

Measurement circuit 7

Measurement equipment: Oscilloscope DSO80604B (Agilent)
Differential probe 1134A (Probe head E2678A)

Please pay your attention to the following points at time of using the products shown in this document.

1. The products shown in this document (hereinafter ”Products”) are designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools and measurement equipment. The Products are not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment. The Products are not designed and manufactured to be used for the apparatus that exerts harmful influence on the human lives due to the defects, failure or malfunction of the Products.
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