OVERVIEW

The 5078 series are CMOS output VCXO ICs that provide a wide frequency pulling range. They employ bipolar oscillator circuit and recently developed varicap diode fabrication process that provides a low phase noise characteristic and a wide frequency pulling range without any external components. The 5078 series are ideal for wide pulling range, low phase noise, VCXO modules.

FEATURES

- VCXO with recently developed varicap diode built-in
- Oscillator: Fundamental frequency oscillation
- Output frequency: 30 to 170MHz
- Operating supply voltage range: 2.97 to 3.63V
- Oscillator frequency range (for fundamental oscillation):
  60 to 100MHz (Ax version)
  100 to 170MHz (Bx version)
- -40 to +105°C operating temperature range
- CMOS output
- Frequency divider built-in
  Selectable by version: f_{OSC}, $f_{OSC}/2$
- Standby function
  High impedance in standby mode, oscillator stops
- 15pF output load capacitance
- Frequency pulling range: ±150ppm@A1 version, V_C=1.65±1.65V, f=77.76MHz (γ=290, C0=2.4pF)
  ±130ppm@B1 version, V_C=1.65±1.65V, f=155.52MHz (γ=330, C0=1.5pF)
- Low phase noise: -130dBc/Hz@A1 version, 1kHz Offset, f=77.76MHz (γ=290, C0=2.4pF)
  -162dBc/Hz@A1 version, 10MHz Offset, f=77.76MHz
  -125dBc/Hz@B1 version, 1kHz Offset, f=155.52MHz (γ=330, C0=1.5pF)
  -162dBc/Hz@B1 version, 10kHz Offset, f=155.52MHz

APPLICATIONS

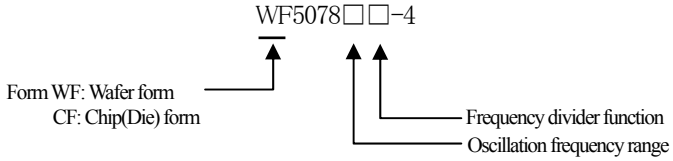
SONET/SDH, Ethernet, Fibre Channel, LTE

SERIES CONFIGURATION

Version Name	Recommended operating frequency range (f_{OSC})*1 [MHz]	Output frequency (f_{OUT})
5078A1	60MHz to 100MHz	f_{OSC}
5078A2	60MHz to 100MHz	$f_{OSC}/2$
5078B1	100MHz to 170MHz	f_{OSC}
5078B2	100MHz to 170MHz	$f_{OSC}/2$

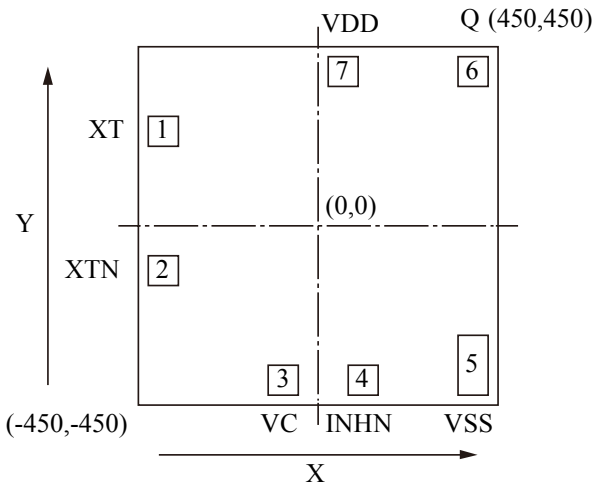
*1. The recommended oscillation frequency is a yardstick value derived from the resonator used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to resonator characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
The recommended characteristics for the crystal element are:
A versions: R1 < 20Ω, C0 < 1.5pF
B versions: R1 < 20Ω, C0 < 1.5pF

ORDERING INFORMATION

Device	Package	Version name
WF5078xx-4	Wafer form	
CF5078xx-4	Chip form	

PAD LAYOUT

(Unit: μm)



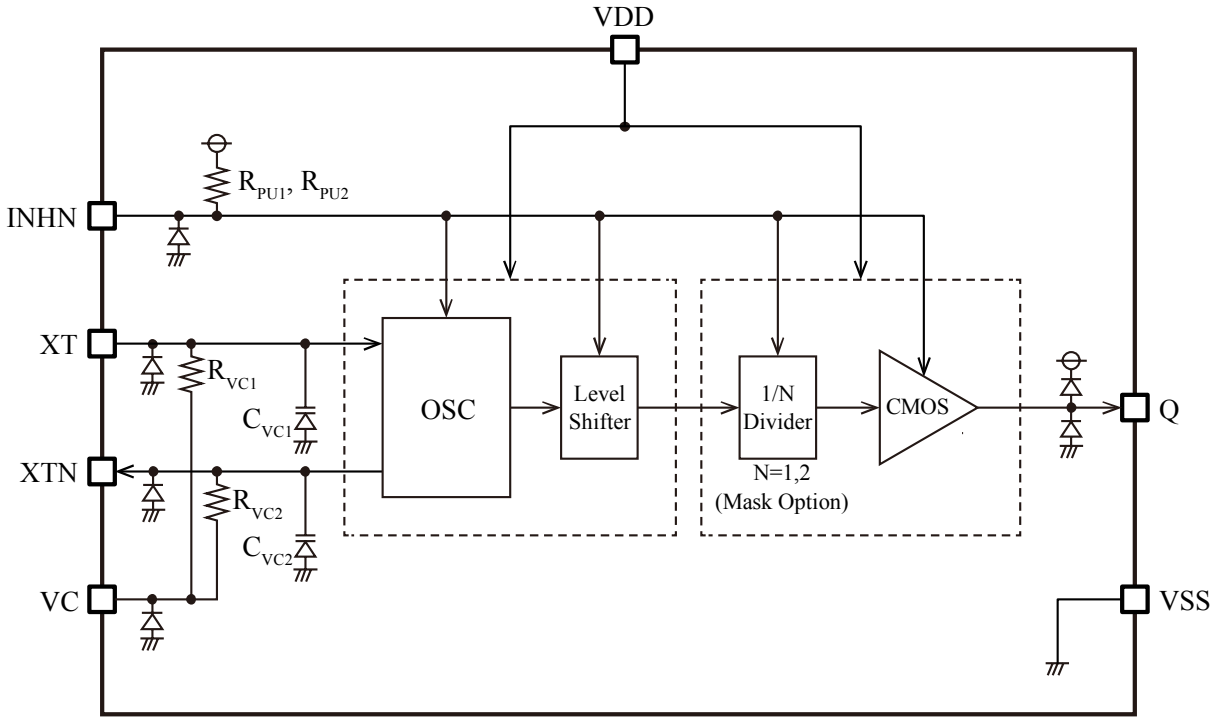
Chip size: 0.9mm×0.9mm
Chip thickness: 130μm
PAD size: 80μm×80μm (PAD No.1, 2, 3, 4, 6, 7 pins)
80μm×160μm (PAD No.5 pin)
Chip base: V_{SS} potential

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O*1	Description	Pad Coordinates (Unit : μm)	
				X	Y
1	XT	I	Crystal connection pin	-345.0	177.0
2	XTN	O		-345.0	-98.0
3	VC	I	Control voltage input pin	-75.4	-345.0
4	INHN	I	Input pin controlled output state(oscillator stops when LOW), Power-saving pull-up resistor built-in	93.2	-345.0
5	VSS	-	(-) ground	337.0	-305.0
6	Q	O	Output one of f_{OSC}, $f_{OSC}/2$	331.9	345.0
7	VDD	-	(+) supply voltage	50.1	345.0

*1. I: Input pin O: Output pin

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition		Rating	Unit
Supply voltage range*1	V_{DD}	VDD pin		-0.3 to +5.0	V
Input voltage range*1*2	V_{IN}	Input pins		-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	Output pins		-0.3 to V_{DD}+0.3	V
Junction temperature*3	T_j			+125	°C
Storage temperature range*4	T_{STG}	Wafer, Chip form		-55 to +125	°C
Output current*3	I_{OUT}	Q pin	T_a = -40 ~ +85°C	±20	mA
			T_a = -40 ~ +105°C	±10	mA

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Operating supply voltage	V_{DD}	Between VDD and VSS pins*2	2.97	3.3	3.63	V
Input voltage	V_{IN}	INHN, VC pins	0		V_{DD}	V
Operating temperature	T_a		-40		+105	°C
Output load capacitance	C_L				15	pF
Oscillator frequency range*1	f_{OSC}	5078Ax	60		100	MHz
		5078Bx	100		170	
Output frequency range	f_{OUT}	5078A1	60		100	MHz
		5078A2	30		50	
		5078B1	100		170	
		5078B2	50		85	

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5078 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics

A1, A2 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating MIN	Rating TYP	Rating MAX	Unit
Current consumption A1 version: f_{OSC}	I_{DD}	measurement circuit 1, no load, INHN=Open V_{DD}=3.3V, f_{OSC}=77.76MHz, f_{OUT}=77.76MHz			5.2	8.0	mA
Current consumption A2 version: f_{OSC}/2	I_{DD}	measurement circuit 1, no load, INHN=Open V_{DD}=3.3V, f_{OSC}=77.76MHz, f_{OUT}=38.88MHz			4.2	7.0	mA
Standby current	I_{STB}	measurement circuit 1, INHN=0V	T_a = -40 ~ +85°C			10	µA
			T_a = -40 ~ +105°C			100	µA
High-level output voltage	V_{OH}	measurement circuit 2, Q pin, I_{OH}=-4mA		V_{DD}-0.4			V
Low-level output voltage	V_{OL}	measurement circuit 2, Q pin, I_{OL}=4mA				0.4	V
Output leakage current	I_Z	measurement circuit 3, Q pin, INHN=0V, T_a=25°C		-1		1	µA
High-level input voltage	V_{IH}	measurement circuit 4, INHN pin		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 4, INHN pin				0.3V_{DD}	V
Pull-up resistance 1	R_{PU1}	measurement circuit 5, INHN pin, INHN=0V		1	4	9	MΩ
Pull-up resistance 2	R_{PU2}	measurement circuit 5, INHN pin, INHN=0.7V_{DD}		50	100	200	kΩ
Oscillator block built-in resistance*1	R_{VC1}	measurement circuit 6, between VC and XT		100	200	300	kΩ
	R_{VC2}	measurement circuit 6, between VC and XTN		100	200	300	
Input leakage resistance*1	R_{VIN}	measurement circuit 7, VC pin, T_a=25°C		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C =0.3V	5.88	6.53	7.18	pF
			V_C =1.65V	3.51	4.13	4.75	
			V_C =3.0V	1.80	2.25	2.70	
	C_{VC2}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C =0.3V	8.82	9.80	10.78	pF
			V_C =1.65V	5.27	6.20	7.13	
			V_C =3.0V	2.70	3.38	4.06	
Maximum modulation frequency	F_M	-3dB frequency, T_a=25°C V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 8, Crystal : 77.76MHz		20	50		kHz

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC - XT or XTN
Input leakage resistance: Resistance between VC - VSS (DC characteristic)
Refer to pg.22 for VC Terminal Input Impedance.

B1, B2 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating MIN	Rating TYP	Rating MAX	Unit
Current consumption B1 version: f_{OSC}	I_{DD}	measurement circuit 1, no load, INHN=Open V_{DD}=3.3V, f_{OSC}=155.52MHz, f_{OUT}=155.52MHz			10	15	mA
Current consumption B2 version: f_{OSC}/2	I_{DD}	measurement circuit 1, no load, INHN=Open V_{DD}=3.3V, f_{OSC}=155.52MHz, f_{OUT}=77.76MHz			8.1	12	mA
Standby current	I_{STB}	measurement circuit 1, INHN=0V	T_a = -40 ~ +85°C			10	µA
			T_a = -40 ~ +105°C			100	µA
High-level output voltage	V_{OH}	measurement circuit 2, Q pin, I_{OH}=-8mA		V_{DD}-0.4			V
Low-level output voltage	V_{OL}	measurement circuit 2, Q pin, I_{OH}=8mA				0.4	V
Output leakage current	I_Z	measurement circuit 3, Q pin, INHN=0V, T_a=25°C		-1		1	µA
High-level input voltage	V_{IH}	measurement circuit 4, INHN pin		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 4, INHN pin				0.3V_{DD}	V
Pull-up resistance 1	R_{PU1}	measurement circuit 5, INHN pin, INHN=0V		1	4	9	MΩ
Pull-up resistance 2	R_{PU2}	measurement circuit 5, INHN pin, INHN=0.7V_{DD}		50	100	200	kΩ
Oscillator block built-in resistance*1	R_{VC1}	measurement circuit 6, between VC and XT		100	200	300	kΩ
	R_{VC2}	measurement circuit 6, between VC and XTN		100	200	300	
Input leakage resistance*1	R_{VIN}	measurement circuit 7, VC pin, T_a=25°C		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C =0.3V	4.38	4.86	5.35	pF
			V_C =1.65V	2.62	3.08	3.55	
			V_C =3.0V	1.38	1.72	2.06	
	C_{VC2}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C =0.3V	6.24	6.94	7.63	pF
			V_C =1.65V	3.70	4.36	5.01	
			V_C =3.0V	1.89	2.36	2.83	
Maximum modulation frequency	F_M	-3dB frequency, T_a=25°C V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 8, Crystal : 155.52MHz		20	50		kHz

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC - XT or XTN
Input leakage resistance: Resistance between VC - VSS (DC characteristic)
Refer to pg.22 for VC Terminal Input Impedance.

Switching Characteristics

A1, A2 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
AC "H" level output voltage	V_{TOP}	measurement circuit 9, C_L=15pF	0.9V_{DD}			V
AC "L" level output voltage	V_{BASE}	measurement circuit 9, C_L=15pF			0.1V_{DD}	V
Duty cycle	Duty	measurement circuit 9, Ta=25°C, V_{DD}=3.3V	45		55	%
Output rise time	t_r	measurement circuit 9, C_L=15pF, 0.1V_{DD}→0.9V_{DD}		1.5	3.0	ns
Output fall time	t_f	measurement circuit 9, C_L=15pF, 0.9V_{DD}→0.1V_{DD}		1.5	3.0	ns
Output enable propagation delay	t_{OE}	measurement circuit 10, T_a=25°C INHN= "Low"→"High"			2	ms
Output disable propagation delay	t_{OD}	measurement circuit 10, T_a=25°C INHN= "High"→"Low"			200	ns

Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated.
The recommended crystal element characteristics are R1 < 20Ω and C0 < 1.5pF.

B1, B2 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +105°C unless otherwise noted

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
AC "H" level output voltage	V_{TOP}	measurement circuit 9, C_L=15pF	0.9V_{DD}			V
AC "L" level output voltage	V_{BASE}	measurement circuit 9, C_L=15pF			0.1V_{DD}	V
Duty cycle	Duty	measurement circuit 9, Ta=25°C, V_{DD}=3.3V	45		55	%
Output rise time	t_r	measurement circuit 9, C_L=15pF, 0.1V_{DD}→0.9V_{DD}		1.2	2.4	ns
Output fall time	t_f	measurement circuit 9, C_L=15pF, 0.9V_{DD}→0.1V_{DD}		1.2	2.4	ns
Output enable propagation delay	t_{OE}	measurement circuit 10, T_a=25°C INHN= "Low"→"High"			2	ms
Output disable propagation delay	t_{OD}	measurement circuit 10, T_a=25°C INHN= "High"→"Low"			200	ns

Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated.
The recommended crystal element characteristics are R1 < 20Ω and C0 < 1.5pF.

Timing chart

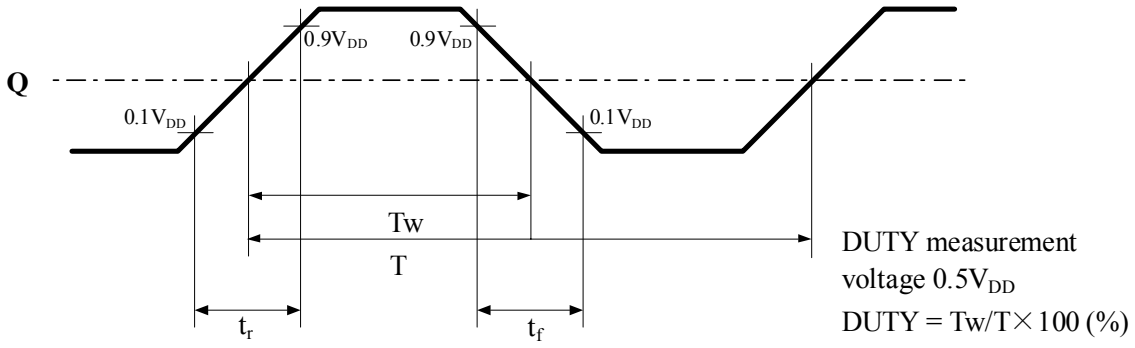


Figure 1. Output switching waveform

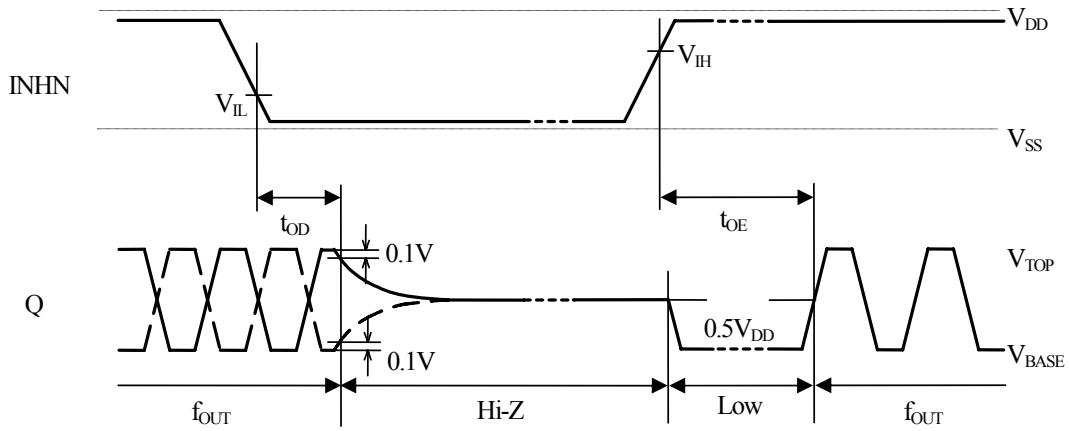


Figure 2. Output disable and oscillation start timing chart

FUNCTIONAL DESCRIPTION

INHN Function

Q output is stopped and becomes high impedance.

INHN	Q	Oscillator
HIGH or Open	f_{OUT}	Operating
LOW	Hi-Z	Stopped

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5078 series have an oscillation detection circuit.

The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

Boot function

It becomes easy to start oscillation by making XTN pin potential to V_{DD} level when oscillation starts up. A current flows into VC pin when the voltage below a V_{DD} level is being applied to VC pin. A boot function is canceled after an oscillation start.

MEASUREMENT CIRCUITS

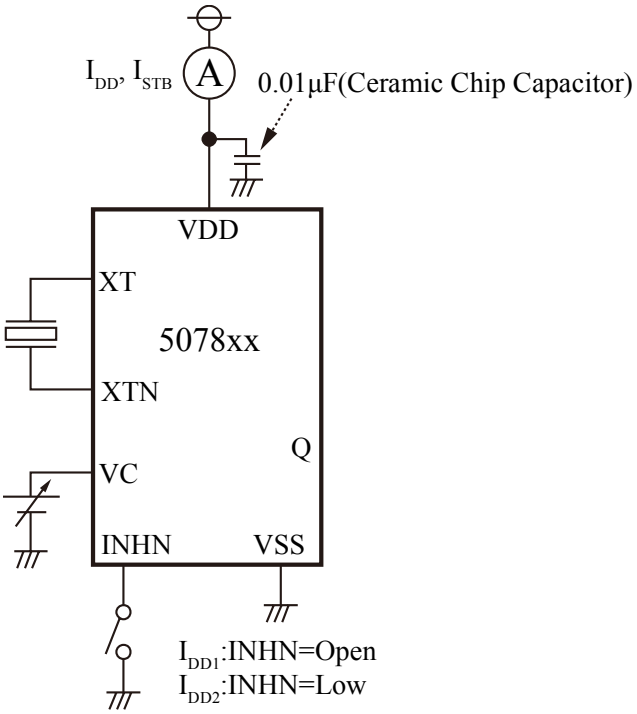
These are measurement circuits for electrical characteristics and switching characteristics.

■ Note: Bypass capacitors specified in each measurement circuit below should be connected between VDD and VSS. If the bypass capacitors are not connected, the required characteristics may not be realized.
Circuit wiring of bypass capacitors and load capacitors should be connected as short as possible (within approximately 3mm). If the circuit wiring is long, the required characteristics may not be realized.

* The capacitor used in measurement circuits below;
GRM188B11H103K (MURATA) 0.01μF

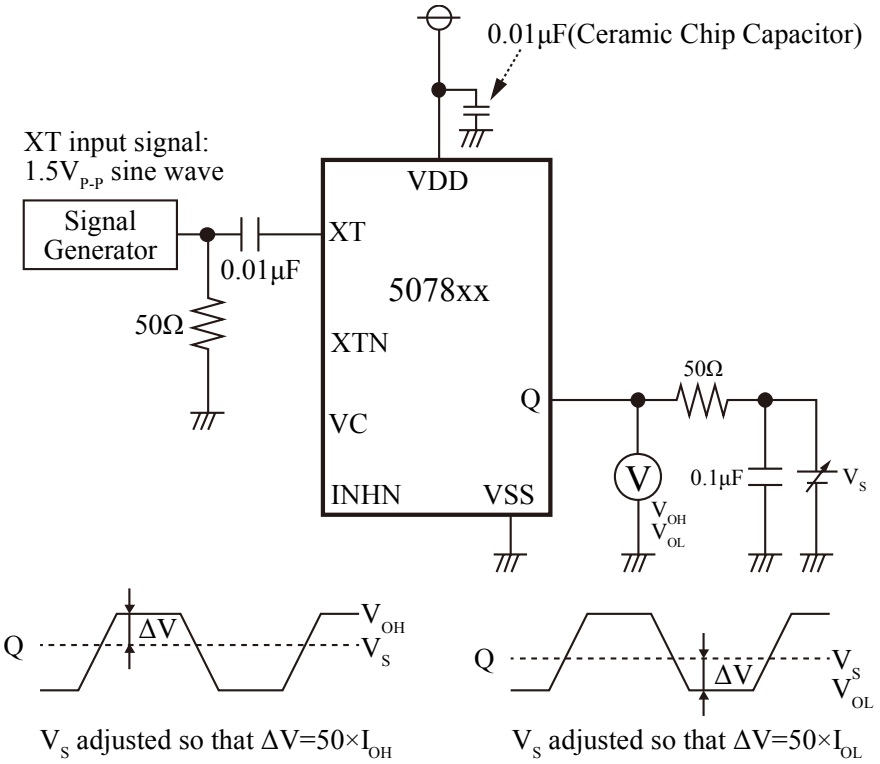
MEASUREMENT CIRCUIT 1

Measurement Parameter: I_{DD}, I_{STB}



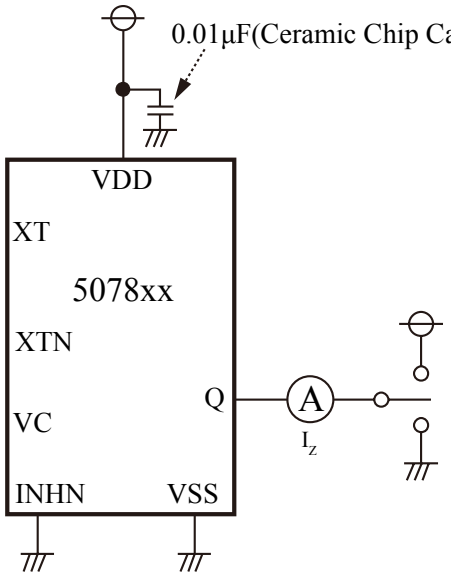
MEASUREMENT CIRCUIT 2

Measurement Parameter: V_{OH}, V_{OL}



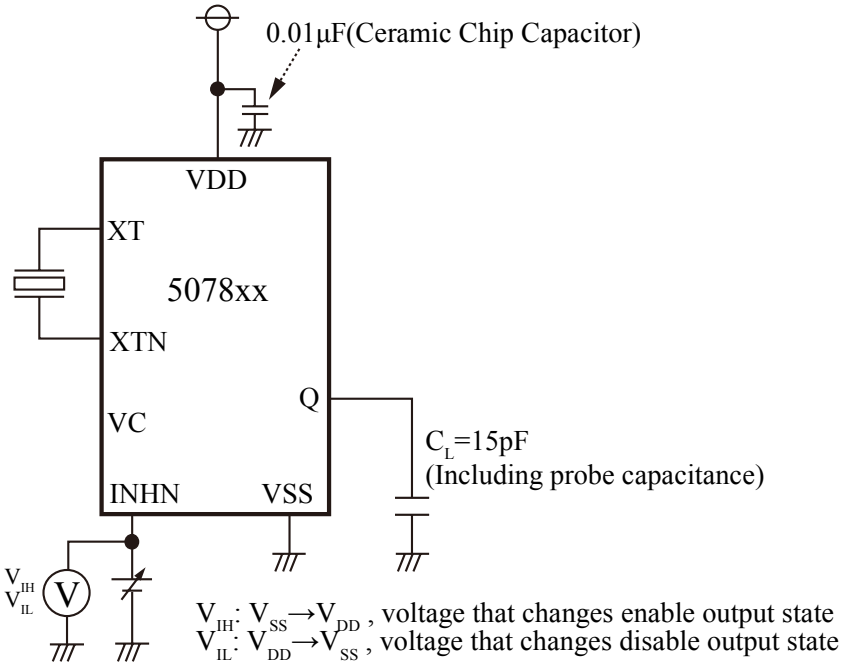
MEASUREMENT CIRCUIT 3

Measurement Parameter: I_Z



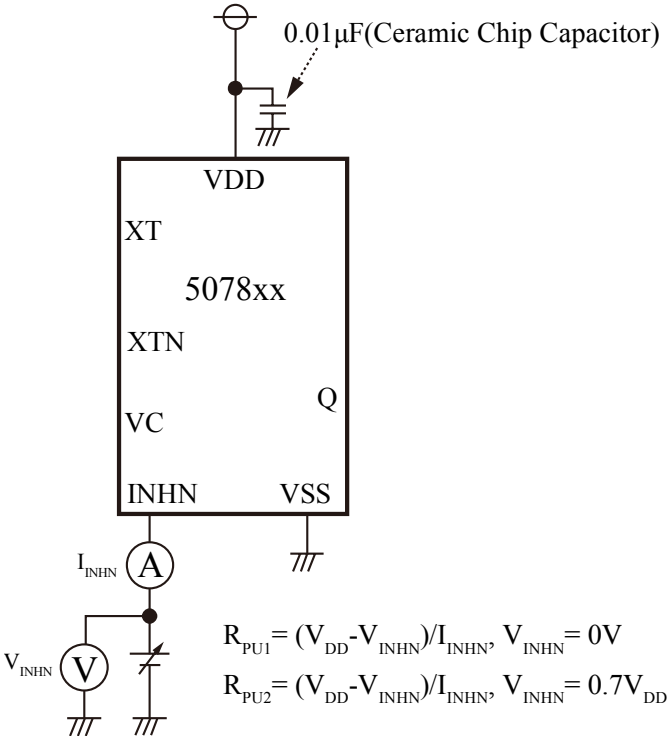
MEASUREMENT CIRCUIT 4

Measurement Parameter: V_{IH}, V_{IL}



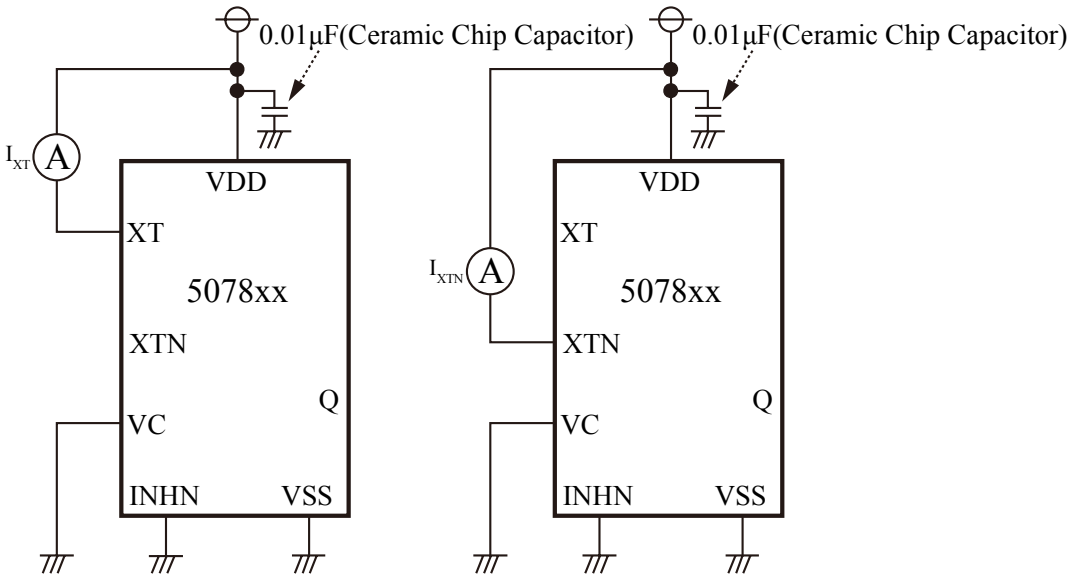
MEASUREMENT CIRCUIT 5

Measurement Parameter: R_{PU1}, R_{PU2}



MEASUREMENT CIRCUIT 6

Measurement Parameter: R_{VC1}, R_{VC2}

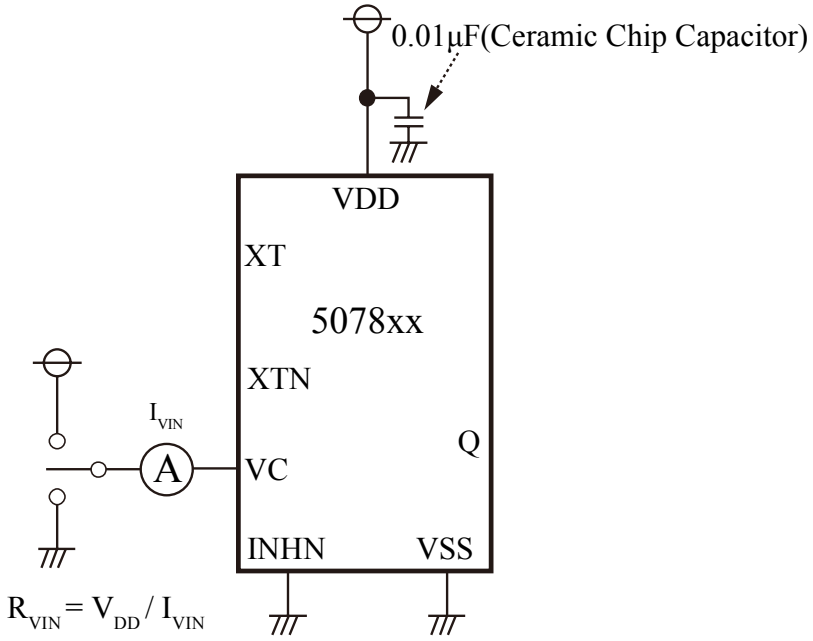


$R_{VC1} = V_{DD} / I_{XT}$

$R_{VC2} = V_{DD} / I_{XTN}$

MEASUREMENT CIRCUIT 7

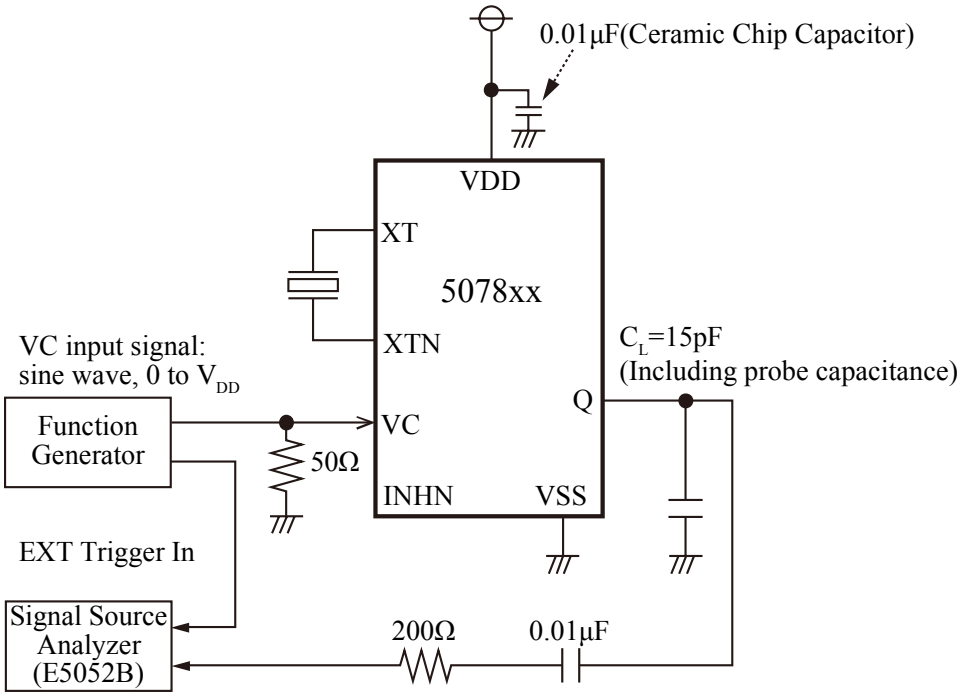
Measurement Parameter: R_{VIN}



$R_{VIN} = V_{DD} / I_{VIN}$

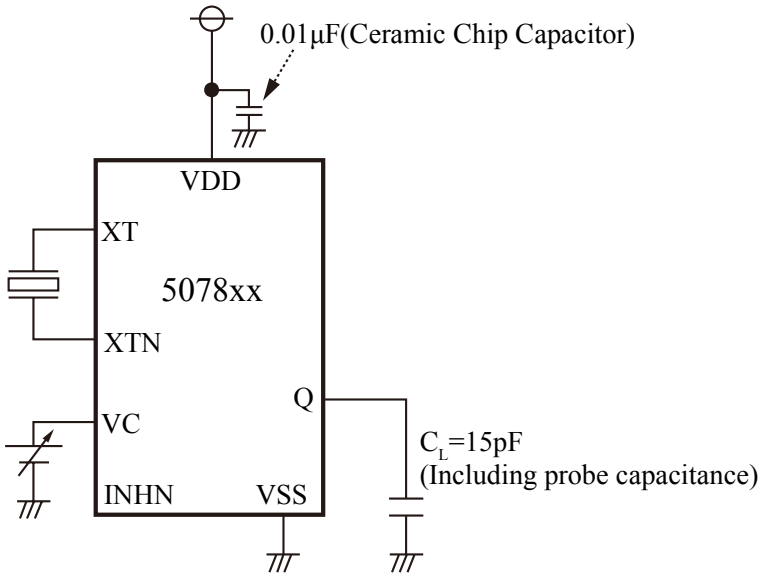
MEASUREMENT CIRCUIT 8

Measurement Parameter: F_M



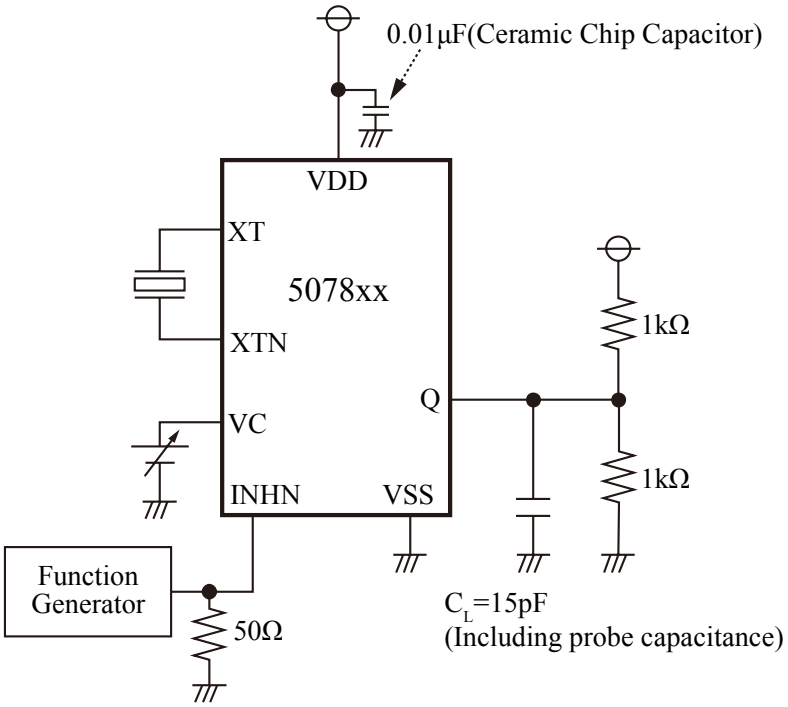
MEASUREMENT CIRCUIT 9

Measurement Parameter: Duty, t_r, t_f, V_{TOP}, V_{BASE}



MEASUREMENT CIRCUIT 10

Measurement Parameter: t_{OE}, t_{OD}



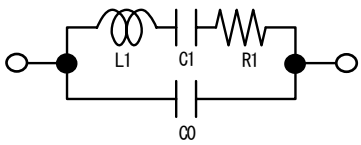
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

Crystal used for measurement

Parameter	A1	B1
f_{OSC}(MHz)	77.76	155.52
C0(pF)	2.4	1.5
γ(=C0/C1)	290	330
R1(Ω)	7.0	9.3

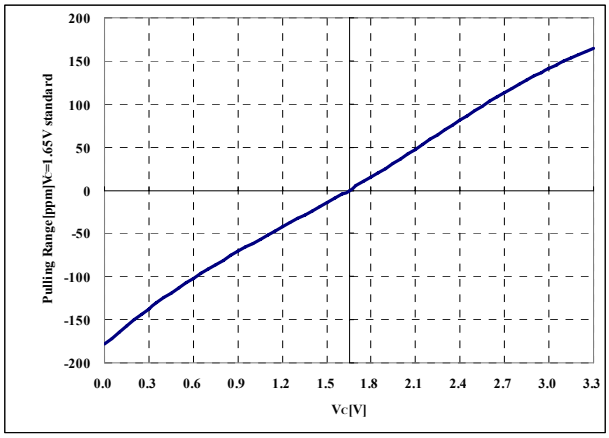
Crystal parameters



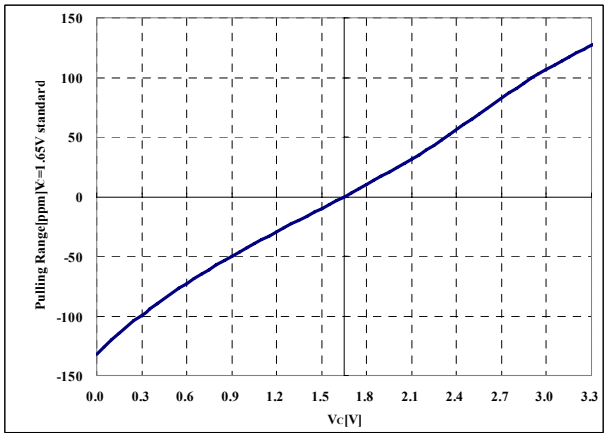
Pulling Range

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C

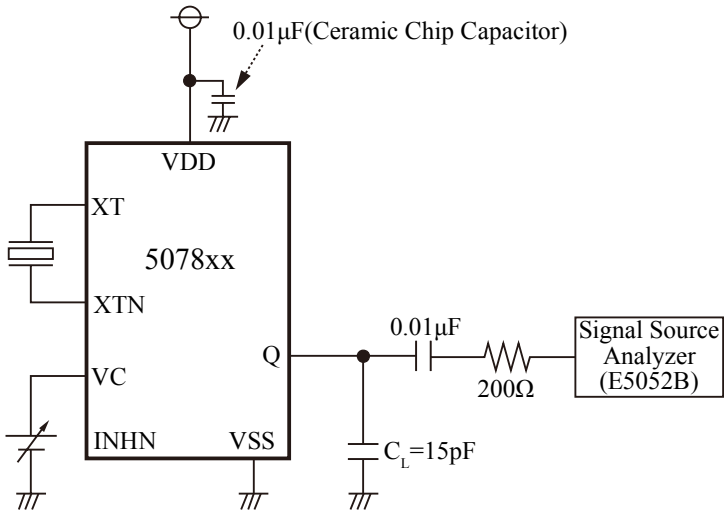
[5078Ax] f_{OSC}=77.76MHz



[5078Bx] f_{OSC}=155.52MHz



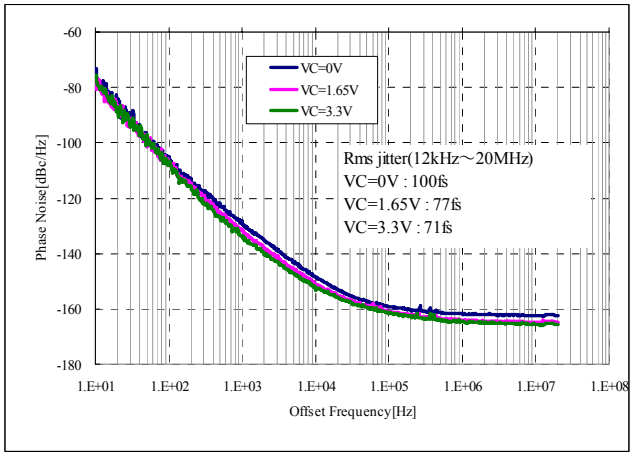
[Measurement circuit diagram]



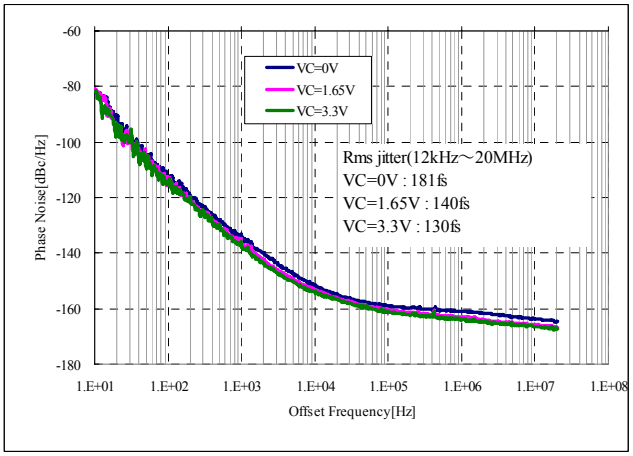
Phase Noise

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C

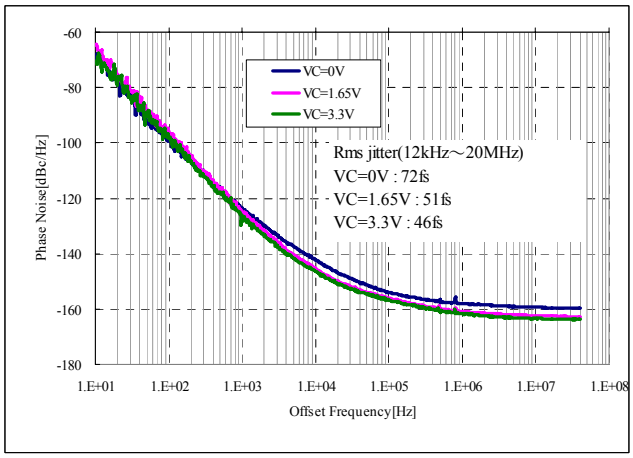
[5078A1] f_{OSC}=77.76MHz, f_{OUT}=77.76MHz



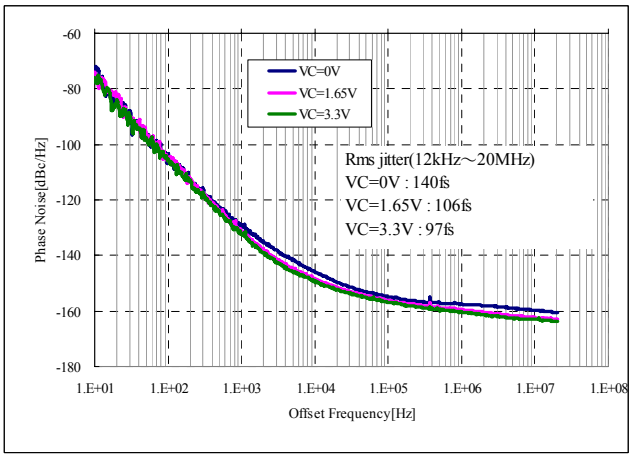
[5078A2] f_{OSC}=77.76MHz, f_{OUT}=38.88MHz



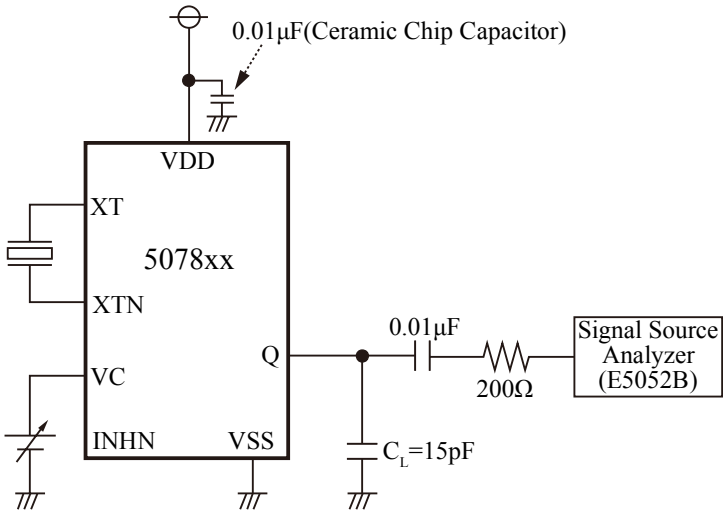
[5078B1] f_{OSC} =155.52MHz, f_{OUT} =155.52MHz



[5078B2] f_{OSC} =155.52MHz, f_{OUT} =77.76MHz



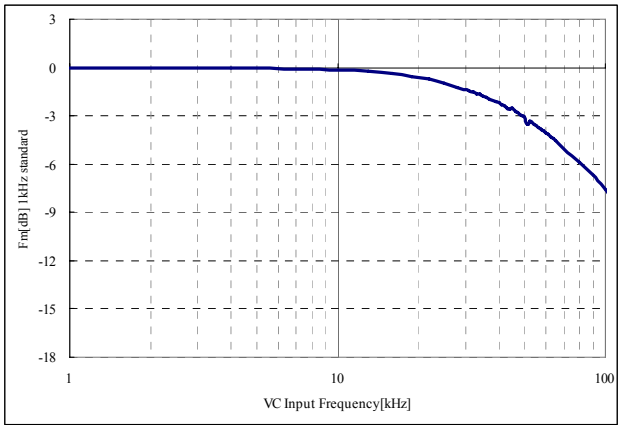
[Measurement circuit diagram]



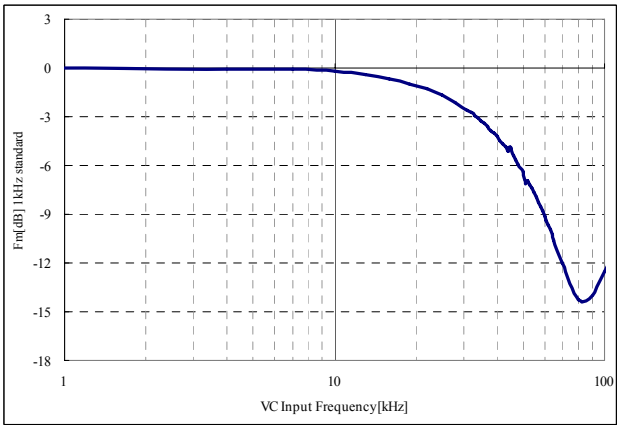
Modulation Bandwidth

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C

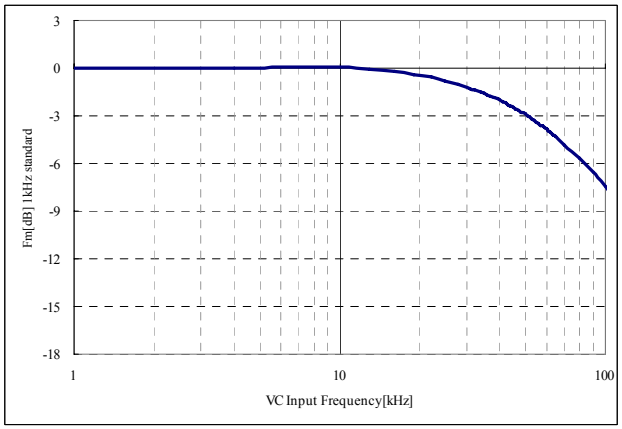
[5078A1] f_{OSC}=77.76MHz, f_{OUT}=77.76MHz



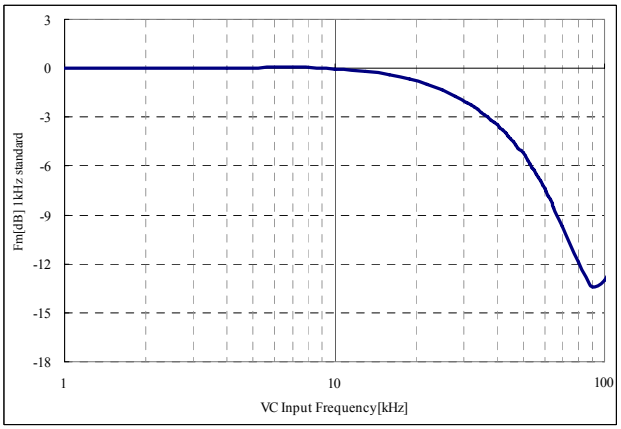
[5078A2] f_{OSC}=77.76MHz, f_{OUT}=38.88MHz



[5078B1] f_{OSC} =155.52MHz, f_{OUT} =155.52MHz



[5078B2] f_{OSC} =155.52MHz, f_{OUT} =77.76MHz

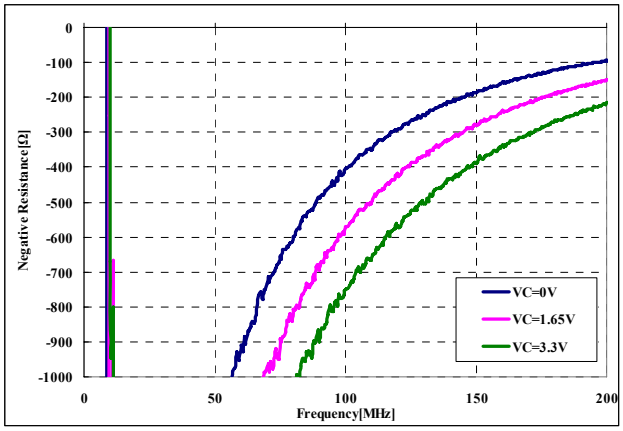


[Measurement circuit diagram] Measurement circuit 8

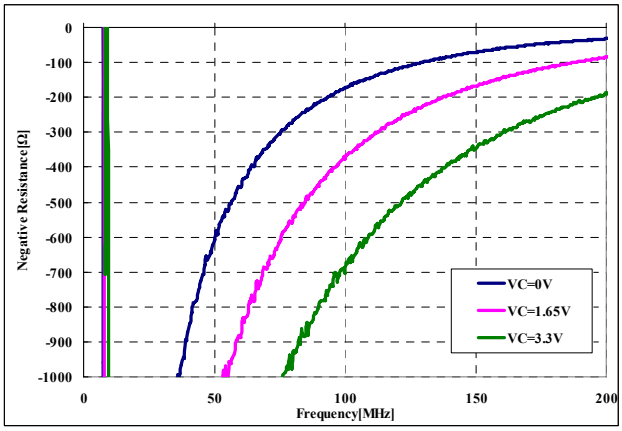
Negative Resistance

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C, C0=0pF

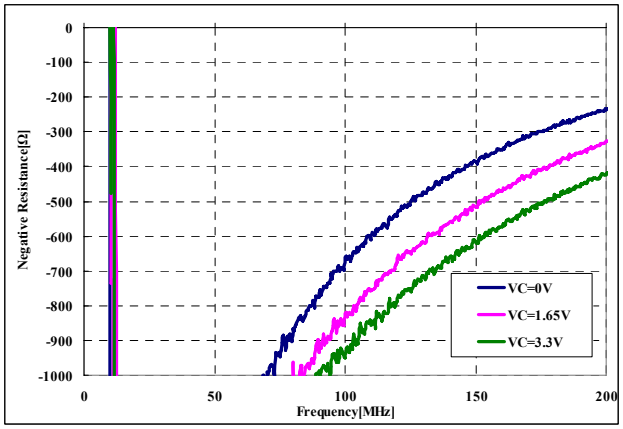
[5078Ax] Boot



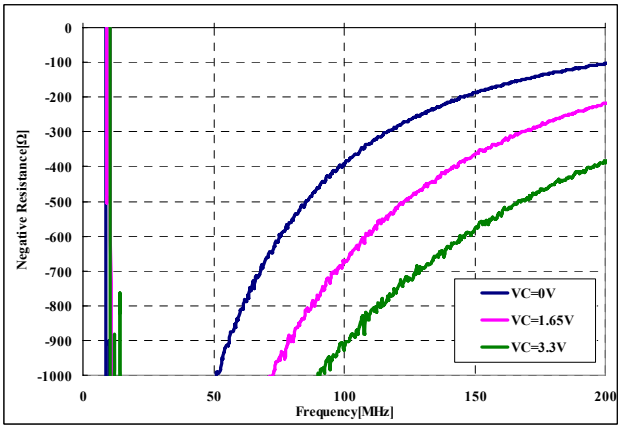
[5078Ax] After boot release



[5078Bx] Boot

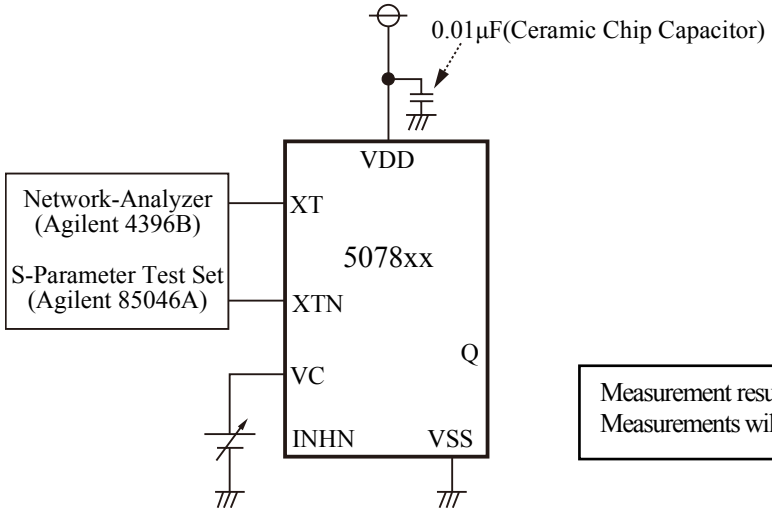


[5078Bx] After boot release



At the time of oscillation start, negative resistance becomes deep by boot function.
The boot function is released when the oscillation is steady, and oscillation starts.

[Measurement circuit diagram]

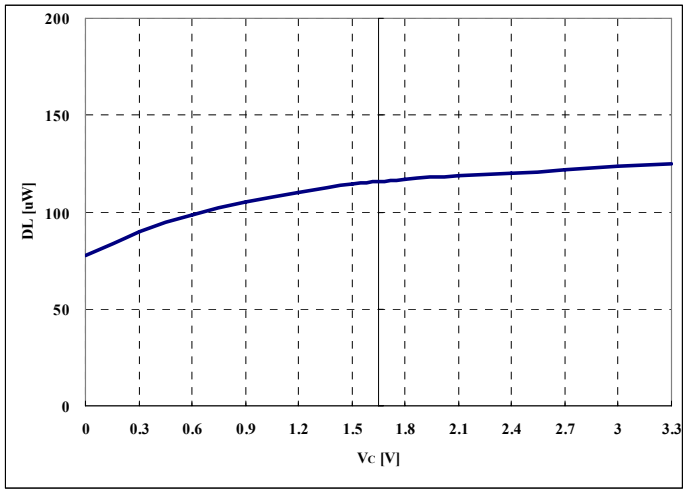


Measurement results using 4396B Agilent analyzer on NPC test jig.
Measurements will vary with test jig and measurement environment.

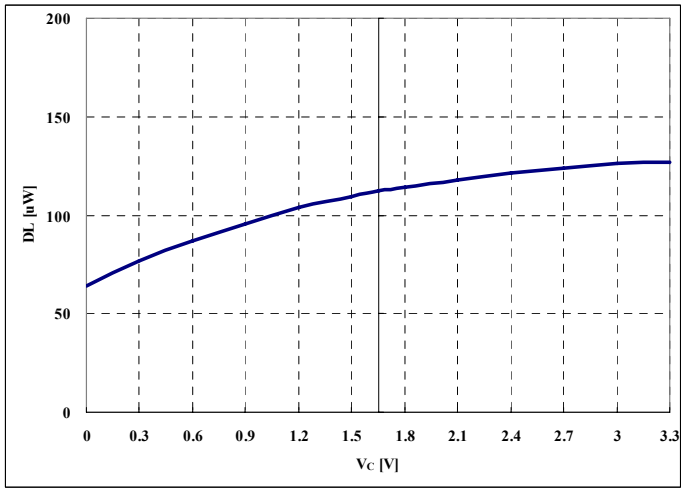
Drive Level

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C

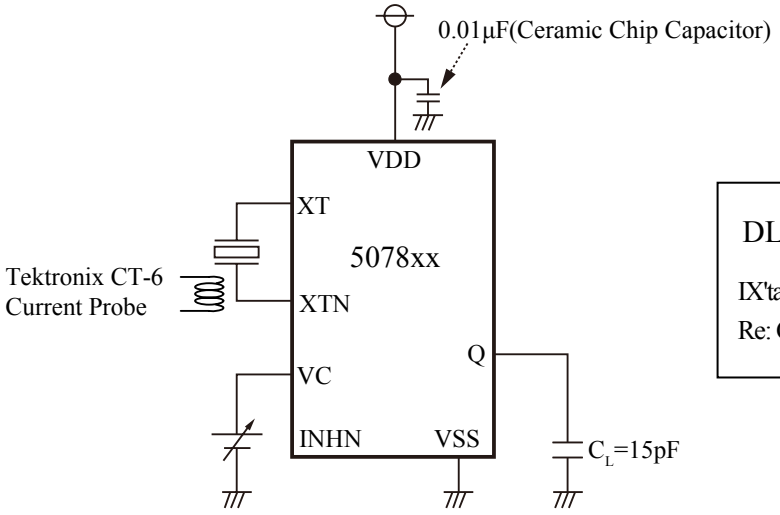
[5078Ax] f_{OSC}=77.76MHz



[5078Bx] f_{OSC}=155.52MHz



[Measurement circuit diagram]



$$DL = (IX'tal)^2 \times Re$$

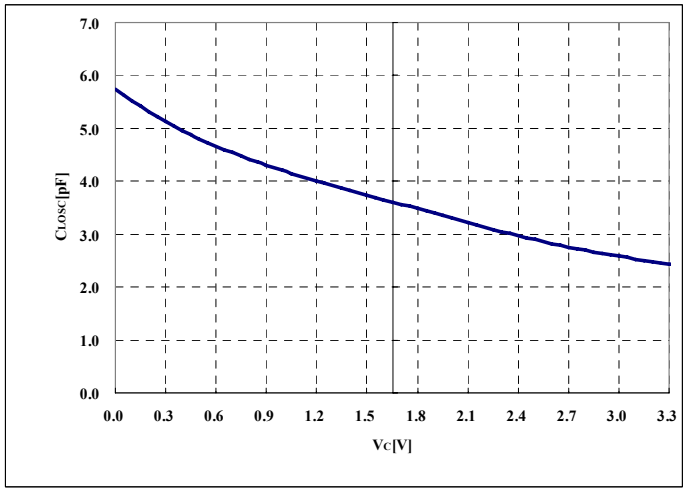
IX'tal: Current though Crystal (RMS)

Re: Crystal's effective resistance

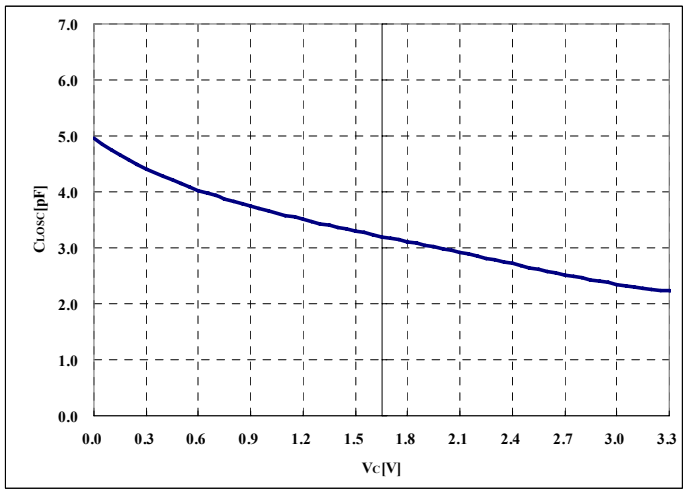
Oscillator CL Characteristics

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C

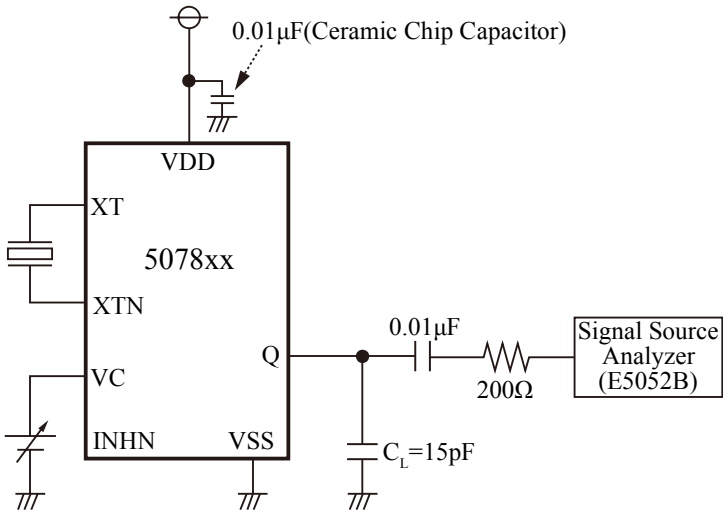
[5078Ax] f_{OSC}=77.76MHz



[5078Bx] f_{OSC}=155.52MHz



[Measurement circuit diagram]



CL_{OSC}: Oscillator circuit equivalent capacitance determined by oscillator frequency

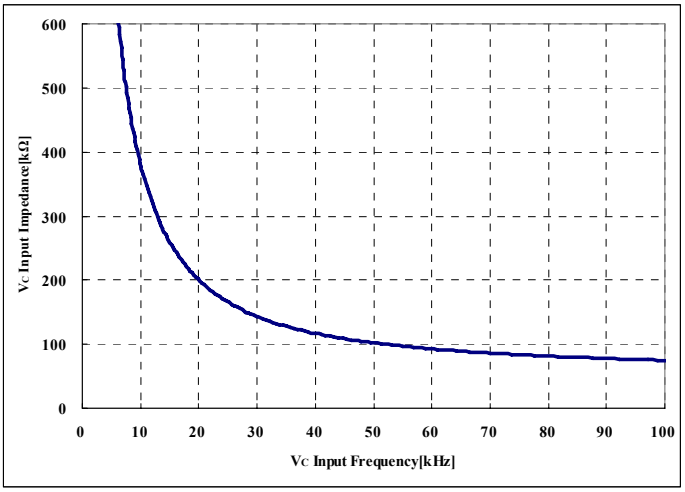
$$CLosc = \frac{C1}{\left(\frac{f_{OSC}}{fs}\right)^2 - 1} - C0$$

C1: Crystal element equivalent series capacitance
C0: Crystal element equivalent parallel capacitance
fs: Crystal element series resonance frequency

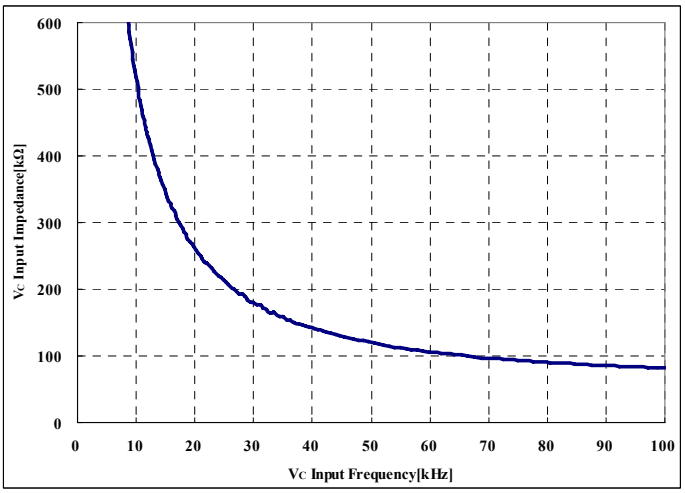
VC Terminal Input Impedance

[Measurement conditions] T_a=25°C, V_C=0V

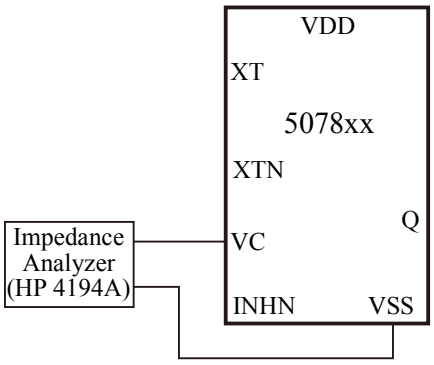
[5078Ax]



[5078Bx]



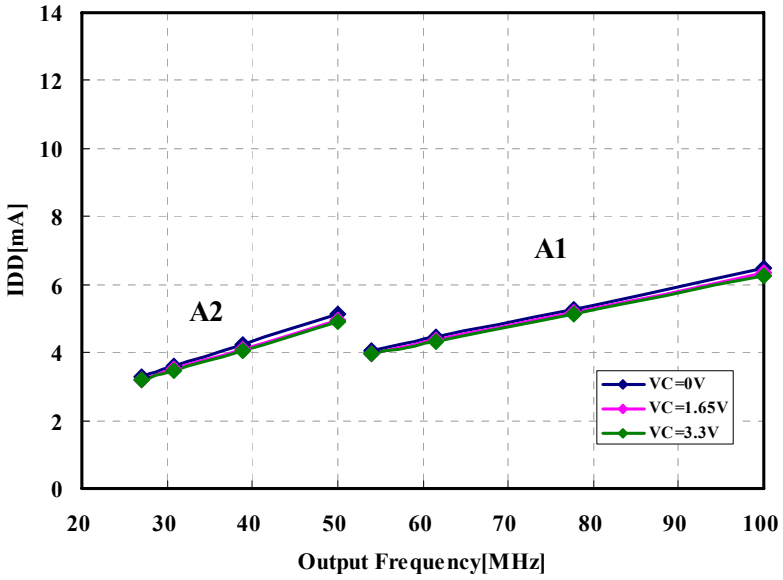
[Measurement circuit diagram]



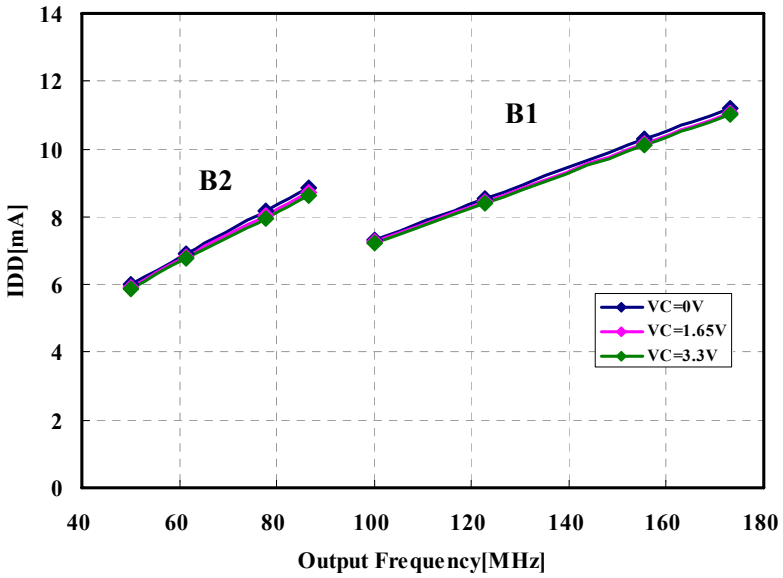
Current Consumption

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, T_a=25°C

[5078Ax]



[5078Bx]

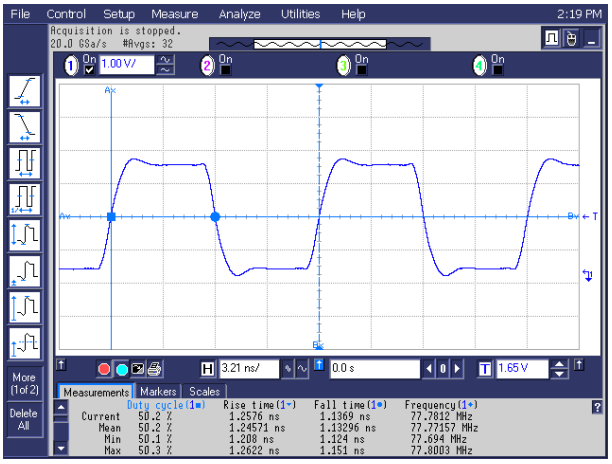


[Measurement circuit diagram] Measurement circuit 1

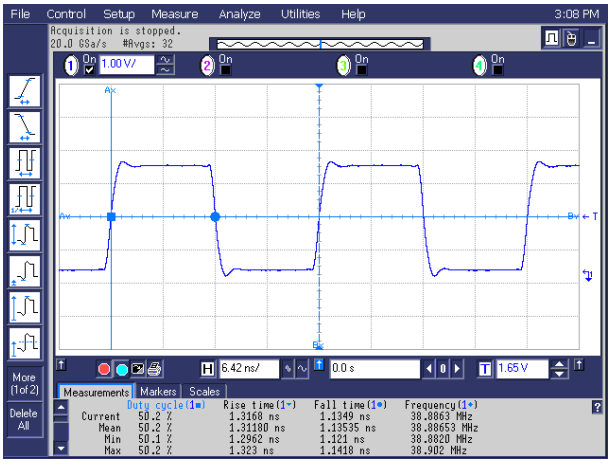
Output Waveform

[Measurement conditions] V_{DD}=3.3V, V_{SS}=0V, V_C=1.65V, T_a=25°C

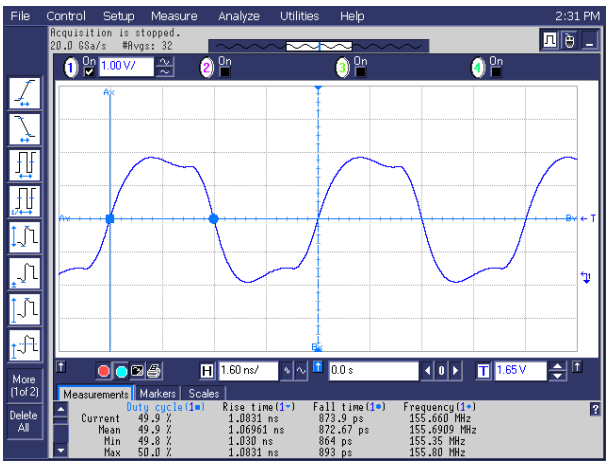
[5078A1] f_{OSC} =77.76MHz, f_{OUT}=77.76MHz



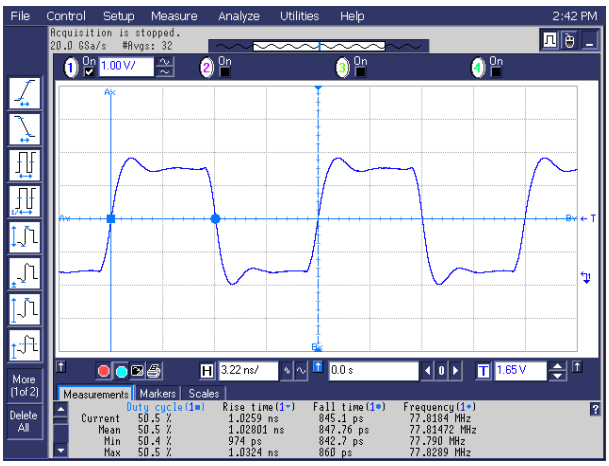
[5078A2] f_{OSC}=77.76MHz, f_{OUT}=38.88MHz



[5078B1] f_{OSC} =155.52MHz, f_{OUT}=155.52MHz



[5078B2] f_{OSC} =155.52MHz, f_{OUT}=77.76MHz



[Measurement circuit diagram] Measurement circuit 9

Measurement equipment: Oscilloscope DSO80604B(Agilent), Differential probe 1134A (Probe head E2678A)

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