1. OVERVIEW

The CF5061HxxL/WF5061HxxL series are LVDS output oscillator ICs that support a wide output frequency range ideal for high-frequency applications typical in high-speed communications devices.

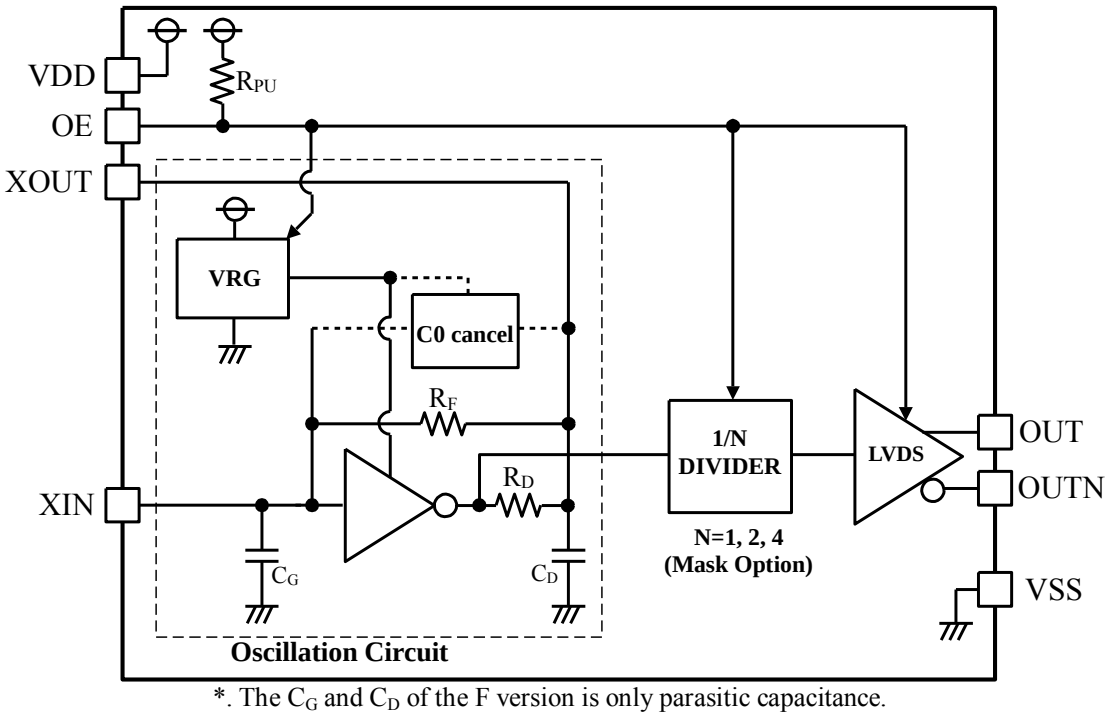
They employ an oscillator circuit optimized for compact, 3rd overtone crystal elements, making them ideal for use as compact, crystal oscillator modules.

The oscillator circuit uses voltage regulator drive to achieve a low drive level.

2. FEATURES

- ■Operating supply voltage: 1.71V to 1.89V
- ■Operating temperature: -40°C to +125°C
- ■Recommended oscillation frequency (f_0): 3rd overtone frequency 100MHz to 140MHz
  Fundamental frequency 100MHz to 140MHz
- ■Output frequency (f_{OUT}): f_0
- ■Oscillator capacitances: C_G, C_D built-in
- ■Output level: LVDS
- ■Standby function: Oscillator stops, Hi-Z outputs,
  power saving pull-up resistor built-in (OE output)
- ■Oscillation detection circuit built-in

3. BLOCK DIAGRAM

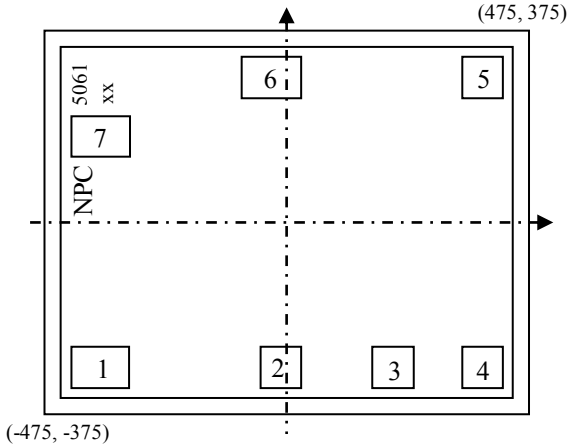


*. The C_G and C_D of the F version is only parasitic capacitance.

4. PAD LAYOUT

(1) Chip size[*1]: X=0.95mm, Y=0.75mm
(2) Rear surface potential: V_{SS} level
(3) Pad size: No. 1, 6, 7: 110µm × 80µm
No. 2, 3, 4, 5: 80µm × 80µm
(4) Chip dimensions

*1. Chip size is measured between scribe line centers.



Pad Coordinates (Origin in chip center), Unit: [µm]

No.	X	Y	Name
1	-363.7	-283.5	VDD
2	-11.7	-283.5	XIN
3	208.2	-283.5	XOUT
4	383.5	-283.5	VSS
5	383.5	283.5	OE
6	-29.1	283.5	OUTN
7	-368.5	168.2	OUT

5. PAD DESCRIPTION

Number	Name	I/O[*1]	Function
1	VDD	-	(+) Supply voltage
2	XIN	I	Oscillator connections
3	XOUT	O	
4	VSS	-	(-) Supply voltage
5	OE	I	Output enable. Outputs are disabled when OE is V_{SS}. Disabled state: Oscillator stopped, Hi-Z outputs
6	OUTN	O	LVDS output (inverting output) Disabled state: Hi-Z
7	OUT	O	LVDS output Disabled state: Hi-Z

*1. I : Input, O : Output

6. VERSION LINEUP

5061 Hx xL

Output frequency
Oscillation frequency range

(1) Version name 1st character (oscillation frequency range)

Version	Oscillation mode	C0 cancel circuit	Recommended C0 value (pF)*1	Oscillator capacitance (pF)*2		Oscillation frequency (reference values) f_0 (MHz)
				C_G	C_D	
D	3rd overtone Fundamental	Yes	1.0 to 2.0*3 (0.8 to 2.5)*4	1	1	100 to 140

∗1. The oscillator circuit is optimized for 5032 to 3225 sized crystal oscillators.
When using 7050 sized crystal elements that have large C0, additional evaluation is recommended before implementation due to the increased risk of insufficient oscillation margin.
*2. Values do not include parasitic capacitance.
*3. Normal recommended range based on the oscillator circuit design.
*4. Values in ( ) are full range values. If using these ranges, additional evaluation is recommended before implementation.

(2) Version name 2nd character (output frequency)

Version	Output frequency (f_{OUT})
6	f_0

7. ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit	Notes
Supply voltage range	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V	*1
Input voltage range	V_{IN}	Inputs	-0.3 to V_{DD}+0.3	V	*1、*2
Output voltage range	V_{OUT}	Outputs	-0.3 to V_{DD}+0.3	V	*1、*2
Junction temperature	T_j		+150	°C	*3
Storage temperature	T_{STG}	Chip, wafer form	-55 to +150	°C	*4

*1. Parameters must not exceed ratings, not even momentarily. If the rating is exceeded, it may affect the electrical characteristics and reliability.
*2. V_{DD} indicates the operating supply voltage in "8. RECOMMENDED OPERATING CONDITIONS."
*3. Do not exceed ratings. If a rating is exceeded, there is a risk of deterioration in characteristics and decrease in reliability.
*4. When stored separately in Nitrogen or vacuum atmosphere.

8. RECOMMENDED OPERATING CONDITIONS

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillation frequency*1	f_0	HD6L	100		140	MHz
Output frequency	f_{OUT}	HD6L	100		140	MHz
Operating supply voltage	V_{DD}	Between VDD and VSS*2	1.71		1.89	V
Input voltage	V_{IN}	Inputs	V_{SS}		V_{DD}	V
Operating temperature	T_a		-40		+125	°C
Output load resistance	R_L	Between OUT and OUTN	99		101	Ω

*1. The oscillation frequency range is a target based on evaluation results for the crystal element used for NPC characteristics verification, and does not represent a guarantee of the oscillation frequency band. The oscillation characteristics can vary significantly depending on the characteristics and mounting conditions of the crystal. Accordingly, oscillation characteristics should be thoroughly evaluated for each crystal.
*2. For stable device operation, connect a 0.01μF or larger ceramic chip capacitor between VDD and VSS, mounted close (within approximately 3mm) to the chip. Also, use the thickest wiring possible between the IC and capacitor.
* Operation outside the recommended operating conditions may adversely affect reliability. Use only within specified ratings.

9. ELECTRICAL CHARACTERISTICS

9.1. DC Characteristics

Measurement circuits 1 to 3 in "Conditions" are shown in "12. MEASUREMENT CIRCUITS."

V_{DD}=1.71 to 1.89V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption (HD6L ver.)	I_{DDD}_1.8V	Measurement circuit 1, OE=Open, f_0=125MHz	V_{DD}=1.8V		13.5	20.0	mA
Standby current	I_{STB}	Measurement circuit 1, OE=V_{SS}	$T_a \leq$+85℃			15	μA
			T_a>+85℃			30	
High-level output voltage	V_{OH}	Measurement circuit 2, OUT/OUTN			1.43	1.60	V
Low-level output voltage	V_{OL}			0.90	1.10		V
Differential output voltage	V_{OD}	Measurement circuit 2, OUT/OUTN		247	330	454	mV
Differential output voltage error	ΔV_{OD}	Measurement circuit 2				50	mV
Offset voltage	V_{OS}	Measurement circuit 2, OUT-OUTN		1.125	1.250	1.375	V
Offset voltage error	ΔV_{OS}	Measurement circuit 2				50	mV
Output leakage current	I_Z	Measurement circuit 3, OE=V_{SS}, OUT/OUTN				10	μA
High-level input voltage	V_{IH}	Measurement circuit 1, OE		0.7V_{DD}			V
Low-level input voltage	V_{IL}	Measurement circuit 1, OE				0.3V_{DD}	V
OE pull-up resistance	R_{PU1}	Measurement circuit 1		0.2	1	8	MΩ
	R_{PU2}	Measurement circuit 1		30	70	150	kΩ
Oscillator feedback resistance (HD6L ver.)	R_{FD}	Design value		1.1	2.2	3.3	kΩ
Oscillator capacitance (HD6L ver.)	C_{GD}	Design value, Excludes parasitic capacitance *1		0.8	1.0	1.2	pF
	C_{DD}			0.8	1.0	1.2	

*1. Confirmed by sampling inspection of the monitor pattern on the wafer.

9.2. AC Characteristics

Measurement circuits 4 and 5 in "Conditions" are shown in "12. MEASUREMENT CIRCUITS."
The conditions for each parameter assume the timing shown in "9.3 TIMING DIAGRAM."

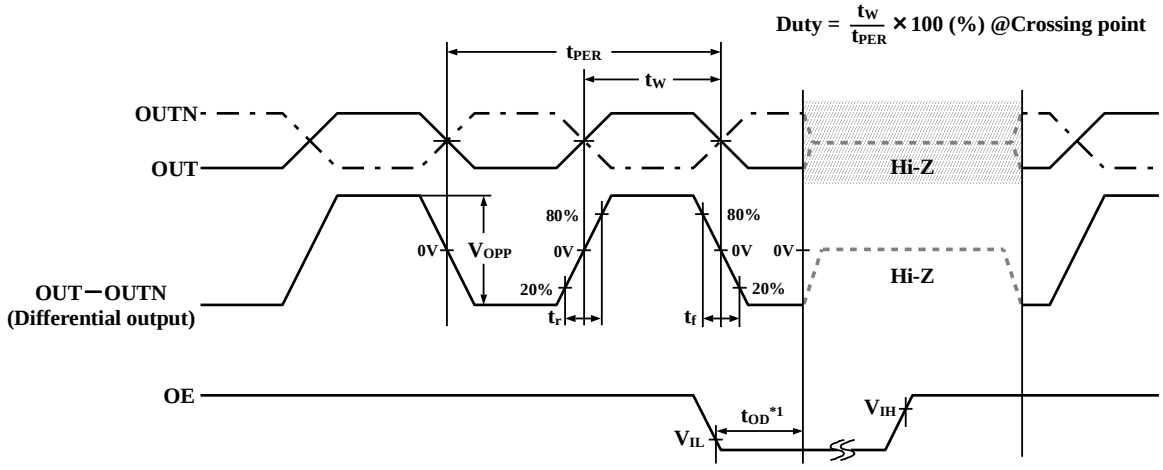
V_{DD}=1.71 to 1.89V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output duty cycle (differential outputs)	Duty	Measurement circuit 4, Measured at 0V crossover point of differential output signal	45		55	%
Output amplitude	V_{OPP}	Measurement circuit 4, Differential output signal	0.4			V
Output rise time	t_r	Measurement circuit 4, Measured between 20% and 80% amplitude of differential output signal		250	500	ps
Output fall time	t_f	Measurement circuit 4, Measured between 80% and 20% amplitude of differential output signal		250	500	ps
Output disable time	t_{OD}	Measurement circuit 5, Time measured OE=V_{IL} (falling edge) and outputs going Hi-Z (see timing diagram for details)			200	ns

* The ratings above are values obtained by measurements using an NPC evaluation standard crystal element, standard testing jig, and evaluation package.
Ratings may have wide tolerances due to crystal element characteristics, evaluation jig, and package parasitic capacitance, so thorough evaluation is recommended.

9.3. Timing Diagram

The timing diagram applies to the "Conditions" in the table in "9.2. AC Characteristics."



*1. The time, after OE falling edge and the output disable time (t_{OD}) has elapsed, taken until the outputs become high impedance (Hi-Z).

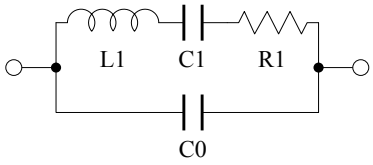
Figure 9-1. Timing diagram

10. REFERENCE CHARACTERISTICS (Typical 5061 Characteristics)

The following characteristics assume the use of the following crystal element.
The characteristics will vary depending on the crystal used and the measurement conditions.

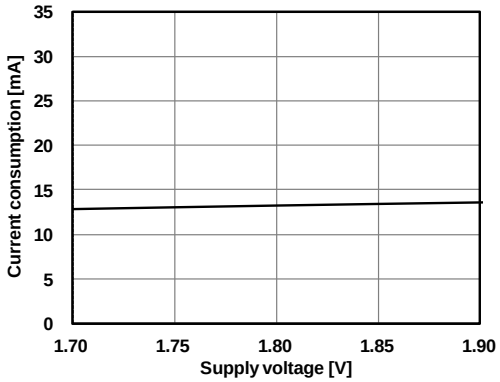
* Crystal oscillator element

Parameter	f_0=125.00MHz
C0(pF)	1.8
R1(Ω)	35
Oscillation mode	3rd overtone



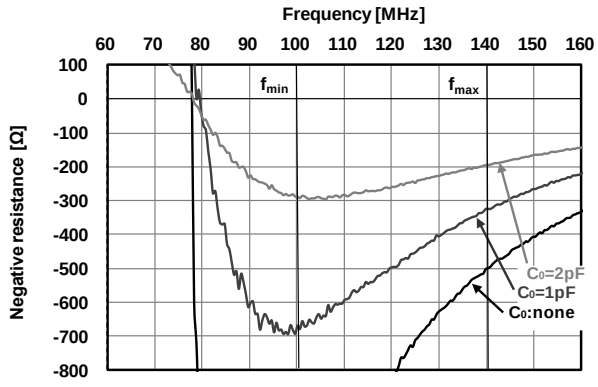
Crystal parameters

10.1. Current Consumption



5061HD6L, f_{OUT}=125MHz, T_a=25°C

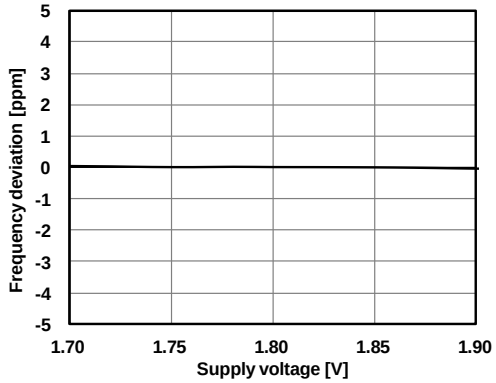
10.2. Negative Resistance



5061HD6L, T_a=25°C, V_{DD}=1.8V

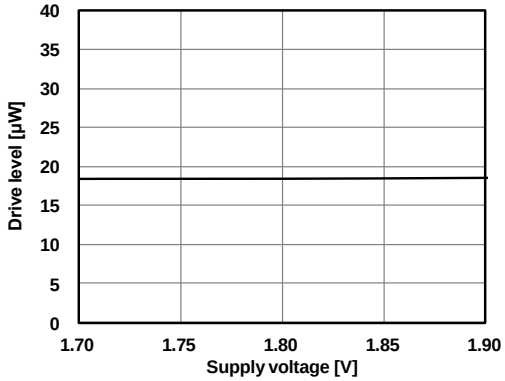
Captions in reference diagrams indicate measurement results for a crystal with equivalent capacitance C0, connected between the XT and XTN terminals of the 5060. The results are from measurements made with the Agilent 4396B using the NPC test jig. The characteristics may vary with measurement jig and measurement conditions.

10.3. Frequency Deviation vs. Voltage



5061HD6L, f_{OUT}=125MHz, T_a=25°C, 1.8V std.

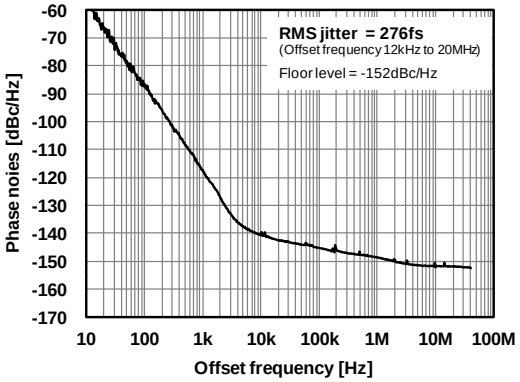
10.4. Drive Level



5061HD6L, f_{OUT}=125MHz, T_a=25°C

10.5. Phase Noise

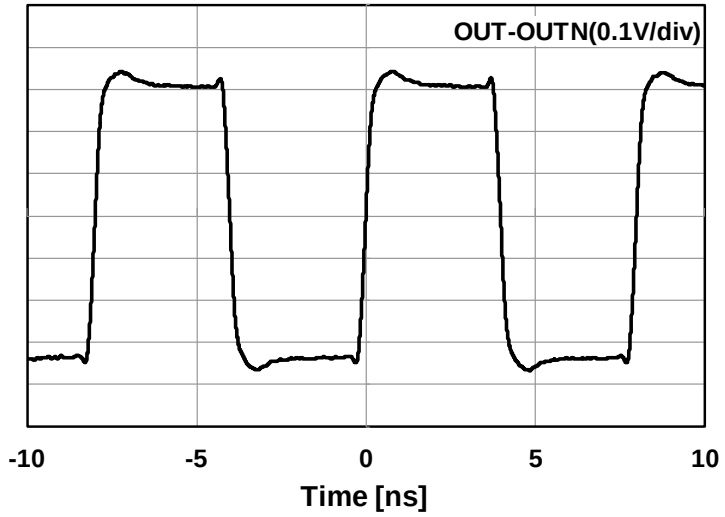
Measurement instrument: Agilent E5052B Signal Source Analyzer



5061HD6L f_{OUT}=125MHz, T_a=25°C, V_{DD}=1.8V

10.6. Output Waveforms

Measuring instrument: Agilent 54855A Oscilloscope



5061HD6L, f_{OUT}=125MHz, T_a=25°C, V_{DD}=1.8V

Duty = 50.1%

t_r = 250ps

t_f = 250ps

11. FUNCTIONAL DESCRIPTION

11.1. OE Function

When OE goes V_{SS}, the OUT/OUTN outputs stop and become high impedance. This function is used to disable the operation of the device.

OE input	OUT/OUTN outputs	Oscillator circuit
V_{DD} or Open	f_0	Operating
V_{SS}	Hi-Z	Stopped

11.2. Power Saving Pull-up Resistor

The OE terminal pull-up resistance switches between R_{PU1} and R_{PU2}, depending on the input level (V_{DD} or V_{SS}).

When the OE terminal is held V_{SS}, the built-in OE terminal pull-up resistance increases (R_{PU1}), reducing the current consumed by the pull-up resistance when the outputs are disabled.

When the device is operating with the OE terminal V_{DD} or open circuit, the pull-up resistance decreases (R_{PU2}), reducing internal susceptibility to the effects of external noise. The OE terminal is held V_{DD} internally to prevent problems that might otherwise cause the outputs to stop abruptly.

11.3. Oscillation Detection Function

The IC has a built-in oscillation detection circuit.

The oscillation detection circuit disables the output circuit when the oscillator starts until the oscillation becomes stable. This function limits the danger of unstable oscillation when the oscillator starts after power is first applied or the output is enabled.

11.4. C0 cancellation circuit

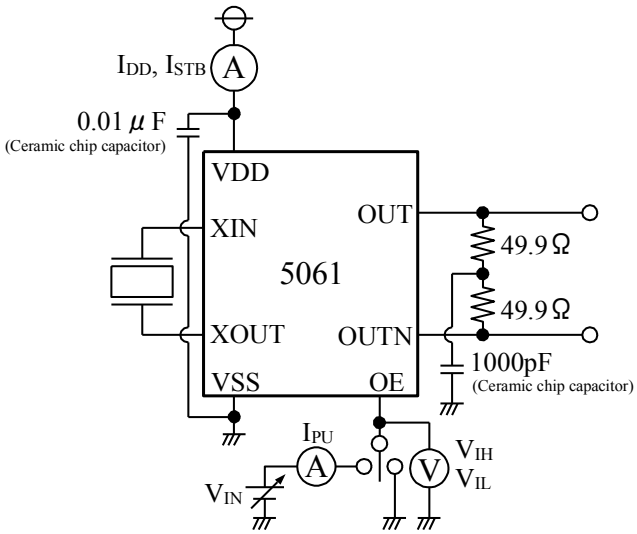
Oscillation circuit with a built-in C0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C0. It reduces the C0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C0.

This cancellation circuit makes it easier to maintain the oscillation margin.

12. MEASUREMENT CIRCUITS

These measurement circuits are used for DC and AC characteristics evaluation.

● **Measurement circuit 1** **Measurement parameters: I_{DD}, I_{STB}, V_{IH}, V_{IL}, R_{PU1}, R_{PU2}**



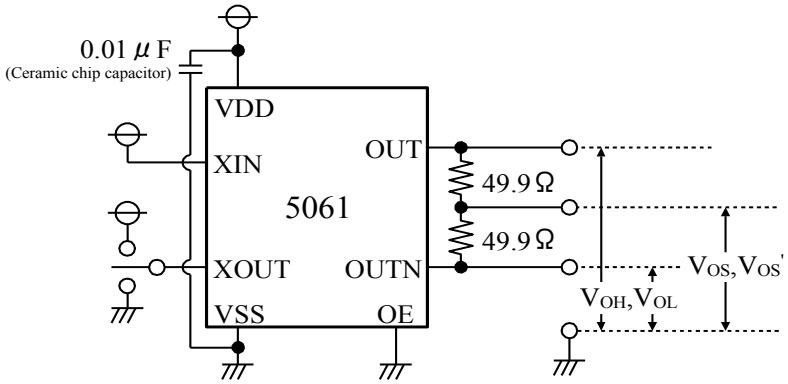
$$R_{PU1} = \frac{V_{DD}}{I_{PU}} \quad (V_{IN} = V_{SS})$$

$$R_{PU2} = \frac{V_{DD} - 0.7V_{DD}}{I_{PU}} \quad (V_{IN} = 0.7V_{DD})$$

V_{IH} : $V_{SS} \rightarrow V_{DD}$ voltage that changes output state
V_{IL} : $V_{DD} \rightarrow V_{SS}$ voltage that changes output state
I_{STB} : OE=V_{SS}

Figure 12-1. Measurement circuit 1

● **Measurement circuit 2** **Measurement parameters: V_{OH}, V_{OL}, V_{OD}, V_{OS}**



XOUT=V_{DD} { OUT =High, OUTN=Low
XOUT=V_{SS} { OUT =Low, OUTN=High

V_{OD} = OUT(High) - OUTN(Low)
V_{OD}' = OUTN(High) - OUT(Low)
$\Delta V_{OD} = |V_{OD} - V_{OD}'|$

V_{OS} : OUT=High, OUTN=Low
V_{OS}' : OUT=Low, OUTN=High
$\Delta V_{OS} = |V_{OS} - V_{OS}'|$

Figure 12-2. Measurement circuit 2

● **Measurement circuit 3 Measurement parameter: I_Z**

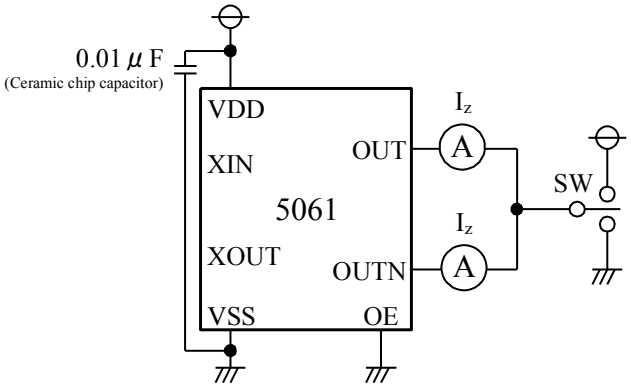


Figure 12-3. Measurement circuit 3

● **Measurement circuit 4 Measurement parameters: Duty, V_{OPP}, t_r, t_f**

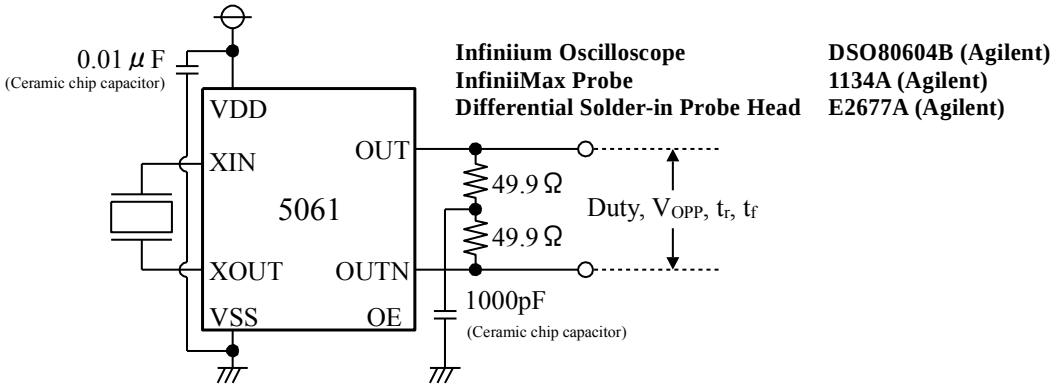


Figure 12-4. Measurement circuit 4

● **Measurement circuit 5 Measurement parameter t_{OD}**

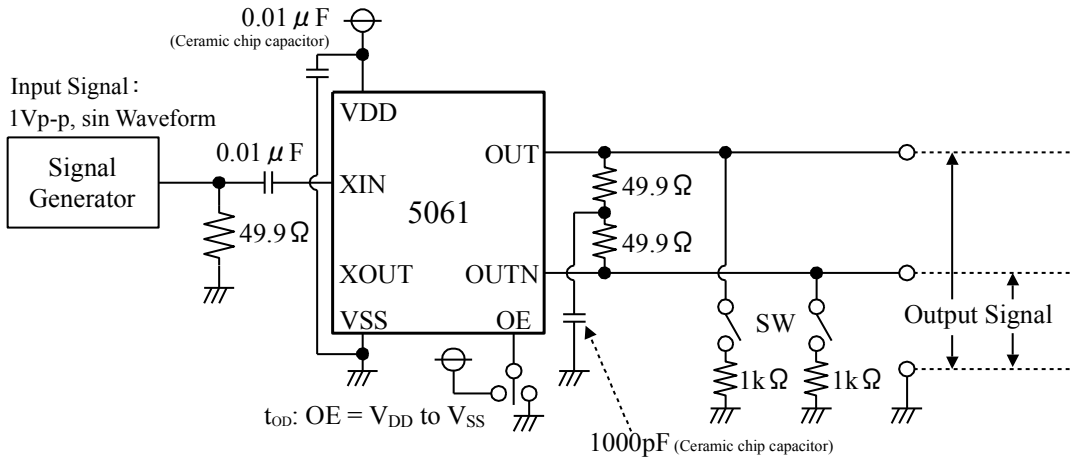
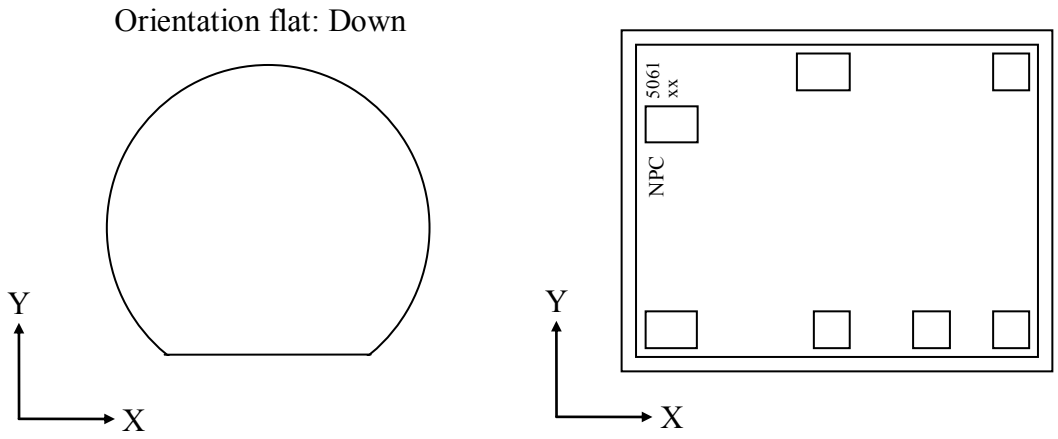
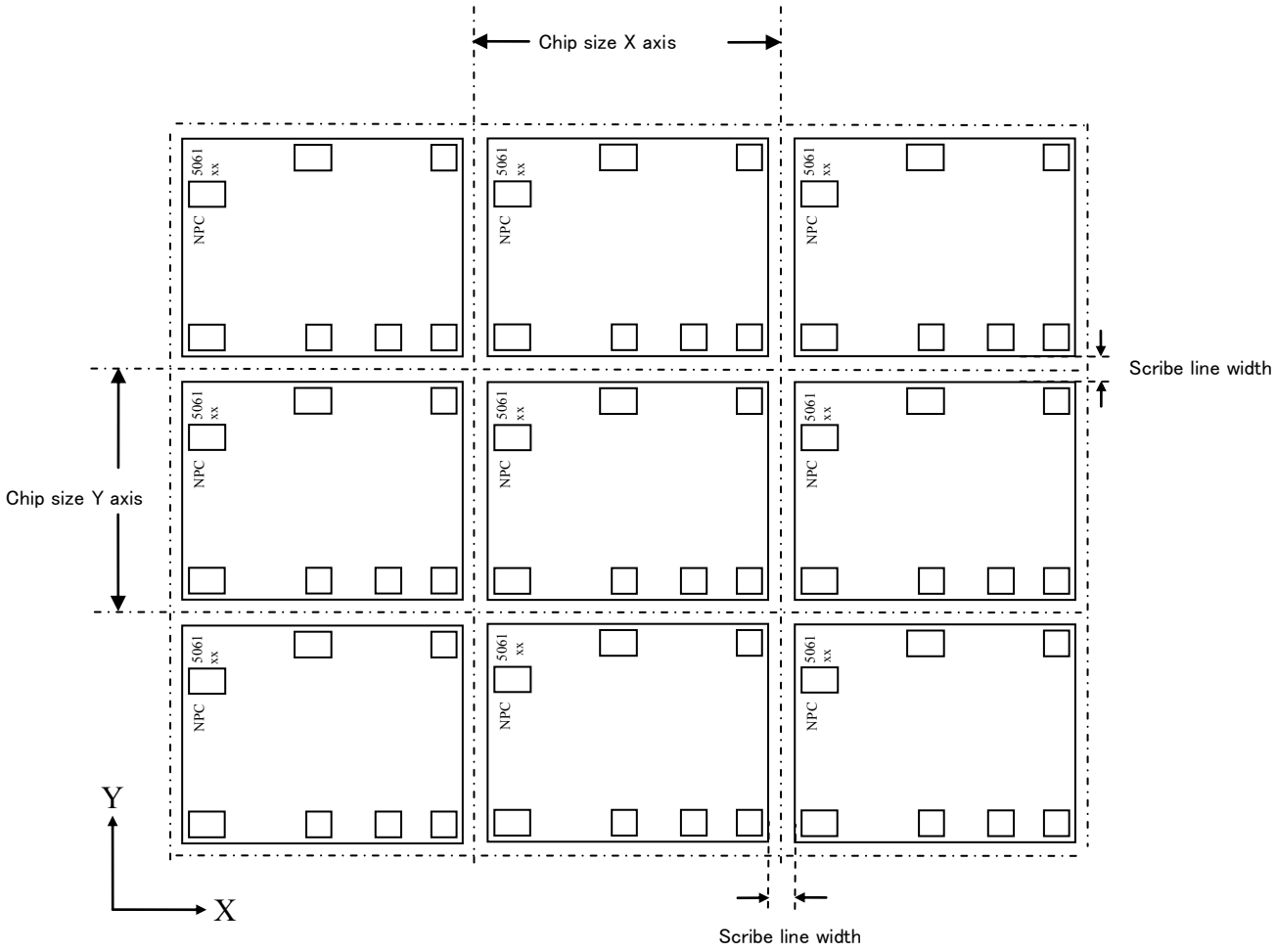


Figure 12-5. **Measurement circuit 5**

13. WAFER SURFACE DIAGRAM

Wafer size: 150mm ± 0.5mm
Scribe line width: 70μm





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In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

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