OVERVIEW

The 5060Hxx series are LV-PECL output oscillator ICs with 125°C operating temperature that support a wide output frequency range ideal for high-frequency applications typical in high-speed communications devices. They employ an oscillator circuit optimized for compact, 3rd overtone crystal elements, making them ideal for use as compact, crystal oscillator modules. The oscillator circuit uses voltage regulator drive to achieve a low drive level.

FEATURES

- Operating supply voltage range: 2.25 to 3.63V
- Recommended oscillation frequency range (varies with version)
  25MHz to 250MHz fundamental oscillation
  50MHz to 220MHz 3rd overtone oscillation
- -40 to 125°C operating temperature range
- LV-PECL output
- Oscillation detection circuit built-in
- Frequency divider built-in
  Selectable by version: f_0, $f_0/2$
- Standby function
  High impedance in standby mode, oscillator stops
- Power-saving pull-up resistor built-in (OE pin)
- Wafer form (WF5060Hxx)
- Chip form (CF5060Hxx)

SERIES CONFIGURATION

Oscillation mode	Recommended oscillation frequency range f_0[*1] [MHz]	C_0 cancellation circuit	Recommend C_0 value[*2] [pF]	Output frequency (pF)	
				f_0	$f_0/2$
fundamental	25 to 100	No	to 1.5[*3] (to 2.0)[*4]	-	5060HL7[*5]
	100 to 175			5060HM6[*5]	-
	175 to 250	Yes	1.2 to 1.8	5060HF6[*6]	-
3rd overtone fundamental	175 to 220				
	50 to 63	No	to 2.0[*3] (to 2.5)[*4]	5060HA6	-
	62 to 80			5060HB6	-
	80 to 107	Yes	1.0 to 2.0[*3] (0.8 to 2.5)[*4]	5060HC6	-
	100 to 140			5060HD6	-
	140 to 175			5060HE6	-

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. The oscillator circuit is optimized for 5032 to 3225 size crystal. In use of 7050 size crystal with large C_0 value, because the risk that oscillation margin is insufficient increases, it must be carefully evaluated.

*3. Normal recommended range based on the oscillator circuit design.

*4. Values in ( ) are full range values. If using these ranges, careful evaluation is recommended before implementation.

*5. L and M versions are recommended for use with crystals such as compact AT cut crystals with extremely low C_0 and R_1, and inverted mesa crystals.

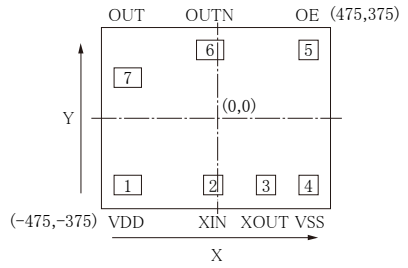
*6. The F version is adjusting C_0 cancellation circuit rather hard to have a negative resistance by a high frequency.
A self-oscillation tends to happen compared with the other versions, so please be careful about a lower limit of C_0. A self-oscillation becomes easy to happen coldly, so please be careful and do initial evaluation.
R_1 in the F version is a fundamental wave (≤ 250MHz) 50 Ω in 3rd overtone (≤ 220MHz), and 20 Ω is an aim.

ORDERING INFORMATION

Device	Package	Version Name
WF5060Hxx-3	Wafer form	WF5060H□□-3 Form WF:Wafer form CF:Chip (Die) form Output frequency 6 : f_0 7 : $f_0/2$ Oscillation frequency L : 25 to 100MHz, M : 100 to 175MHz A : 50 to 63MHz, B : 62 to 80MHz, C : 80 to 107MHz D : 100 to 140MHz, E : 140 to 175MHz F : 175 to 220MHz (3rd overtone) 175 to 250MHz (Fundamental)
CF5060Hxx-3	Chip form	

PAD LAYOUT

(Unit: µm)



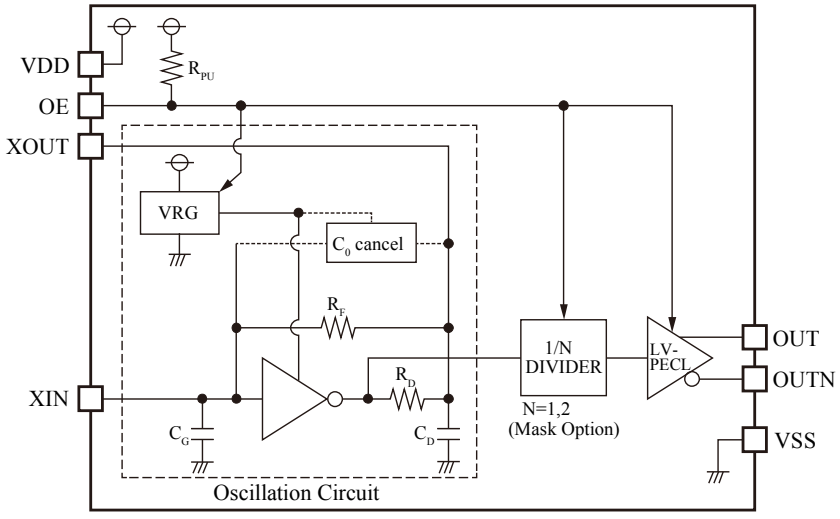
Chip size: 0.95mm×0.75mm
Chip thickness : 180µm
PAD size : 110µm×80µm (No.1, 6, 7)
80µm×80µm (No.2, 3, 4, 5)
Chip base : Vss level
* Coordinates at the chip center are (0,0).

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O*1	Function	PAD coordinates [µm]	
				X	Y
1	VDD	-	(+) supply voltage	-363.7	-283.5
2	XIN	I	Crystal connection pins	-11.7	-283.5
3	XOUT	O	Crystal is connected between XIN and XOUT.	208.2	-283.5
4	VSS	-	(-) ground	383.5	-283.5
5	OE	I	Input pin controlled output state (oscillator stops when Low), Power-saving pull-up resistor built-in	383.5	283.5
6	OUTN	O	LV-PECL output pin (Inverting output)	-29.1	283.5
7	OUT	O	LV-PECL output pin (Non-inverting output)	-368.5	168.2

*1. I: Input pin O: Output pin

BLOCK DIAGRAM



*. The C_G and C_D of the F version is only parasitic capacitance.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range*1	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range*1*2	V_{IN}	Input pins	-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	Output pins	-0.3 to V_{DD}+0.3	V
Junction temperature*3	T_j		+150	℃
Storage temperature range*4	T_{STG}	Chip form, Wafer form	-55 to~ +150	℃

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Oscillator frequency*1	f_0	5060HL7		25	-	100	MHz
		5060HM6		100	-	175	
		5060HA6		50	-	63	
		5060HB6		62	-	80	
		5060HC6		80	-	107	
		5060HD6		100	-	140	
		5060HE6		140	-	175	
		5060HF6	3rd overtone	175	-	220	
			Fundamental	175	-	250	
Output frequency	f_{OUT}	5060HL7		12.5	-	50	MHz
		5060HM6		100	-	175	
		5060HA6		50	-	63	
		5060HB6		62	-	80	
		5060HC6		80	-	107	
		5060HD6		100	-	140	
		5060HE6		140	-	175	
		5060HF6	3rd overtone	175	-	220	
			Fundamental	175	-	250	
Operating supply voltage	V_{DD}	Between VDD and VSS*2		2.25	-	3.63	V
Input voltage	V_{IN}	Input pins		0	-	V_{DD}	V
Operating temperature	T_a			-40	-	+125	℃
Output load resistance	R_L	OUT pin, OUTN pin, Terminated to V_{DD}-2V		49.5	-	50.5	Ω

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5060H series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics

DC Characteristics

Measurement circuits 1 to 3 in "Conditions" are shown in "MEASUREMENT CIRCUITS."

V_{DD}=2.25 to 3.63V, V_{SS}=0V, T_a= -40 to +125°C unless otherwise noted.

Parameter	Symbol	Conditions			MIN	TYP	MAX	Unit
Current consumption (HL7 ver.)	I_{DDL}_3.3V	Measurement circuit 1 OE=Open f_0=100MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	44.0	54.0	mA
	I_{DDL}_2.5V			V_{DD}=2.5V	-	41.0	51.0	
	I_{DDL}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	56.0	mA
	I_{DDL}_2.5V			V_{DD}=2.5V	-	-	53.0	
Current consumption (HM6 ver.)	I_{DDM}_3.3V	Measurement circuit 1 OE=Open f_0=156.25MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	46.0	55.0	mA
	I_{DDM}_2.5V			V_{DD}=2.5V	-	42.0	50.0	
	I_{DDM}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	57.0	mA
	I_{DDM}_2.5V			V_{DD}=2.5V	-	-	53.0	
Current consumption (HA6 ver.)	I_{DDA}_3.3V	Measurement circuit 1 OE=Open f_0=62.5MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	45.5	54.5	mA
	I_{DDA}_2.5V			V_{DD}=2.5V	-	42.5	51.0	
	I_{DDA}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	56.5	mA
	I_{DDA}_2.5V			V_{DD}=2.5V	-	-	53.0	
Current consumption (HB6 ver.)	I_{DDB}_3.3V	Measurement circuit 1 OE=Open f_0=80MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	46.0	55.0	mA
	I_{DDB}_2.5V			V_{DD}=2.5V	-	43.0	51.5	
	I_{DDB}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	57.5	mA
	I_{DDB}_2.5V			V_{DD}=2.5V	-	-	53.5	
Current consumption (HC6 ver.)	I_{DDC}_3.3V	Measurement circuit 1 OE=Open f_0=106.25MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	49.0	56.0	mA
	I_{DDC}_2.5V			V_{DD}=2.5V	-	45.5	52.0	
	I_{DDC}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	58.0	mA
	I_{DDC}_2.5V			V_{DD}=2.5V	-	-	54.0	
Current consumption (HD6 ver.)	I_{DDD}_3.3V	Measurement circuit 1 OE=Open f_0=125MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	49.0	56.0	mA
	I_{DDD}_2.5V			V_{DD}=2.5V	-	45.5	52.0	
	I_{DDD}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	58.0	mA
	I_{DDD}_2.5V			V_{DD}=2.5V	-	-	54.0	
Current consumption (HE6 ver.)	I_{DDE}_3.3V	Measurement circuit 1 OE=Open f_0=156.25MHz	$T_a \leq$+85°C	V_{DD}=3.3V	-	50.0	57.0	mA
	I_{DDE}_2.5V			V_{DD}=2.5V	-	46.0	52.5	
	I_{DDE}_3.3V		T_a>+85°C	V_{DD}=3.3V	-	-	59.0	mA
	I_{DDE}_2.5V			V_{DD}=2.5V	-	-	54.5	
Current consumption (HF6 ver.)	I_{DDF}_3.3V	Measurement circuit 1, OE=Open f_0=200MHz		V_{DD}=3.3V	-	53.0	66.0	mA
	I_{DDF}_2.5V			V_{DD}=2.5V	-	48.0	61.0	
Standby current	I_{STB}	Measurement circuit 1 OE=Low		$T_a \leq$+85°C	-	-	15	µA
				T_a>+85°C	-	-	30	
High-level output voltage	V_{OH}	Measurement circuit 2 OUT/OUTN pin		$T_a \leq$+85°C	V_{DD} -1.025	V_{DD} -0.950	V_{DD} -0.880	V
				T_a>+85°C	V_{DD} -1.040			
Low-level output voltage	V_{OL}	Measurement circuit 2, OUT/OUTN pin			V_{DD} -1.810	V_{DD} -1.700	V_{DD} -1.620	V
Output leakage current	I_Z	Measurement circuit 3, OE=Low, OUT/OUTN pin			-	-	10	µA
High-level input voltage	V_{IH}	Measurement circuit 1, OE pin			0.7V_{DD}	-	-	V
Low-level input voltage	V_{IL}	Measurement circuit 1, OE pin			-	-	0.3V_{DD}	V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
OE pin pull-up resistance	R_{PU1}	Measurement circuit 1	0.2	1	8	MΩ
	R_{PU2}	Measurement circuit 1	30	70	150	kΩ
Oscillator feedback resistance (HL7 ver.)	R_{FL}	Design value	50	100	200	kΩ
Oscillator feedback resistance (HM6 ver.)	R_{FM}	Design value	50	100	200	kΩ
Oscillator feedback resistance (HA6 ver.)	R_{FA}	Design value	1.2	2.4	3.6	kΩ
Oscillator feedback resistance (HB6 ver.)	R_{FB}	Design value	1.1	2.2	3.3	kΩ
Oscillator feedback resistance (HC6 ver.)	R_{FC}	Design value	1.1	2.2	3.3	kΩ
Oscillator feedback resistance (HD6 ver.)	R_{FD}	Design value	1.1	2.2	3.3	kΩ
Oscillator feedback resistance (HE6 ver.)	R_{FE}	Design value	1.1	2.2	3.3	kΩ
Oscillator feedback resistance (HF6 ver.)	R_{FF}	Design value	0.95	1.9	2.85	kΩ
Oscillator capacitance (HL7 ver.)	C_{GL}	Design value. Excluding parasitic capacitance*1	9.6	12.0	14.4	pF
	C_{DL}		11.2	14.0	16.8	
Oscillator capacitance (HM6 ver.)	C_{GM}	Design value. Excluding parasitic capacitance*1	1.6	2.0	2.4	pF
	C_{DM}		1.6	2.0	2.4	
Oscillator capacitance (HA6 ver.)	C_{GA}	Design value. Excluding parasitic capacitance*1	8.0	10.0	12.0	pF
	C_{DA}		11.2	14.0	16.8	
Oscillator capacitance (HB6 ver.)	C_{GB}	Design value. Excluding parasitic capacitance*1	8.0	10.0	12.0	pF
	C_{DB}		9.6	12.0	14.4	
Oscillator capacitance (HC6 ver.)	C_{GC}	Design value. Excluding parasitic capacitance*1	3.2	4.0	4.8	pF
	C_{DC}		3.2	4.0	4.8	
Oscillator capacitance (HD6 ver.)	C_{GD}	Design value. Excluding parasitic capacitance*1	1.6	2.0	2.4	pF
	C_{DD}		1.6	2.0	2.4	
Oscillator capacitance (HE6 ver.)	C_{GE}	Design value. Excluding parasitic capacitance*1	0.8	1.0	1.2	pF
	C_{DE}		0.8	1.0	1.2	
Oscillator capacitance (HF6 ver.)	C_{GF}	Design value. Excluding parasitic capacitance*1	-	0	-	pF
	C_{DF}		-	0	-	

*1. Confirmed by sampling inspection of the monitor pattern on the wafer.

AC Characteristics

Measurement circuits 4 and 5 in "Conditions" are shown in "MEASUREMENT CIRCUITS."
The conditions for each parameter assume the timing shown in "Timing Diagram."
V_{DD} = 2.25 to 3.63V, V_{SS} = 0V, T_a = -40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions				MIN	TYP	MAX	Unit
Output duty cycle 1 (Differential output)	Duty1	Measurement circuit 4 Measured at differential output signal 0V (crossing point)				45	-	55	%
Output duty cycle 2 (Single-ended output)	Duty2	Measurement circuit 4 Measured at 50% single-ended output swing				45	-	55	%
Output swing	V_{OPP}	Measurement circuit 4, single-ended output signal				0.4	-	-	V
Output rise time[*1]	t_r	Measurement circuit 4, Measured at 20% to 80% single-ended output swing	HA6 HB6 HC6 HD6 HE6 HL7 HM6 ver.	$T_a \leq +85°C$	$2.97V \leq V_{DD} \leq 3.63V$	-	200	400	ps
					$2.375V \leq V_{DD} < 2.97V$	-	250	500	
					$2.25V \leq V_{DD} < 2.375V$	-	300	600	
				$T_a > +85°C$	$2.97V \leq V_{DD} \leq 3.63V$	-	-	500	
					$2.25V \leq V_{DD} < 2.97V$	-	-	600	
			HF6 ver.		$2.97V \leq V_{DD} \leq 3.63V$	-	200	400	
					$2.375V \leq V_{DD} < 2.97V$	-	250	500	
					$2.25V \leq V_{DD} < 2.375V$	-	300	600	
Output fall time[*2]	t_f	Measurement circuit 4, Measured at 80% to 20% single-ended output swing	HA6 HB6 HC6 HD6 HE6 HL7 HM6 ver.	$T_a \leq +85°C$	$2.97V \leq V_{DD} \leq 3.63V$	-	200	400	ps
					$2.375V \leq V_{DD} < 2.97V$	-	250	500	
					$2.25V \leq V_{DD} < 2.375V$	-	300	600	
				$T_a > +85°C$	$2.97V \leq V_{DD} \leq 3.63V$	-	-	500	
					$2.25V \leq V_{DD} < 2.97V$	-	-	600	
			HF6 ver.		$2.97V \leq V_{DD} \leq 3.63V$	-	200	400	
					$2.375V \leq V_{DD} < 2.97V$	-	250	500	
					$2.25V \leq V_{DD} < 2.375V$	-	300	600	
Output disable time	t_{OD}	Measurement circuit 5 Time until Hi-Z is output at OE(fall)=V_{IL} (Refer to the timing chart for details.)				-	-	200	ns

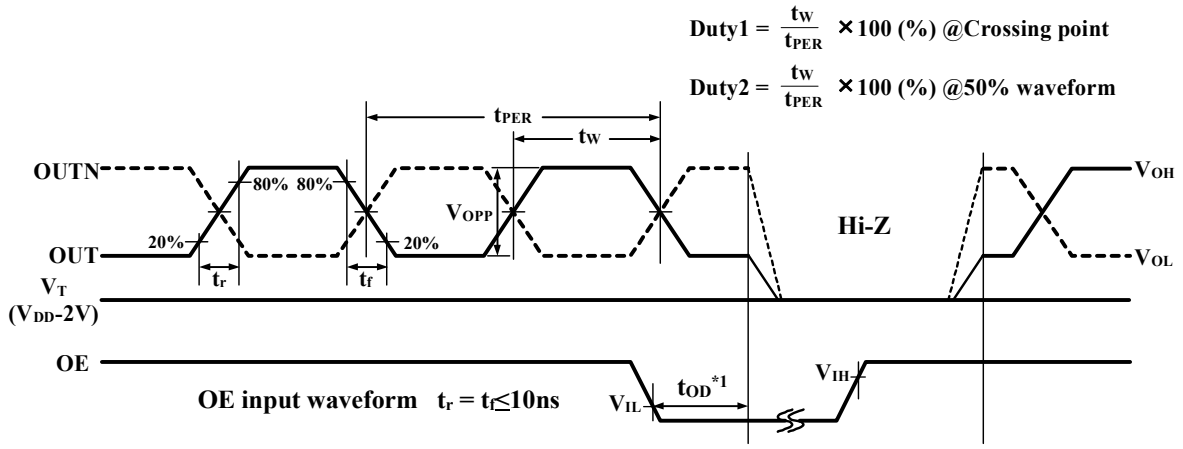
*1. Measurement circuit 4, Measured between 20% and 80% amplitude of single-ended signal

*2. Measurement circuit 4, Measured between 80% and 20% amplitude of single-ended signal

* The ratings above are values obtained by measurements using an NPC evaluation standard crystal element, standard testing jig, and evaluation package. Ratings may have wide tolerances due to crystal element characteristics, evaluation jig, and package parasitic capacitance, so thorough evaluation is recommended.

Timing Diagram

The timing diagram applies to the "Conditions" in the table in "AC Characteristics."



*1. The OUT/OUTN output goes high impedance after the OE is fallen and then the output disable time "t_{OD}" has elapsed. The output signal is pulled down to V_T (terminated voltage) by load resistance.

FUNCTIONAL DESCRIPTION

OE Function

When OE goes LOW, the OUT/OUTN outputs stop and become high impedance. This function is used to disable the operation of the device.

OE	OUT/OUTN	Oscillator
High or Open	f_0, $f_0/2$	Operating
Low	Hi-Z	Stopped

Power Saving Pull-up Resistor

The OE terminal pull-up resistance switches between R_{PU1} and R_{PU2}, depending on the input level (HIGH or LOW).

When the OE terminal is held LOW, the built-in OE terminal pull-up resistance increases (R_{PU1}), reducing the current consumed by the pull-up resistance when the outputs are disabled.

When the device is operating with the OE terminal HIGH or open circuit, the pull-up resistance decreases (R_{PU2}), reducing internal susceptibility to the effects of external noise. The OE terminal is held HIGH internally to prevent problems that might otherwise cause the outputs to stop abruptly.

Oscillation Detection Function

The IC has a built-in oscillation detection circuit. The oscillation detection circuit disables the output circuit when the oscillator starts until the oscillation becomes stable. This function limits the danger of unstable oscillation when the oscillator starts after power is first applied or the output is enabled.

C_0 cancellation circuit

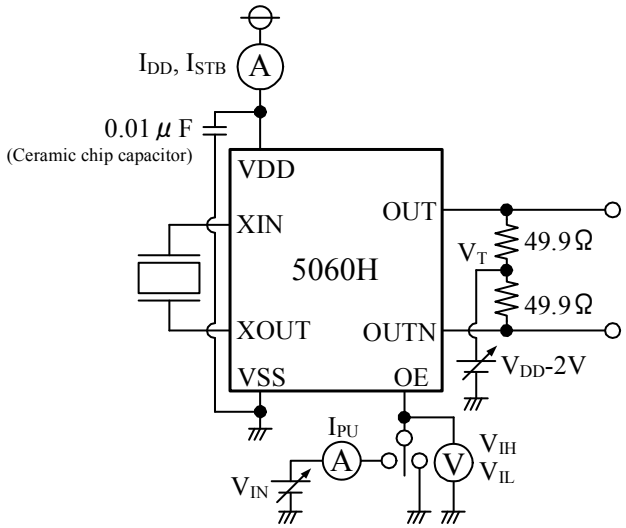
Oscillation circuit with a built-in C_0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C_0. It reduces the C_0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C_0.

This cancellation circuit makes it easier to maintain the oscillation margin.

MEASUREMENT CIRCUITS

MEASUREMENT CIRCUIT 1

Measurement Parameter : I_{DD}, I_{STB}, V_{IH}, V_{IL}, R_{PU1}, R_{PU2}



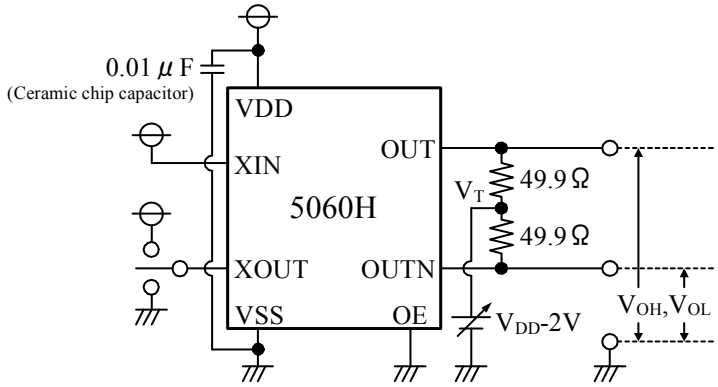
$$R_{PU1} = \frac{V_{DD}}{I_{PU}} \quad (V_{IN} = 0V)$$

$$R_{PU2} = \frac{V_{DD} - 0.7V_{DD}}{I_{PU}} \quad (V_{IN} = 0.7V_{DD})$$

V_{IH} : $V_{SS} \rightarrow V_{DD}$ voltage that changes output state
V_{IL} : $V_{DD} \rightarrow V_{SS}$ voltage that changes output state

MEASUREMENT CIRCUIT 2

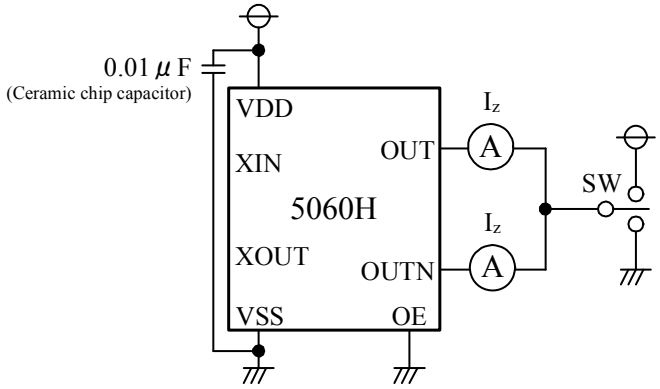
Measurement Parameter : V_{OH}, V_{OL}



XOUT=High { OUT =High, OUTN=Low
XOUT=Low { OUT =Low, OUTN=High

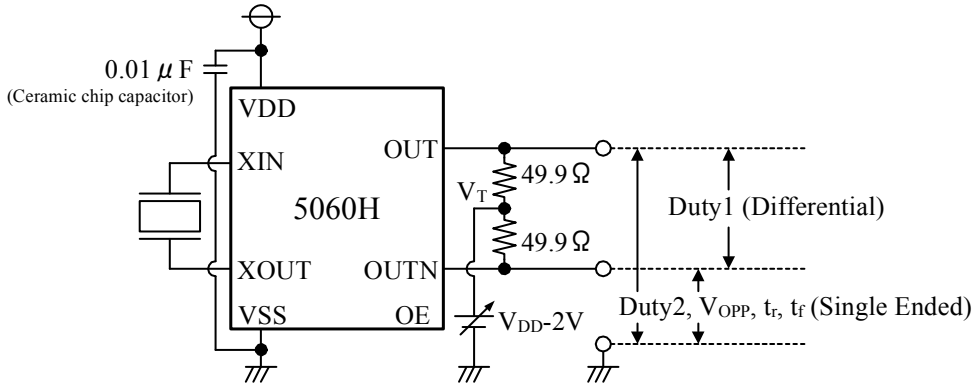
MEASUREMENT CIRCUIT 3

Measurement Parameter : I_Z



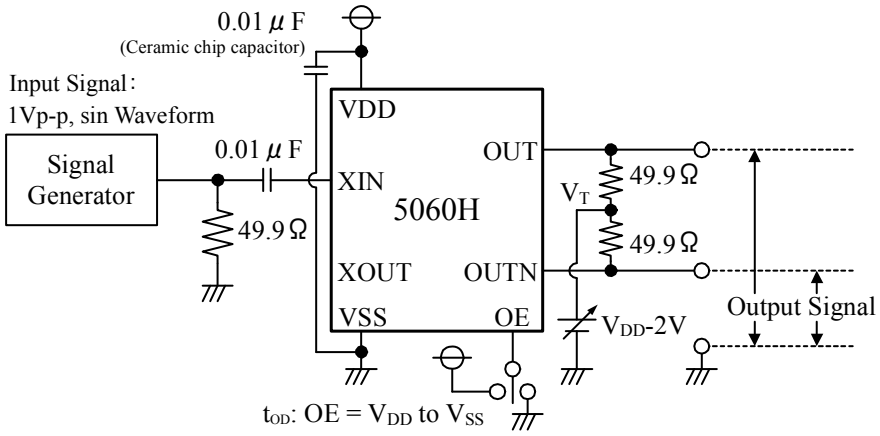
MEASUREMENT CIRCUIT 4

Measurement Parameter : Duty1, Duty2, V_{OPP}, t_r, t_f



MEASUREMENT CIRCUIT 5

Measurement Parameter : t_{OD}



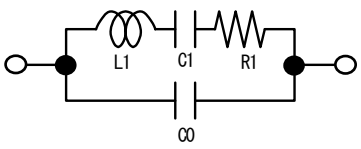
REFERENCE DATA

The following characteristics are measured using the crystal below.
Note that the characteristics will vary with the crystal used.

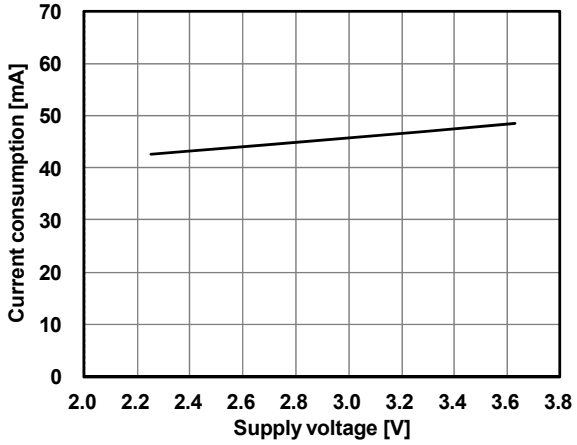
Crystal used for measurement (3rd overtone)

Parameter	f_0=125.00MHz	f_0=156.25MHz
C_0(pF)	1.8	1.2
R_1(Ω)	35	60

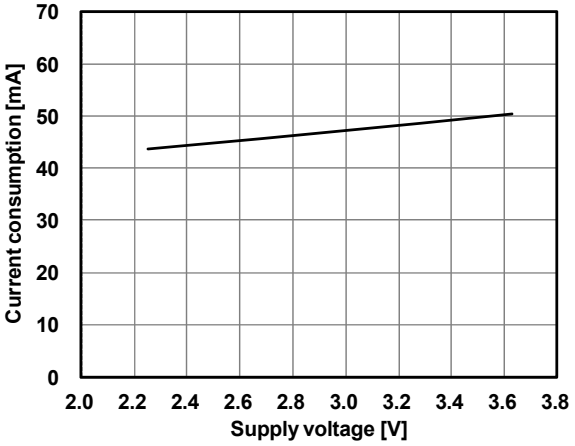
Crystal parameters



Current Consumption

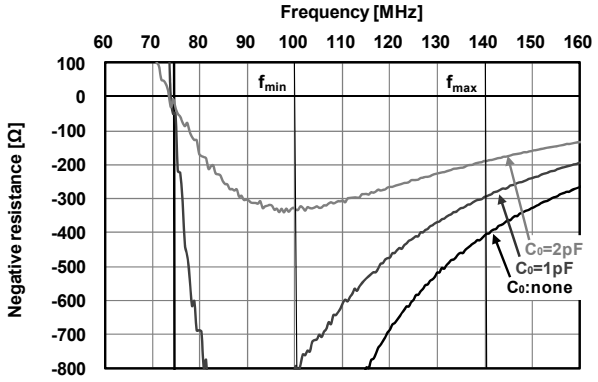


5060HD6, f_{OUT}=125MHz, T_a=25°C

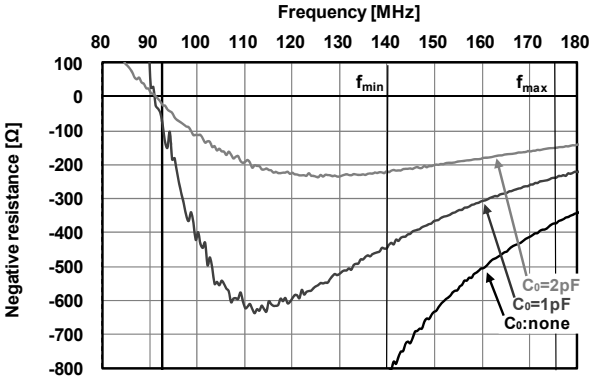


5060HE6, f_{OUT}=156.25MHz, T_a=25°C

Negative Resistance



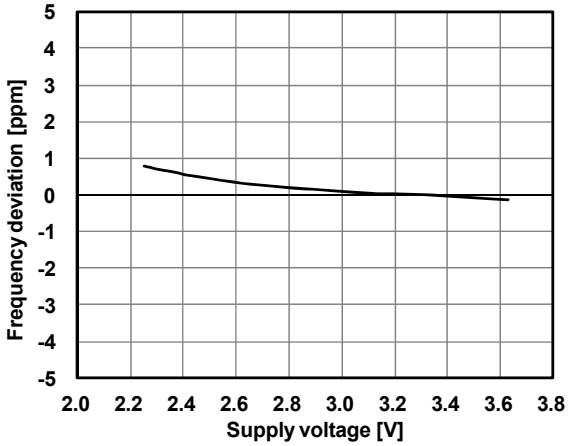
5060HD6, V_{DD}=3.3V, T_a=25°C



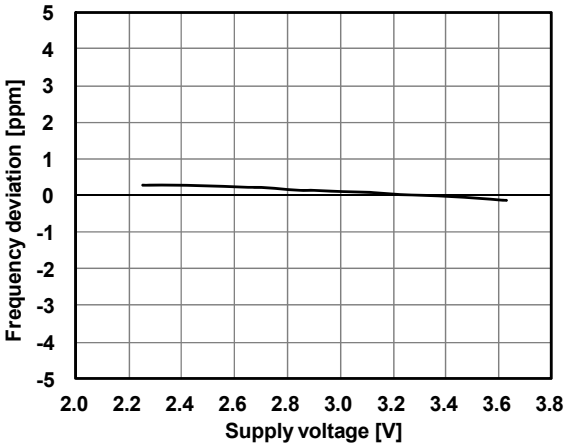
5060HE6, V_{DD}=3.3V, T_a=25°C

The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XIN and XOUT pins. They were performed with Agilent 4396B using the NPC test jig.
They may vary in a measurement jig, and measurement environment.

Frequency Deviation by Voltage

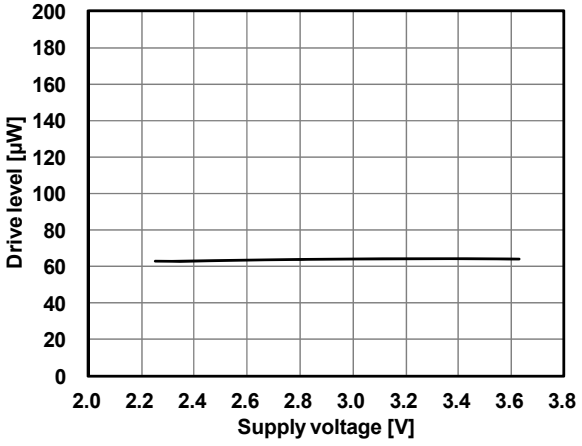


5060HD6, f_{OUT}=125MHz, T_a=25°C, 3.3V std.

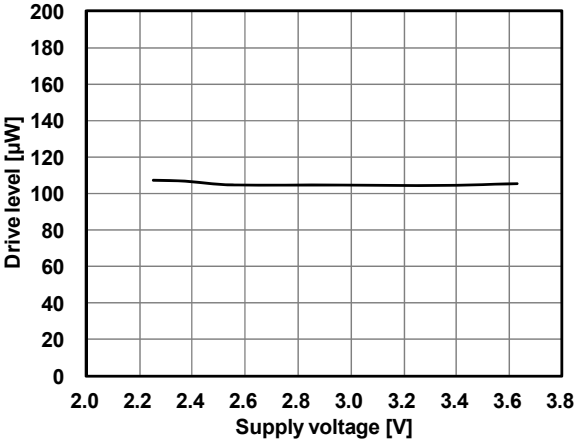


5060HE6, f_{OUT}=156.25MHz, T_a=25°C, 3.3V std.

Drive Level

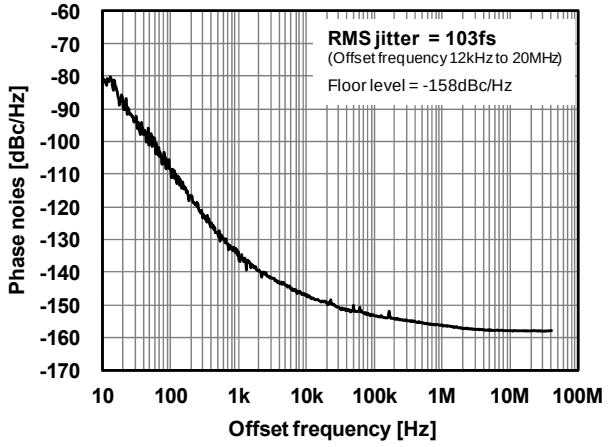


5060HD6, f_{OUT}=125MHz, T_a=25°C

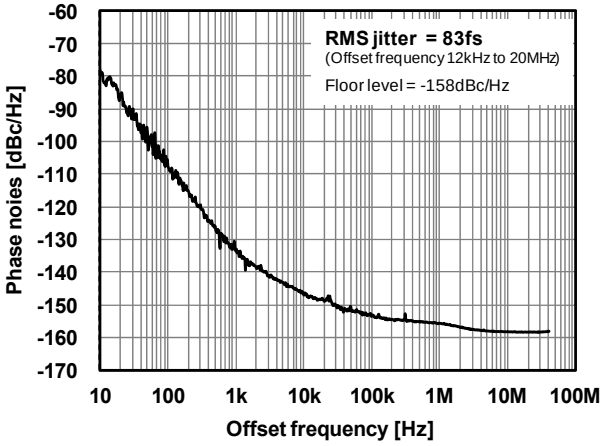


5060HE6, f_{OUT}=156.25MHz, T_a=25°C

Phase Noise



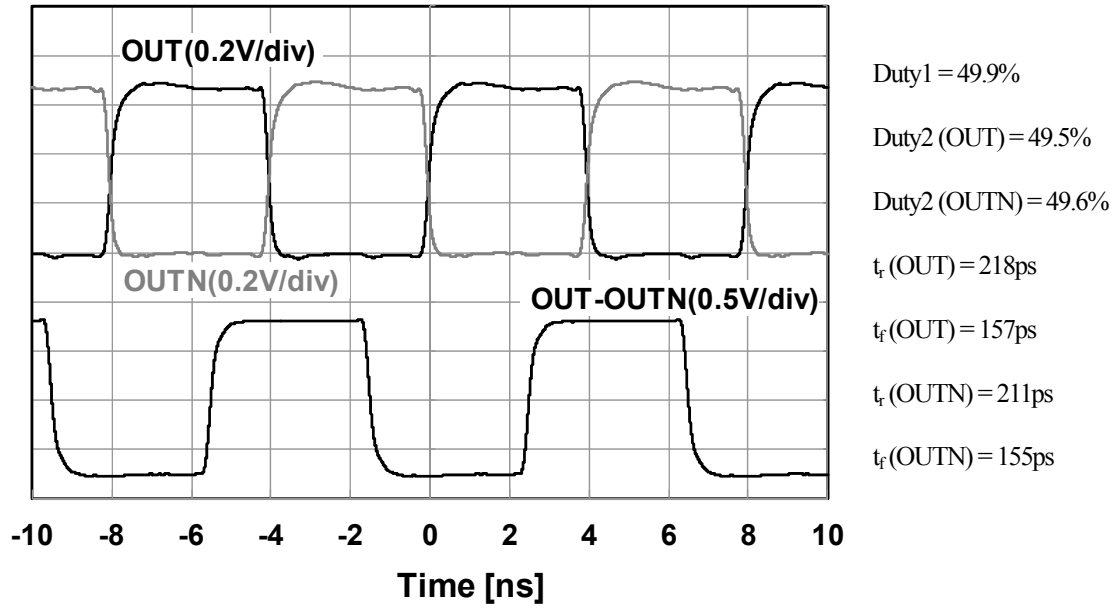
5060HD6, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C



5060HE6, f_{OUT}=156.25MHz, V_{DD}=3.3V, T_a=25°C

Measurement instrument: Agilent E5052B Signal Source Analyzer

Output Waveform



Duty1 = 49.9%

Duty2 (OUT) = 49.5%

Duty2 (OUTN) = 49.6%

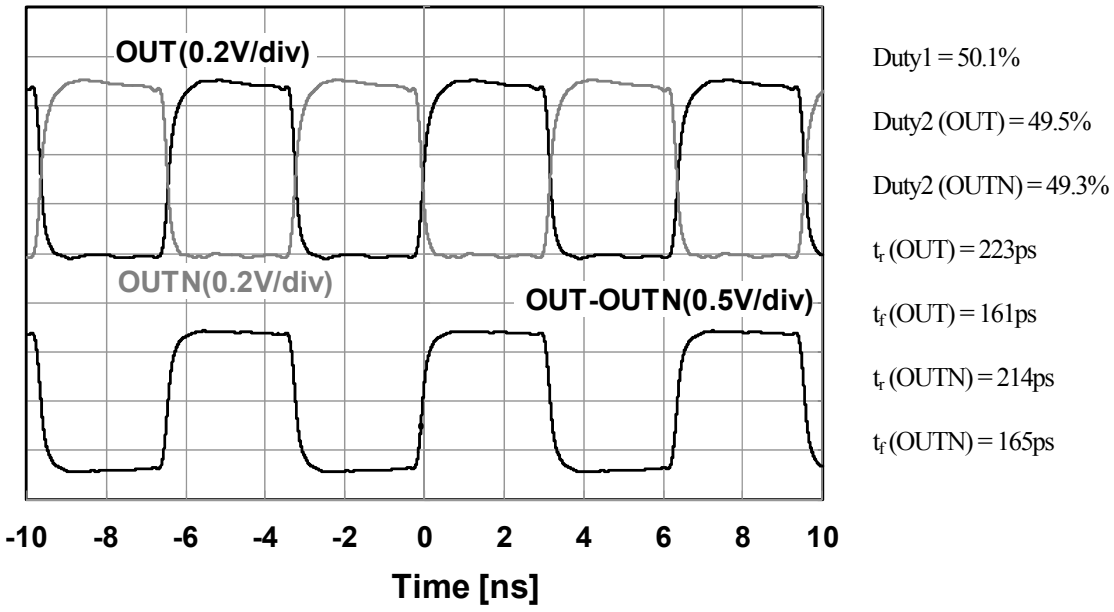
t_r (OUT) = 218ps

t_f (OUT) = 157ps

t_r (OUTN) = 211ps

t_f (OUTN) = 155ps

5060HD6, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C



Duty1 = 50.1%

Duty2 (OUT) = 49.5%

Duty2 (OUTN) = 49.3%

t_r (OUT) = 223ps

t_f (OUT) = 161ps

t_r (OUTN) = 214ps

t_f (OUTN) = 165ps

5060HE6, f_{OUT}=156.25MHz, V_{DD}=3.3V, T_a=25°C

Measurement equipment: Oscilloscope DSO80604B (Agilent)
Differential probe 1134A (Agilent)
Probe head E2675A (Agilent)

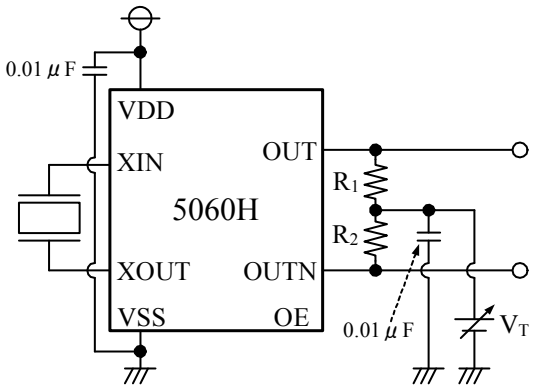
APPLICATION CIRCUIT (TERMINATION CIRCUIT)

This section describes sample termination circuits that can be used with the device. The termination circuits use chip resistors, and care should be taken to prevent resistance value mismatch. Also, the length of wiring between the outputs and termination resistance should be as short as possible to prevent mismatch. Chip capacitors are used for the bypass capacitors and should be placed as close as possible to the device terminals.

These application circuit examples are provided as reference circuit diagrams only, and do not represent circuits guaranteed by NPC.
We accept no responsibility from any damage or less resulting from their use. Always use devices after conducting thorough evaluation.

TERMINATION CIRCUIT1 (RECOMMENDED CIRCUIT)

This is a standard LV-PECL termination circuit identical to the circuit in measurement circuit 4.
The characteristics values in "Electrical Characteristics" are based on the measurement results obtained using this circuit.
It uses an external V_{DD}-2V supply and provides a 50Ω termination.
Problems due to differences in the output characteristics are minimized, allowing characteristics close to ideal to be obtained.
Additional wiring pattern to apply the termination voltage V_T must be prepared on the evaluation board.



$R_1 = R_2 = 50\,\Omega$

$V_T = V_{DD}\text{-}2V \begin{cases} 1.3V\ @\ V_{DD}=3.3V \\ 0.5V\ @\ V_{DD}=2.5V \end{cases}$

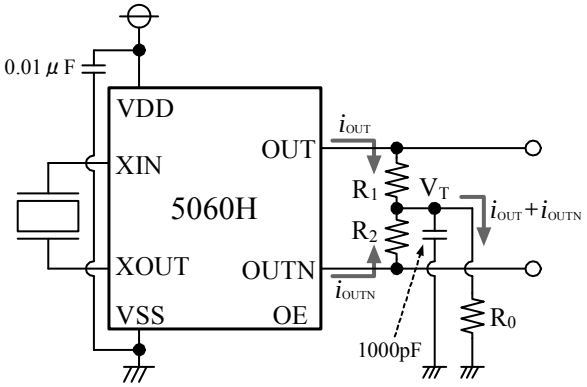
TERMINATION CIRCUIT2

This method creates the V_{DD}-2V termination voltage using a voltage drop .$R_0 \times (i_{OUT} + i_{OUTN})$ obtained by connecting a resistor between V_T and V_{SS}. As there is no requirement to supply the termination voltage V_T from an external supply, the circuit can operate from a single power supply. However, the termination voltage V_T wiring pattern must be prepared on the evaluation board.

Differences in the output characteristics may occur due to differences in the values of R_0 and V_{DD}.

Operation at V_{DD}=3.3V and 2.5V requires different values of resistance for R_0.

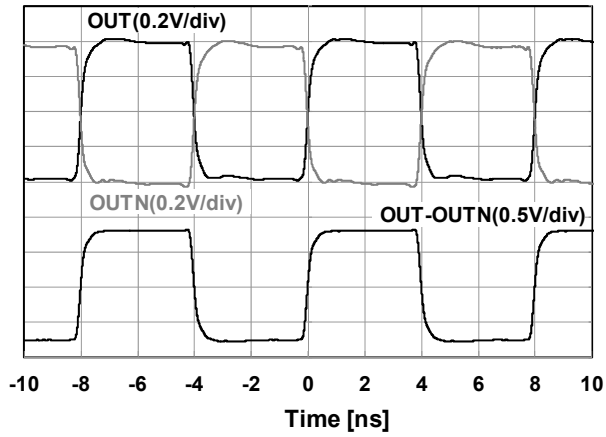
It is possible to obtain improved characteristics by connecting a 1000pF capacitor directly to the termination resistance $R_1(R_2)$-V_T junction.



$$V_{DD} = 3.3V \begin{cases} R_0 = 50\,\Omega \\ R_1 = R_2 = 50\,\Omega \end{cases}$$

$$V_{DD} = 2.5V \begin{cases} R_0 = 22\,\Omega \\ R_1 = R_2 = 50\,\Omega \end{cases}$$

$$V_T = R_0 \times (i_{OUT}+i_{OUTN})$$



Duty1 = 50.0%

Duty2 (OUT) = 49.5%

Duty2 (OUTN) = 49.7%

t_r (OUT) = 197ps

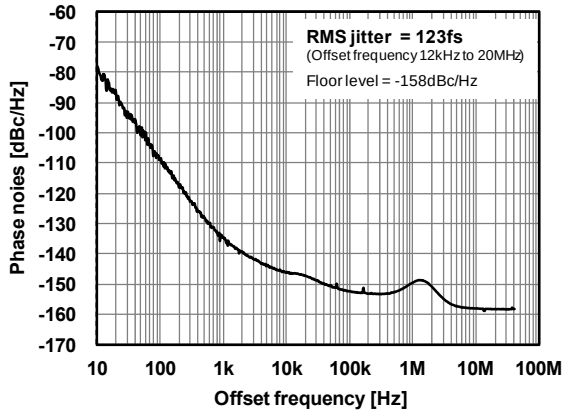
t_f (OUT) = 162ps

t_r (OUTN) = 194ps

t_f (OUTN) = 159ps

5060HD6, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C

Output waveform reference data by termination circuit 2

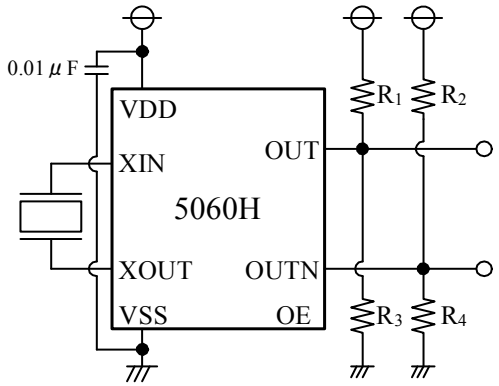


5060D6, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C

Phase noise reference data by termination circuit 2

TERMINATION CIRCUIT3

This circuit employs a voltage divider using pairs of resistors to obtain a parallel resistance of 50Ω.
As there is no requirement to supply the termination voltage V_T from an external supply, the circuit can operate from a single power supply.
Also, termination voltage V_T pattern wiring is not required.
Differences in the output characteristics may occur due to differences in the values of R_1 to R_4 and V_{DD}.
Operation at V_{DD}=3.3V and 2.5V requires different values of resistance for R_1 to R_4.



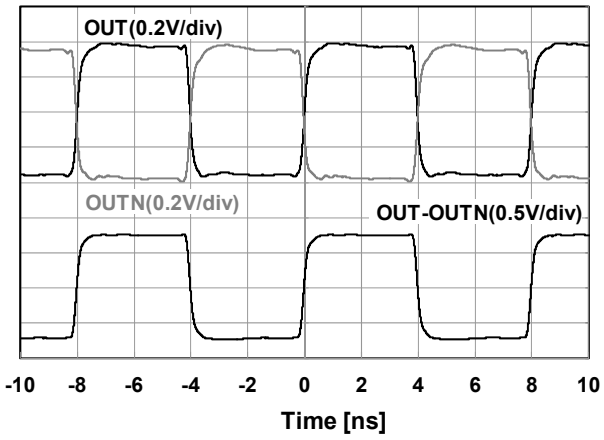
$$V_{DD} = 3.3V \begin{cases} R_1 = R_2 = 130\,\Omega \\ R_3 = R_4 = 83\,\Omega \end{cases}$$

$$V_{DD} = 2.5V \begin{cases} R_1 = R_2 = 250\,\Omega \\ R_3 = R_4 = 62\,\Omega \end{cases}$$

$$V_{T(OUT)} = V_{DD} \times \frac{R_1}{R_1 + R_3}$$

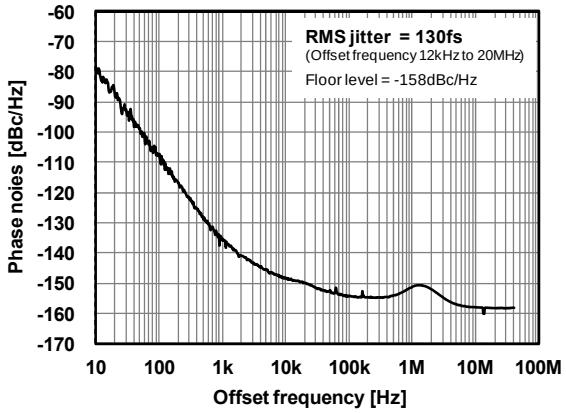
$$V_{T(OUTN)} = V_{DD} \times \frac{R_2}{R_2 + R_4}$$

$$V_T \mathrel{\dot{\approx}} V_{DD} - 2V$$



Duty1 = 50.1%
Duty2 (OUT) = 49.7%
Duty2 (OUTN) = 49.8%
t_r (OUT) = 218ps
t_f (OUT) = 208ps
t_r (OUTN) = 216ps
t_f (OUTN) = 198ps

5060HD6, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C
Output waveform reference data by termination circuit 3

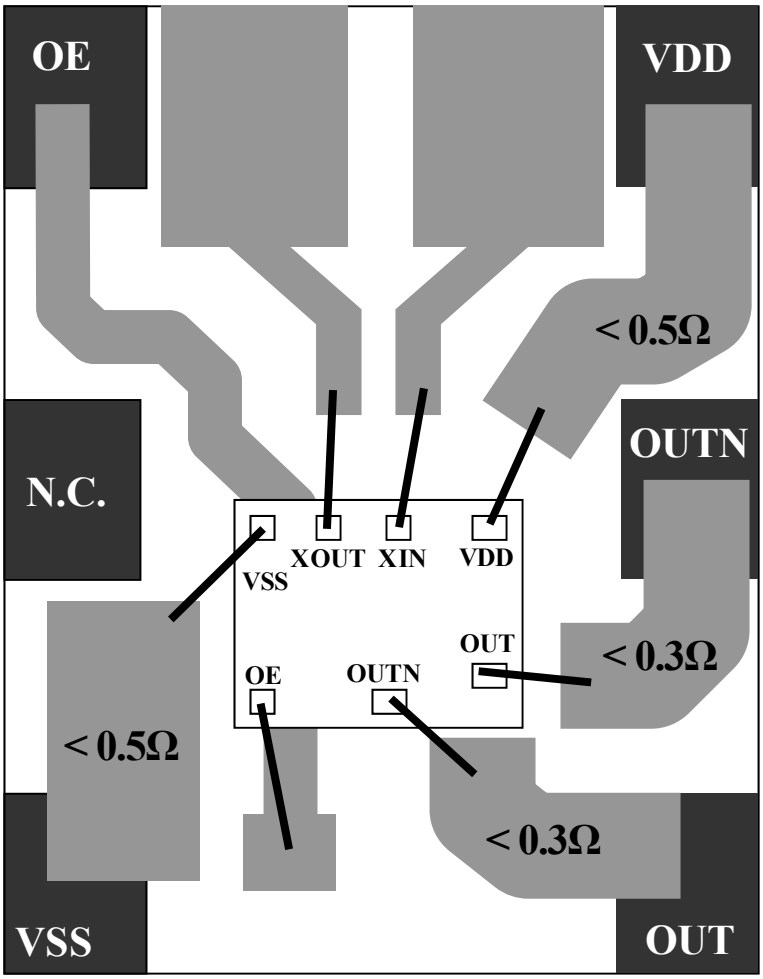


5060HD6, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C
Phase noise reference data by termination circuit 3

MOUNTING PRECAUTIONS

This device is an oscillator IC designed for use in miniature crystal oscillators, and is susceptible to parasitic components caused by device mounting conditions. Observe the following points in order to obtain the best characteristics.

- The VDD and VSS wiring resistance (pattern resistance) should be less than 0.5Ω.
- The OUT and OUTN wiring resistance (pattern resistance) should be less than 0.3Ω.
- The OUT and OUTN pattern wiring including the bonding, should be of equal length in order to obtain best device characteristics.



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