

OVERVIEW

The 5054H series, 5054xF are miniature crystal oscillator module ICs supported 40MHz to 170MHz 3rd overtone oscillation mode. The Oscillator circuit stage has voltage regulator drive, significantly reducing current consumption and crystal current, compared with existing devices, and significantly reducing the oscillator characteristics supply voltage dependency. There are 2 pad layout package options available for optimized mounting, making these devices ideal for miniature crystal oscillators.

FEATURES

- Wide range of operating supply voltage: 1.70 to 3.63V (HxA to HxE ver.), 2.25 to 3.63V (xF ver.)
- Recommended oscillation frequency range (3rd overtone oscillator): 40 to 135MHz (HxA to HxE ver.), 133 to 170MHz (xF ver.)
- Operating temperature range: -40 to 125°C (HxA to HxE ver.), -40 to 105°C (xF ver.)
- Regulated voltage drive oscillator circuit for reduced power consumption and crystal drive current
- Standby function High impedance in standby mode, oscillator stops
- Optimized low crystal drive current oscillation for miniature crystal units
- Output drive capability: $\pm 8\text{mA}$
- 50 $\pm$ 5% output duty (1/2V_{DD})
- 15pF output load capacitance
- 2 pad layout options for mounting 5054(H)Ax for Flip Chip Bonding, 5054(H)Cx for Wire Bonding
- Wafer form WF5054(H)xx
- Chip form CF5054(H)xx

APPLICATIONS

- 5.0 $\times$ 3.2, 3.2 $\times$ 2.5, 2.5 $\times$ 2.0 size miniature crystal oscillator modules

SERIES CONFIGURATION

Operating supply voltage range[V]	Recommended oscillation frequency range *1 [MHz]	C ₀ cancellation/ Recommended C ₀ value[pF]	PAD layout and Version name *2	
			Flip Chip Bonding	Wire Bonding
1.70 to 3.63	40 to 50	No/ ≤ 2	5054HAA	5054HCA
1.70 to 3.63	50 to 65	No/ ≤ 2	5054HAB	5054HCB
1.70 to 3.63	65 to 85	Yes/1 to 2	5054HAC	5054HCC
1.70 to 3.63	85 to 105	Yes/1 to 2	5054HAD	5054HCD
1.70 to 3.63	105 to 135	Yes/1 to 2	5054HAE	5054HCE
2.25 to 3.63	133 to 170	Yes/1 to 2	5054AF	5054CF

*1. The oscillation frequency is a yardstick value derived from the crystal used for Seiko NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. It becomes WF5054(H)xx in case of the wafer form and CF5054(H)xx in case of the chip form.

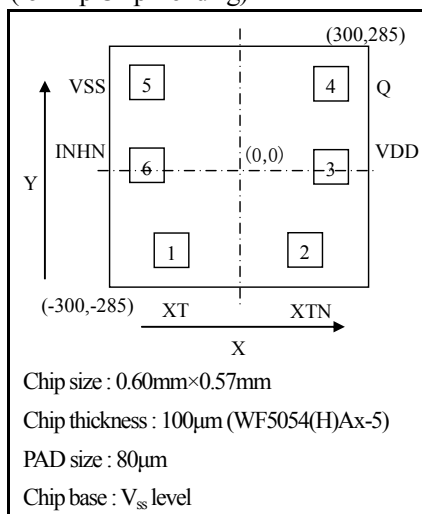
ORDERING INFORMATION

Device	Package	Version name
WF5054(H)xx-x	Wafer form	WF5054(H)□□-□□ Form WF : Wafer form CF : Chip(Die) form Chip thickness 5: 100μm Oscillation frequency range PAD layout A: for Flip Chip Bonding C: for Wire Bonding
CF5054(H)xx-x	Chip form	

PAD LAYOUT

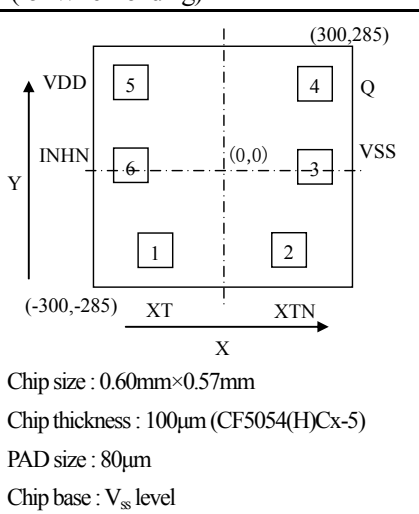
▪ WF5054(H)Ax

(for Flip Chip Bonding)



▪ CF5054(H)Cx

(for Wire Bonding)



· Coordinates at the chip center are (0,0).

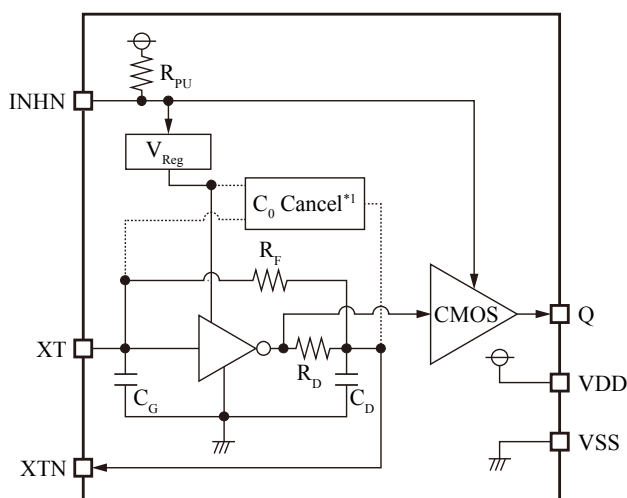
PAD COORDINATES

PAD No.	PAD coordinates[µm]	
	X	Y
1	-145.2	-193.5
2	145.2	-193.5
3	208.5	-1.1
4	208.5	193.5
5	-208.5	193.5
6	-208.5	-1.1

PIN DESCRIPTION

PAD No.		Pin	Function
5054(H)Ax	5054(H)Cx		
1	1	XT	Crystal connection pins. Crystal is connected between XT and XTN.
2	2	XTN	
3	5	VDD	(+) supply voltage
4	4	Q	Output pin
5	3	VSS	(-) ground
6	6	INHN	Input pin controlled output state (oscillator stops when Low), Power-saving pull-up resistor built-in

BLOCK DIAGRAM



*1. The 5054HxA, HxB versions don't have built-in C_0 cancellation circuit.

SPECIFICATIONS

Absolute Maximum Ratings

 $V_{SS}=0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range ^{*1}	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range ^{*1*2}	V_{IN}	Input pins	-0.3 to $V_{DD}+0.3$	V
Output voltage range ^{*1*2}	V_{OUT}	Output pins	-0.3 to $V_{DD}+0.3$	V
Output current ^{*3}	I_{OUT}	Q pin	± 20	mA
Junction temperature ^{*3}	T_j		150	°C
Storage temperature range ^{*4}	T_{STG}	Chip form, Wafer form	-55 to +150	°C

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded.

Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

 $V_{SS}=0V$

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Oscillator frequency*1	f _{OSC}	V _{DD} =1.70 to 3.63V	5054HxA ver.	40	-	50	MHz
			5054HxB ver.	50	-	65	
			5054HxC ver.	65	-	85	
			5054HxD ver.	85	-	105	
			5054HxE ver.	105	-	135	
		V _{DD} =2.25 to 3.63V	5054xF ver.	133	-	170	
Output frequency	f _{OUT}	V _{DD} =1.70 to 3.63V, C _{LOUT} ≤15pF	5054HxA ver.	40	-	50	MHz
			5054HxB ver.	50	-	65	
			5054HxC ver.	65	-	85	
			5054HxD ver.	85	-	105	
			5054HxE ver.	105	-	135	
		V _{DD} =2.25 to 3.63V, C _{LOUT} ≤15pF	5054xF ver.	133	-	170	
Operating supply voltage	V _{DD}	Between VDD and VSS*2	5054HxA ~ 5054HxE ver.	1.70	-	3.63	V
			5054xF ver.	2.25			
Input voltage	V _{IN}	Input pins		V _{SS}	-	V _{DD}	V
Operating temperature	T _a	5054HxA ~ 5054HxE ver.		-40	-	+125	°C
		5054xF ver.			-	+105	
Output load capacitance	C _L	Q output		-	-	15	pF

*1. The oscillation frequency is a yardstick value derived from the crystal used for Seiko NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. Mount a ceramic chip capacitor that is larger than $0.01\mu F$ proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5054 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics

DC Characteristics (HxA to HxE versions)

$V_{DD}=1.70$ to 3.63 V, $V_{SS}=0$ V, $T_a=-40$ to $+125^{\circ}\text{C}$ unless otherwise noted.

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HIGH-level output voltage	V_{OH}	Q pin, measurement circuit 3, $I_{OH}=-8\text{mA}$, $T_a=-40$ to $+85^{\circ}\text{C}$	$V_{DD}-0.4$	-	V_{DD}	V
		Q pin, measurement circuit 3, $I_{OH}=-8\text{mA}$	$V_{DD}-0.45$	-	V_{DD}	
LOW-level output voltage	V_{OL}	Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$, $T_a=-40$ to $+85^{\circ}\text{C}$	0	-	0.4	V
		Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$	0	-	0.45	
HIGH-level input voltage	V_{IH}	INH pin, measurement circuit 4	$0.7V_{DD}$	-	-	V
LOW-level input voltage	V_{IL}	INH pin, measurement circuit 4	-	-	$0.3V_{DD}$	V
Output leakage current	I_Z	Q pin, measurement circuit 5 INH pin="Low"	$Q=V_{DD}$	-	10	μA
			$Q=V_{SS}$	-10	-	
Current consumption *1	I_{DD}	5054HxA(f_{OSC}), measurement circuit 1 no load, INH pin="OPEN" $f_{OSC}=50\text{MHz}$, $f_{OUT}=50\text{MHz}$	$V_{DD}=3.3\text{V}$	-	3.5	mA
			$V_{DD}=2.5\text{V}$	-	3.0	
			$V_{DD}=1.8\text{V}$	-	2.5	
		5054HxB(f_{OSC}), measurement circuit 1 no load, INH pin="OPEN" $f_{OSC}=65\text{MHz}$, $f_{OUT}=65\text{MHz}$	$V_{DD}=3.3\text{V}$	-	4.0	
			$V_{DD}=2.5\text{V}$	-	3.0	
			$V_{DD}=1.8\text{V}$	-	2.5	
		5054HxC(f_{OSC}), measurement circuit 1 no load, INH pin="OPEN" $f_{OSC}=85\text{MHz}$, $f_{OUT}=85\text{MHz}$	$V_{DD}=3.3\text{V}$	-	4.5	
			$V_{DD}=2.5\text{V}$	-	4.0	
			$V_{DD}=1.8\text{V}$	-	3.5	
		5054HxD(f_{OSC}), measurement circuit 1 no load, INH pin="OPEN" $f_{OSC}=100\text{MHz}$, $f_{OUT}=100\text{MHz}$	$V_{DD}=3.3\text{V}$	-	5.5	
			$V_{DD}=2.5\text{V}$	-	4.5	
			$V_{DD}=1.8\text{V}$	-	4.0	
		5054HxE(f_{OSC}), measurement circuit 1 no load, INH pin="OPEN" $f_{OSC}=133\text{MHz}$, $f_{OUT}=133\text{MHz}$	$V_{DD}=3.3\text{V}$	-	7.0	
			$V_{DD}=2.5\text{V}$	-	5.5	
			$V_{DD}=1.8\text{V}$	-	4.5	
Standby current	I_{ST}	Measurement circuit 1, INH pin="Low", $T_a=-40$ to $+85^{\circ}\text{C}$	-	-	10	μA
		Measurement circuit 1, INH pin="Low"	-	-	20	
INH pin pull-up resistance	R_{PU1}	Measurement circuit 6	0.8	3	24	$\text{M}\Omega$
	R_{PU2}	Measurement circuit 6	30	70	150	$\text{k}\Omega$
Oscillator feedback resistance	R_F	5054HxA ver. Design value	1.6	3.1	4.7	$\text{k}\Omega$
		5054HxB ver. Design value	1.3	2.6	3.9	
		5054HxC ver. Design value	1.4	2.8	4.2	
		5054HxD ver. Design value	1.2	2.3	3.5	
		5054HxE ver. Design value	1.1	2.1	3.2	

5054H series, 5054xF

$V_{DD}=1.70$ to $3.63V$, $V_{SS}=0V$, $T_a=-40$ to $+125^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillator capacitance	C_G	5054HxA ver. Design value (a monitor pattern on a wafer is tested)	7.2	9.0	10.8	pF
	C_D	Excluding parasitic capacitance.	8.0	10.0	12.0	
	C_G	5054HxB ver. Design value (a monitor pattern on a wafer is tested)	5.6	7.0	8.4	
	C_D	Excluding parasitic capacitance.	7.2	9.0	10.8	
	C_G	5054HxC ver. Design value (a monitor pattern on a wafer is tested)	2.4	3.0	3.6	
	C_D	Excluding parasitic capacitance.	3.2	4.0	4.8	
	C_G	5054HxD ver. Design value (a monitor pattern on a wafer is tested)	0.8	1.0	1.2	
	C_D	Excluding parasitic capacitance.	1.6	2.0	2.4	
	C_G	5054HxE ver. Design value (a monitor pattern on a wafer is tested)	0.0	0.0	0.0	
	C_D	Excluding parasitic capacitance.	0.8	1.0	1.2	

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA] + C_{LOUT}[pF] \times V_{DD}[V] \times f_{OUT}[MHz] \times 10^{-3}$$

DC Characteristics (xF version)

$V_{DD}=2.25$ to 3.63 V, $V_{SS}=0$ V, $T_a=-40$ to $+105^{\circ}\text{C}$ unless otherwise noted.

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HIGH-level output voltage	V_{OH}	Q pin, measurement circuit 3, $I_{OH}=8\text{mA}$, $T_a=-40$ to $+85^{\circ}\text{C}$	$V_{DD}-0.4$	-	V_{DD}	V
		Q pin, measurement circuit 3, $I_{OH}=8\text{mA}$	$V_{DD}-0.45$	-	V_{DD}	
LOW-level output voltage	V_{OL}	Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$, $T_a=-40$ to $+85^{\circ}\text{C}$	0	-	0.4	V
		Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$	0	-	0.45	
HIGH-level input voltage	V_{IH}	INH pin, measurement circuit 4	$0.7V_{DD}$	-	-	V
LOW-level input voltage	V_{IL}	INH pin, measurement circuit 4	-	-	$0.3V_{DD}$	V
Output leakage current	I_Z	Q pin, measurement circuit 5 INH=“Low”, $T_a=-40$ to $+85^{\circ}\text{C}$	$Q=V_{DD}$	-	-	μA
			$Q=V_{SS}$	-10	-	
		Q pin, measurement circuit 5 INH=“Low”	$Q=V_{DD}$	-	-	
			$Q=V_{SS}$	-100	-	
Current consumption ^{*1}	I_{DD}	5054xF(f_{OSC}), measurement circuit 1, no load, INH=“OPEN”, $f_{OSC}=170\text{MHz}$, $f_{OUT}=170\text{MHz}$	$V_{DD}=3.3\text{V}$	-	15.0	mA
			$V_{DD}=2.5\text{V}$	-	13.0	
Standby current	I_{ST}	Measurement circuit 1, INH=“Low” $T_a=-40$ to $+85^{\circ}\text{C}$	-	-	10	μA
		Measurement circuit 1, INH=“Low”	-	-	100	
INH pull-up resistance	R_{PU1}	Measurement circuit 6	0.8	3	24	$\text{M}\Omega$
	R_{PU2}	Measurement circuit 6	30	70	150	$\text{k}\Omega$
Oscillator feedback resistance	R_F	Design value	2.1	4.0	6.0	$\text{k}\Omega$
Oscillator capacitance	C_G	Design value (a monitor pattern on a wafer is tested)	0.0	0.0	0.0	pF
	C_D	Excluding parasitic capacitance	0.8	1.0	1.2	

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[\text{mA}] = I_{DD}[\text{mA}] + C_{LOUT}[\text{pF}] \times V_{DD}[\text{V}] \times f_{OUT}[\text{MHz}] \times 10^{-3}$$

AC Characteristics

$V_{DD}=1.70$ to $3.63V$, $V_{SS}=0V$, $T_a=-40$ to $+125^{\circ}C$ unless otherwise noted.

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Output rise time	t_{r1}	Measurement circuit 1 $C_{LOUT}=15pF$ $0.1V_{DD}$ to $0.9V_{DD}$ $V_{DD}=2.25$ to $3.63V$	HxA, HxB, HxC, HxD, HxE ver.	-	1.0	2.0	ns
			$T_a=-40$ to $+105^{\circ}C$, xF ver.	-	1.0	2.0	
	t_{r2}	Measurement circuit 1 $C_{LOUT}=15pF$ $0.1V_{DD}$ to $0.9V_{DD}$ $V_{DD}=1.70$ to $2.25V$	$T_a=-40$ to $+85^{\circ}C$ HxA, HxB, HxC, HxD, HxE ver.	-	1.5	2.5	
			HxA, HxB, HxC, HxD, HxE ver.	-	1.5	3.0	
Output fall time	t_{f1}	Measurement circuit 1 $C_{LOUT}=15pF$ $0.9V_{DD}$ to $0.1V_{DD}$ $V_{DD}=2.25$ to $3.63V$	HxA, HxB, HxC, HxD, HxE ver.	-	1.0	2.0	ns
			$T_a=-40$ to $+105^{\circ}C$, xF ver.	-	1.0	2.0	
	t_{f2}	Measurement circuit 1 $C_{LOUT}=15pF$ $0.9V_{DD}$ to $0.1V_{DD}$ $V_{DD}=1.70$ to $2.25V$	$T_a=-40$ to $+85^{\circ}C$ HxA, HxB, HxC, HxD, HxE ver.	-	1.5	2.5	
			HxA, HxB, HxC, HxD, HxE ver.	-	1.5	3.0	
Output duty cycle	DUTY	Measurement circuit 1 $C_{LOUT}=15pF$ $T_a=25^{\circ}C$	$V_{DD}=1.70$ to $3.63V$ HxA, HxB, HxC, HxD, HxE ver.	45	50	55	%
			$V_{DD}=2.25$ to $3.63V$, xF ver.	45	50	55	
Output disable delay time	t_{OD}	Measurement circuit 2, $T_a=25^{\circ}C$, $C_{LOUT}\leq 15pF$		-	-	200	ns

Timing chart

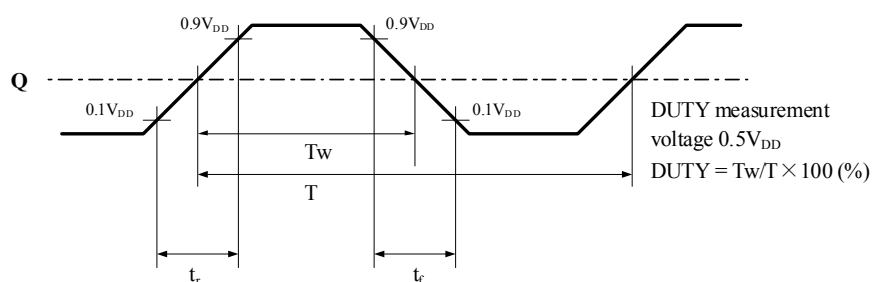
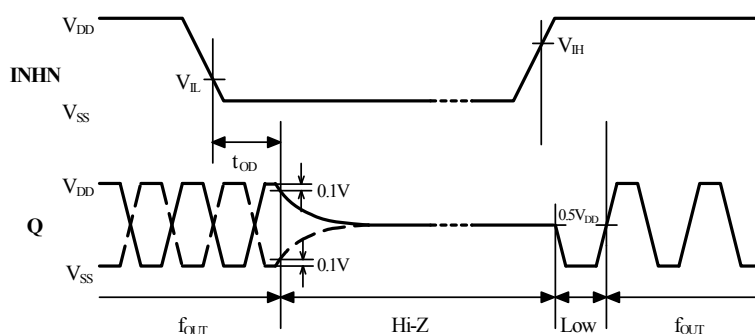


Figure 1. Output switching waveform

Figure 2. Output disable delay (t_{OD}) timing chart

FUNCTIONAL DESCRIPTION

INHN Function

When INHN goes Low level, the Q output becomes high impedance.

INHN	Q	Oscillator
High(Open)	f_{OUT}	Operating
Low	Hi-Z	Stopped

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (High or Low).

When INHN is tied to Low level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance.

When INHN is left open circuit or tied to High level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes High level. Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5054 series incorporate an oscillation detection circuit. The oscillation detection circuit disables the output until the oscillator circuit starts up. This function avoids the problem where the oscillator does not start, due to abnormal oscillation conditions, where power is applied or when the oscillator is restarted using INHN.

C_0 cancellation circuit

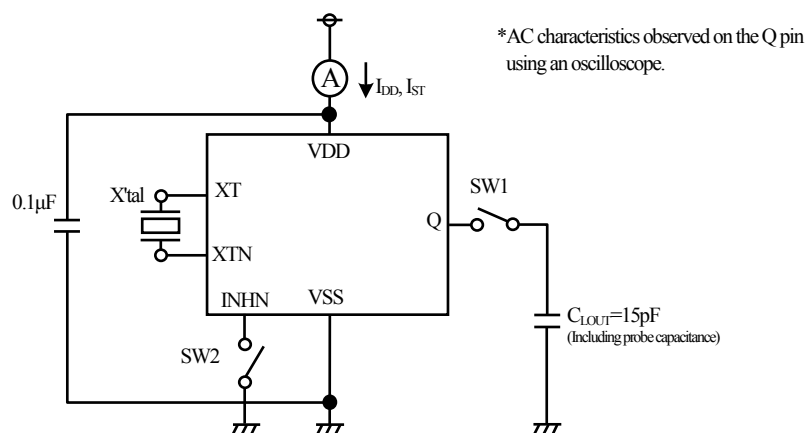
Oscillation circuit with a built-in C_0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C_0 . It reduces the C_0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C_0 .

This cancellation circuit makes it easier to maintain the oscillation margin.

MEASUREMENT CIRCUITS

Measurement circuit 1

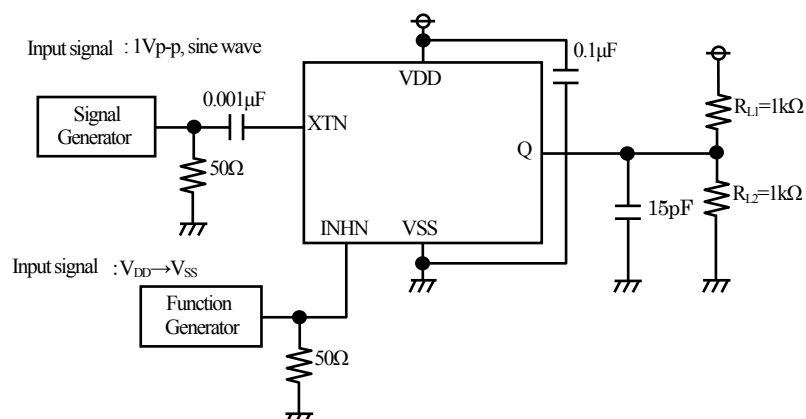
Measurement Parameter: I_{DD} , I_{ST} , DUTY, t_r , t_f



Parameter	SW1	SW2
I_{DD}	OFF	OFF
I_{ST}	ON or OFF	ON
DUTY, t_r , t_f	ON	OFF

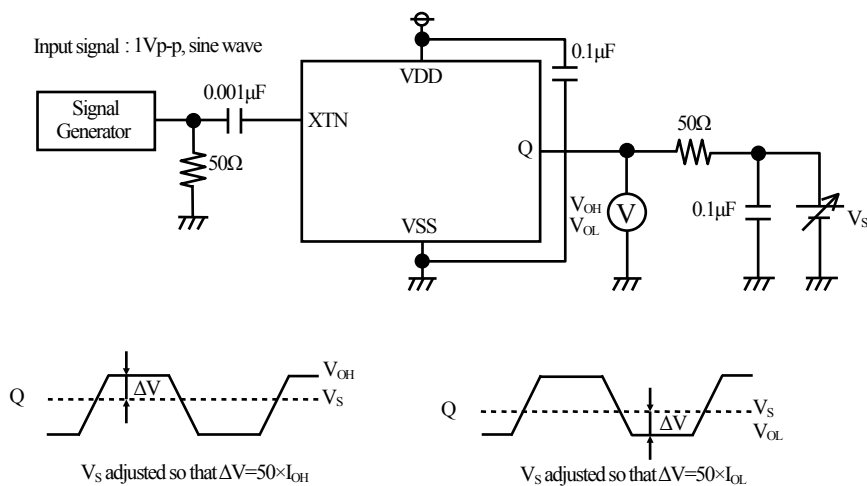
Measurement circuit 2

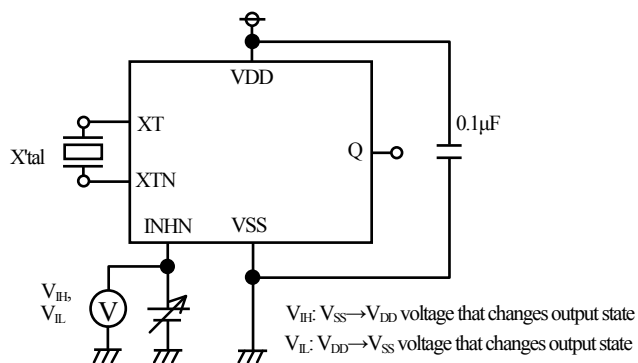
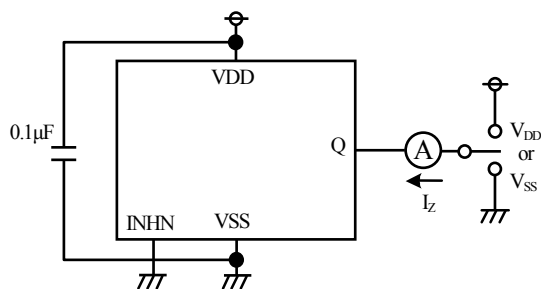
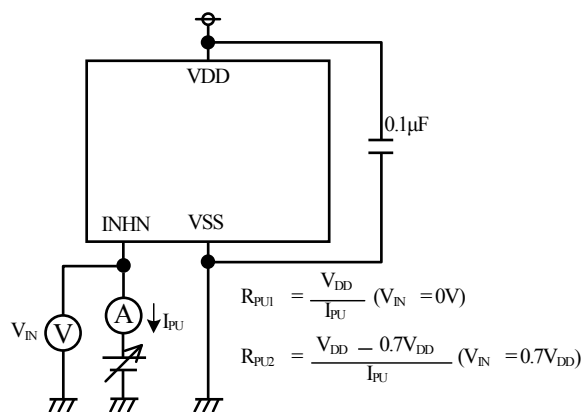
Measurement Parameter: t_{OD}



Measurement circuit 3

Measurement Parameter: V_{OH} , V_{OL}



Measurement circuit 4Measurement Parameter: V_{IH} , V_{IL} **Measurement circuit 5**Measurement Parameter: I_Z **Measurement circuit 6**Measurement Parameter: R_{PU1} , R_{PU2} 

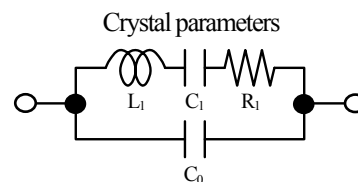
DATA REFERENCE CHARACTERISTICS EXAMPLE (5054 Typical Characteristics)

The characters given below were measured using a Seiko NPC standards jig and standard crystal element, and do not represent a guarantee of device characteristics.

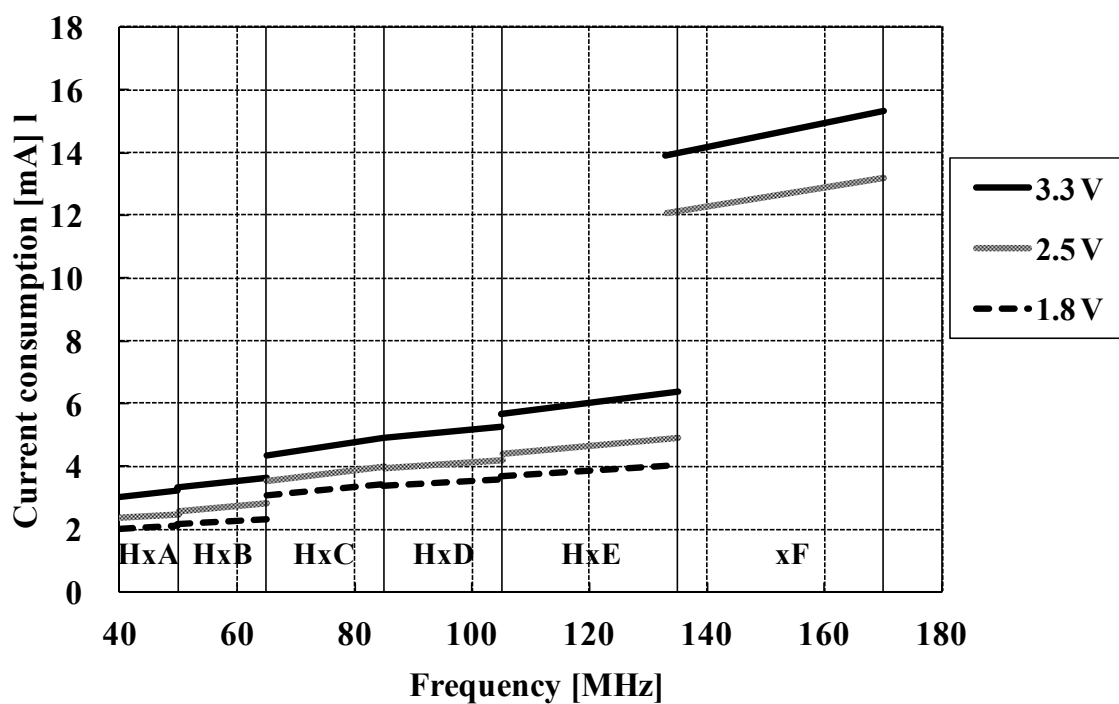
Note that the characteristics will vary due to measurement environment and the oscillator element used.

Crystal used for measurement

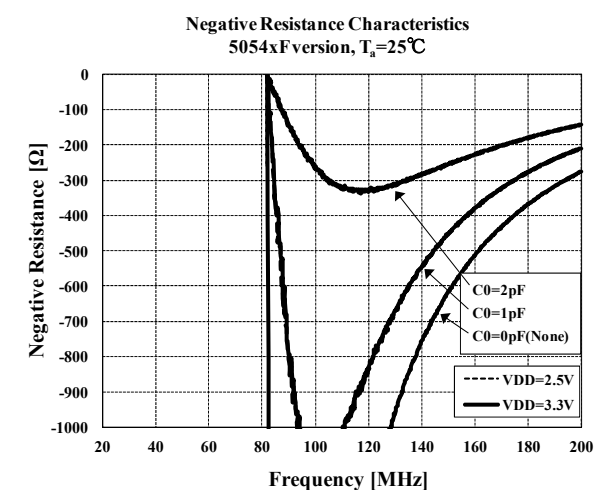
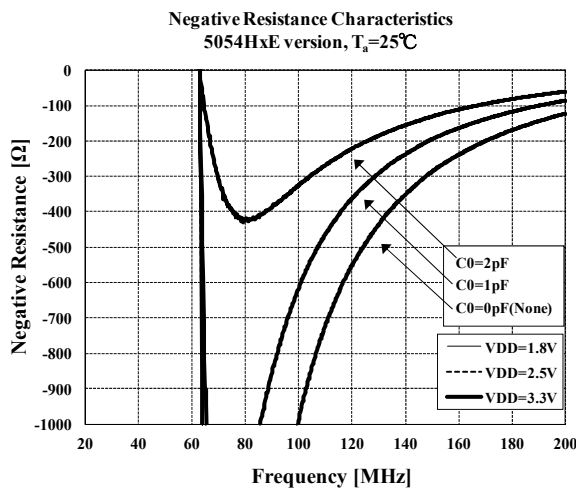
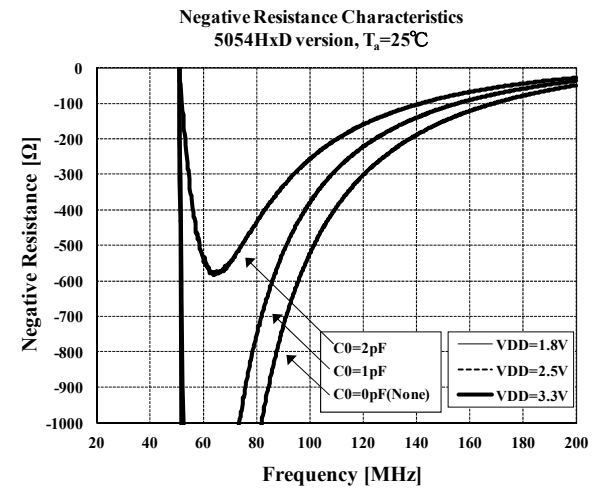
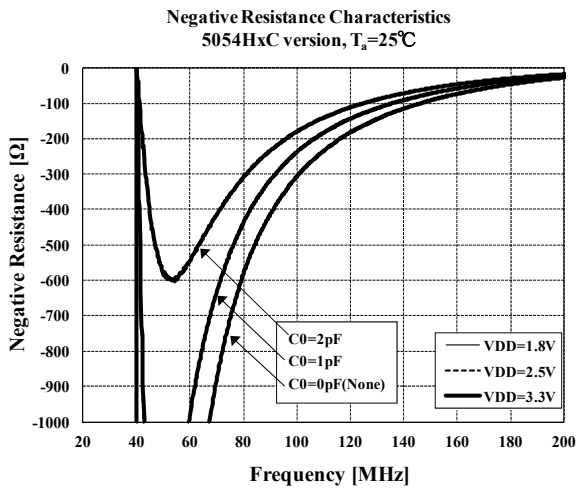
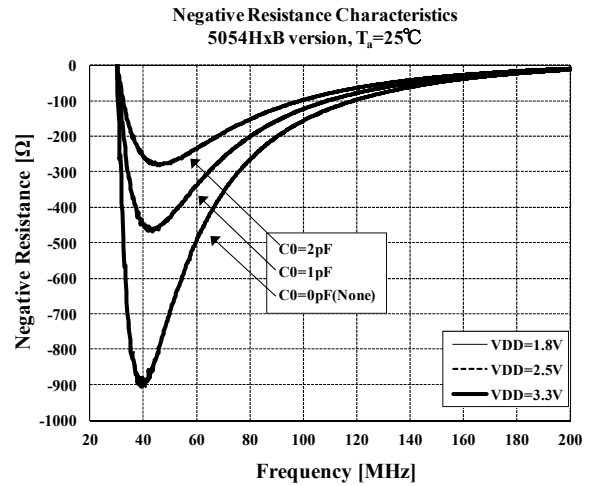
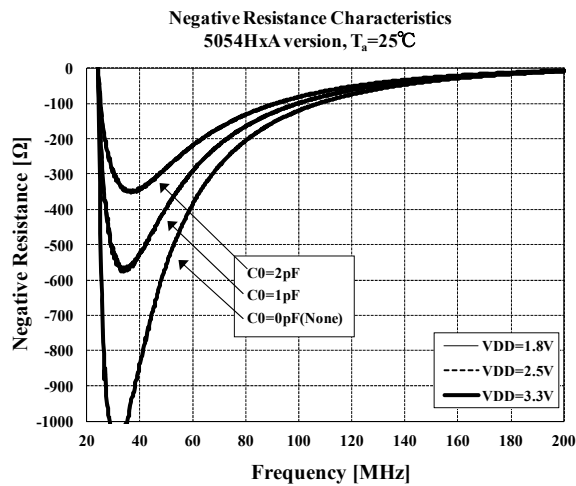
Parameter	50MHz	65MHz	80MHz	100MHz	125MHz	170MHz
C_0 (pF)	1.3	1.7	1.6	1.7	2.0	2.8
R_1 (Ω)	59	40	59	44	33	45

**Current Consumption****Current Consumption Characteristics**

$T_a=25^\circ\text{C}$, No load



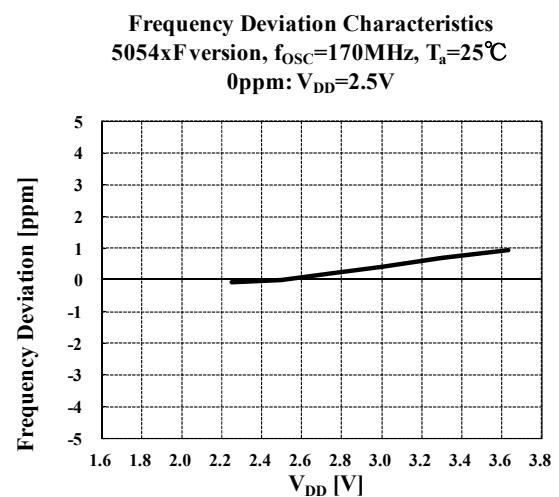
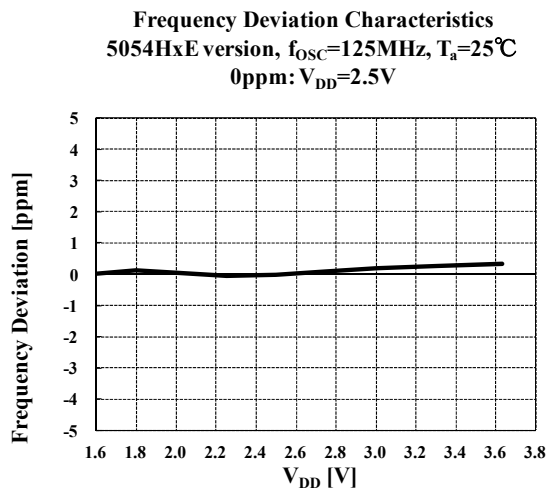
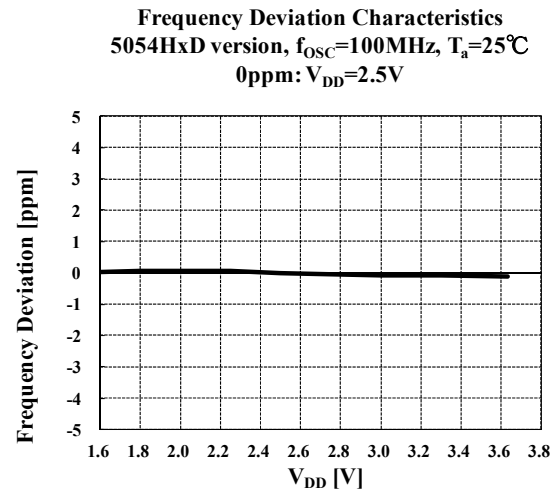
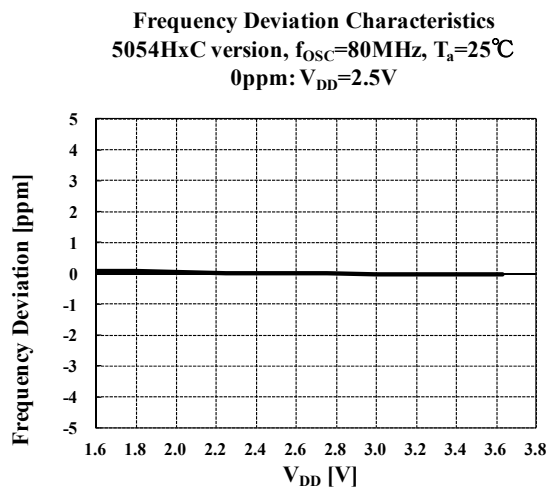
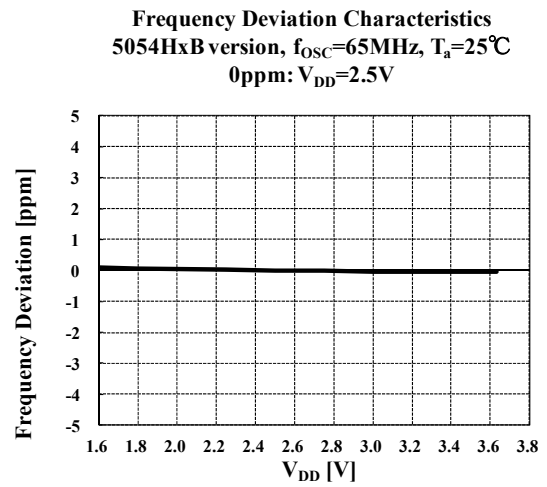
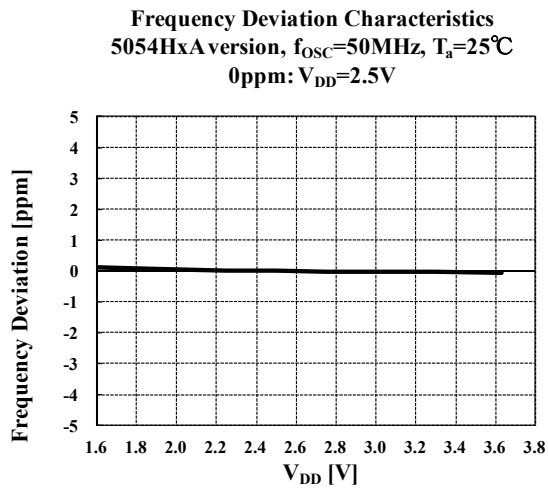
Negative Resistance



Measurement equipment: Agilent 4396B Impedance Analyzer

The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XT and XTN pins. They were performed with Agilent 4396B using the Seiko NPC test jig. They may vary in a measurement jig, and measurement environment.

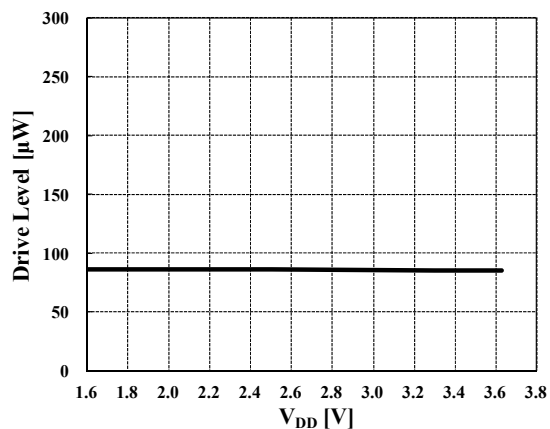
Frequency Deviation by Voltage



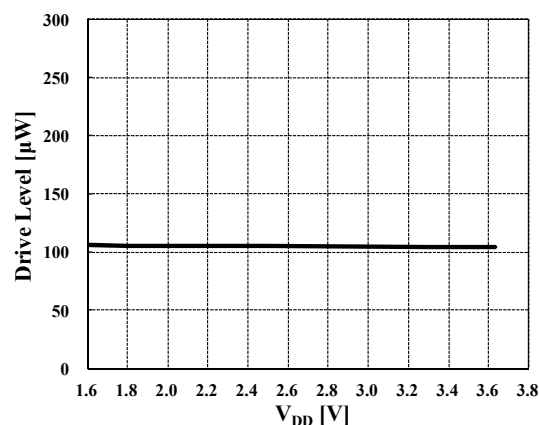
Measurement equipment: Agilent 53132A Frequency Counter

Drive Level

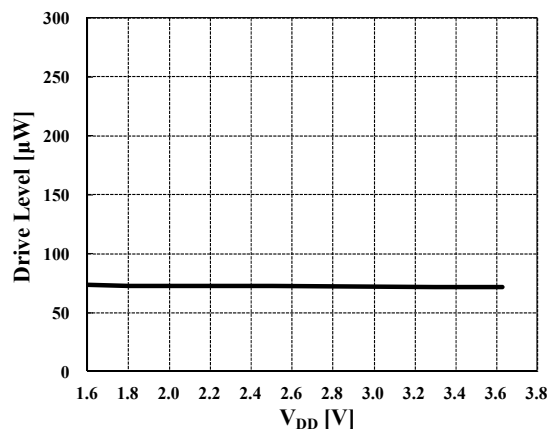
Drive Level Characteristics
5054HxA version, $f_{OSC}=50\text{MHz}$, $T_a=25^\circ\text{C}$



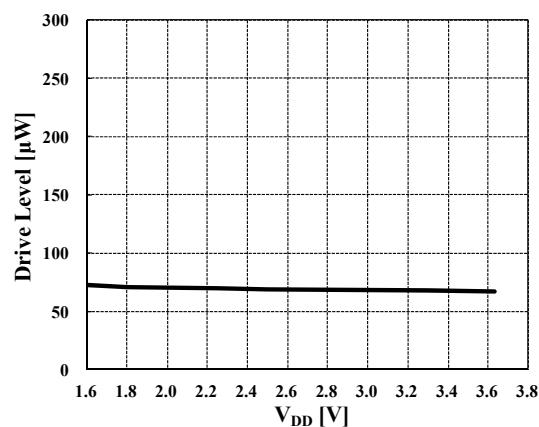
Drive Level Characteristics
5054HxB version, $f_{OSC}=65\text{MHz}$, $T_a=25^\circ\text{C}$



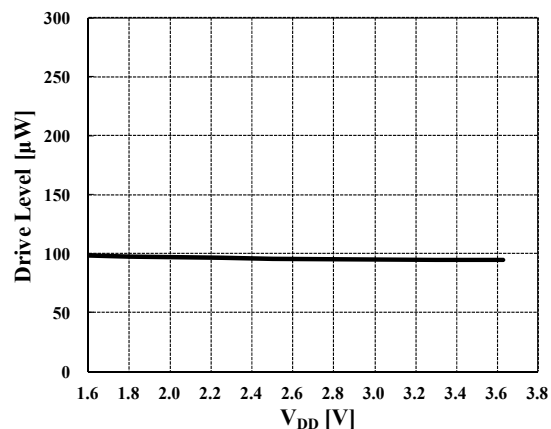
Drive Level Characteristics
5054HxC version, $f_{OSC}=85\text{MHz}$, $T_a=25^\circ\text{C}$



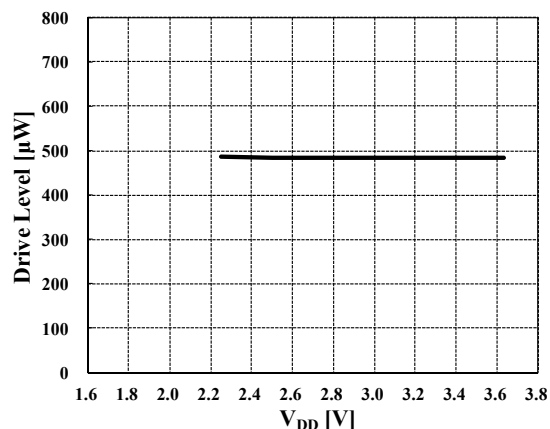
Drive Level Characteristics
5054HxD version, $f_{OSC}=100\text{MHz}$, $T_a=25^\circ\text{C}$



Drive Level Characteristics
5054HxE version, $f_{OSC}=125\text{MHz}$, $T_a=25^\circ\text{C}$



Drive Level Characteristics
5054xF version, $f_{OSC}=170\text{MHz}$, $T_a=25^\circ\text{C}$

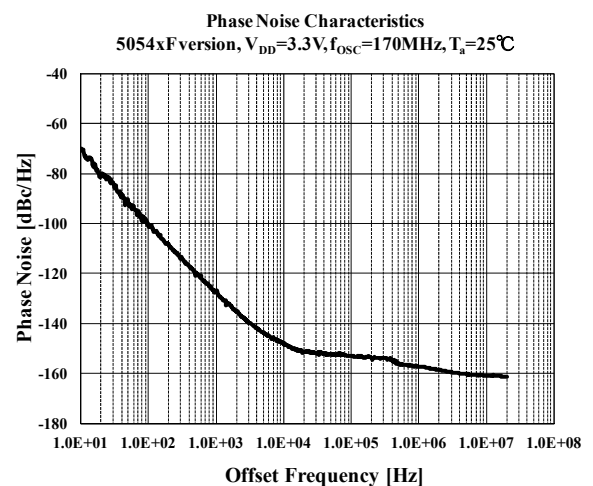
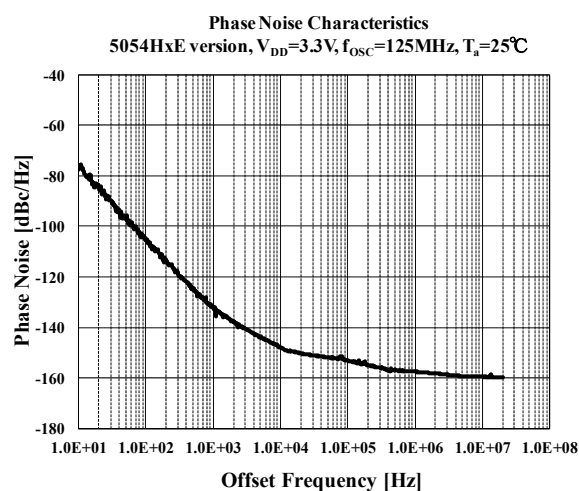
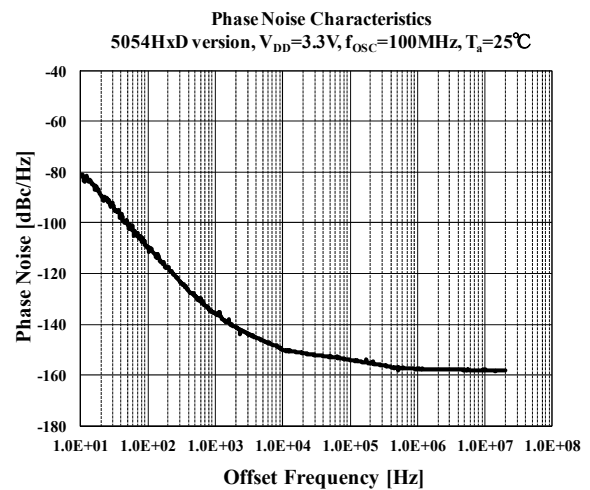
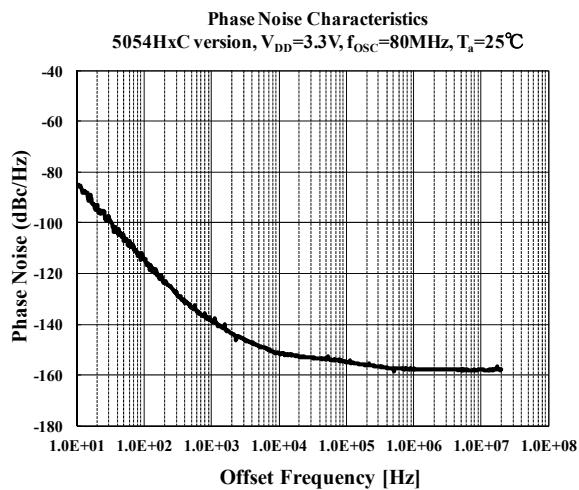
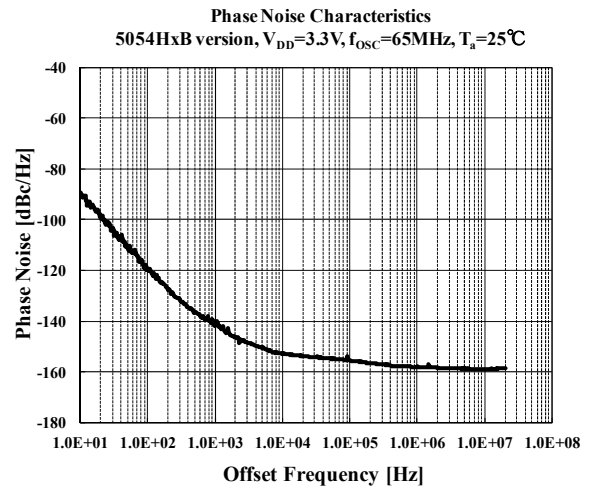
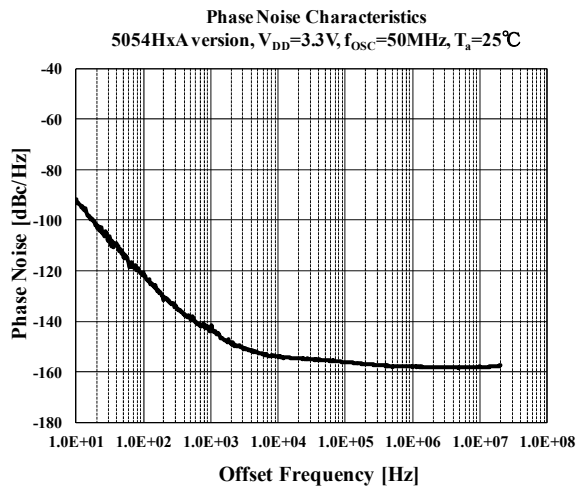


Measurement equipment: Agilent DSO80604B Digital Oscilloscope

Tektronix CT-6 Current probe

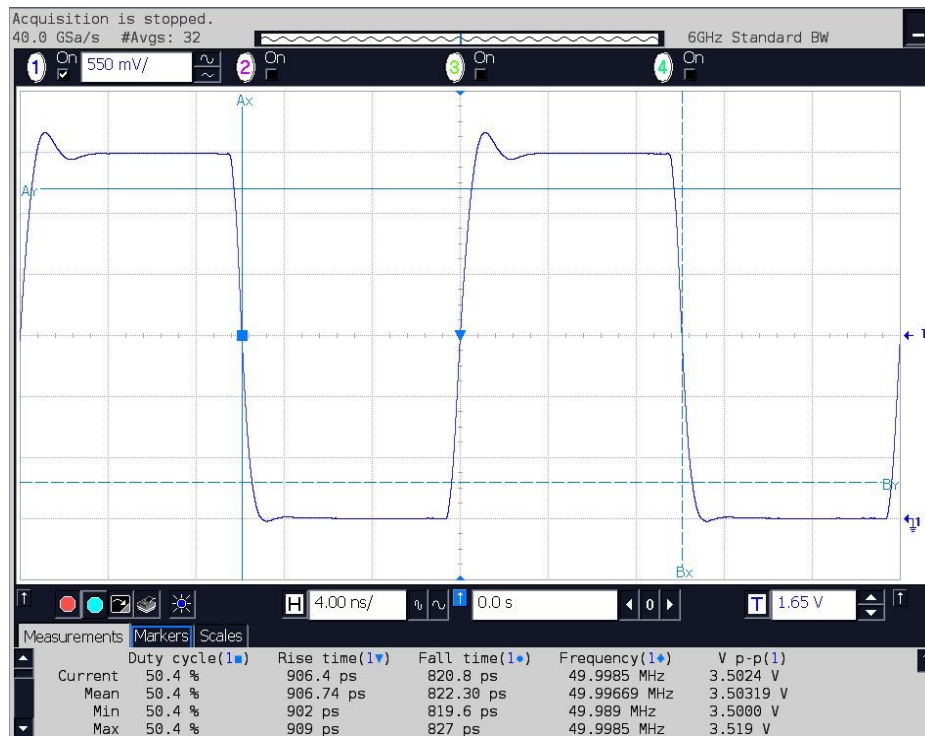
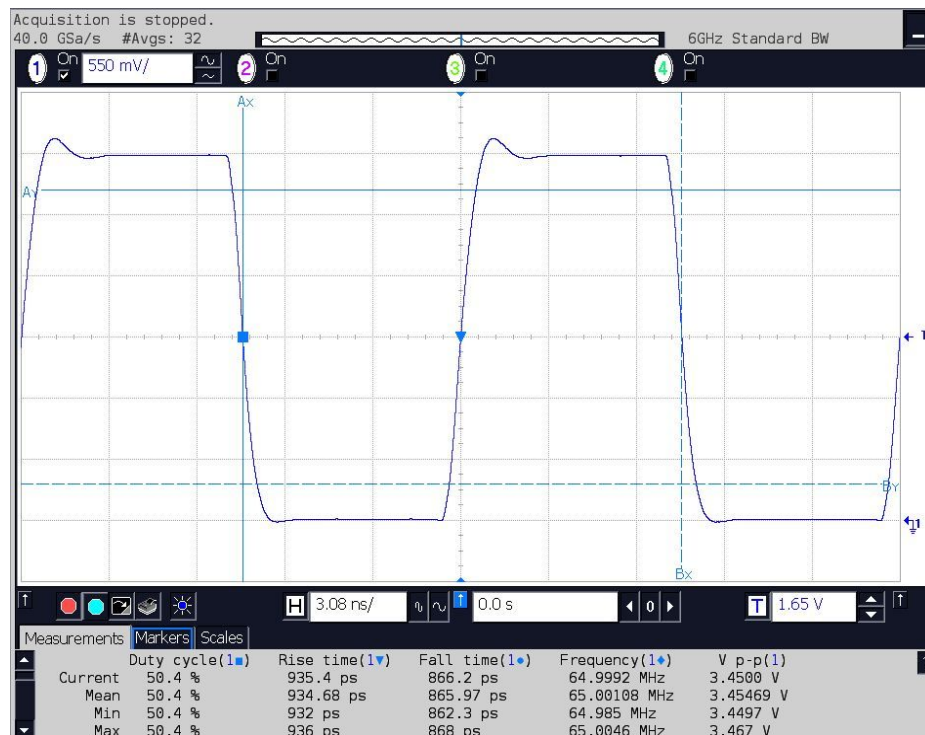
Agilent 53132A Frequency Counter

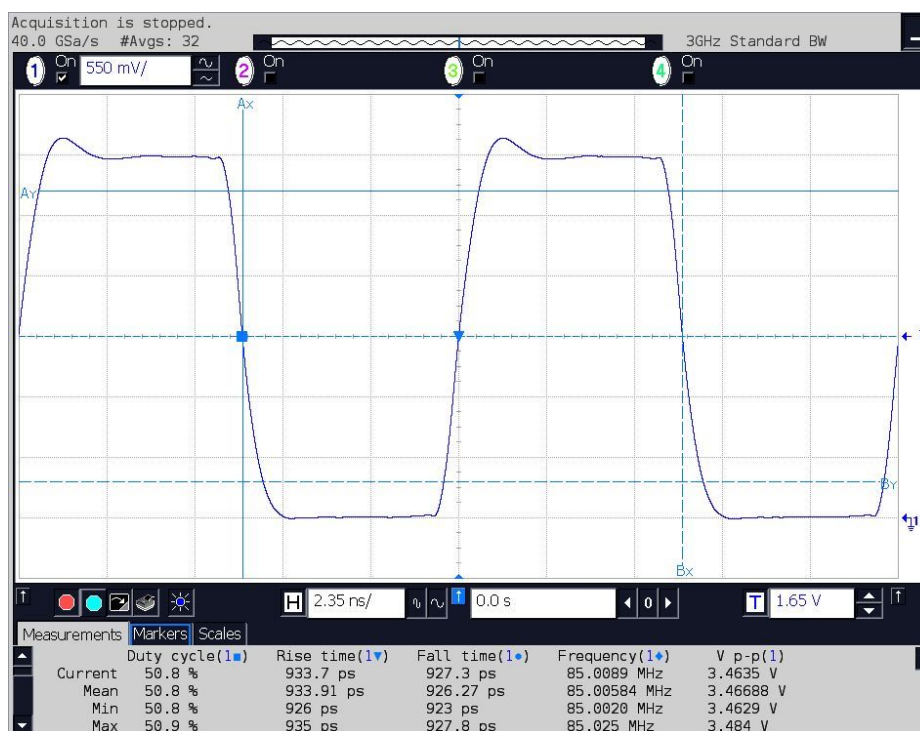
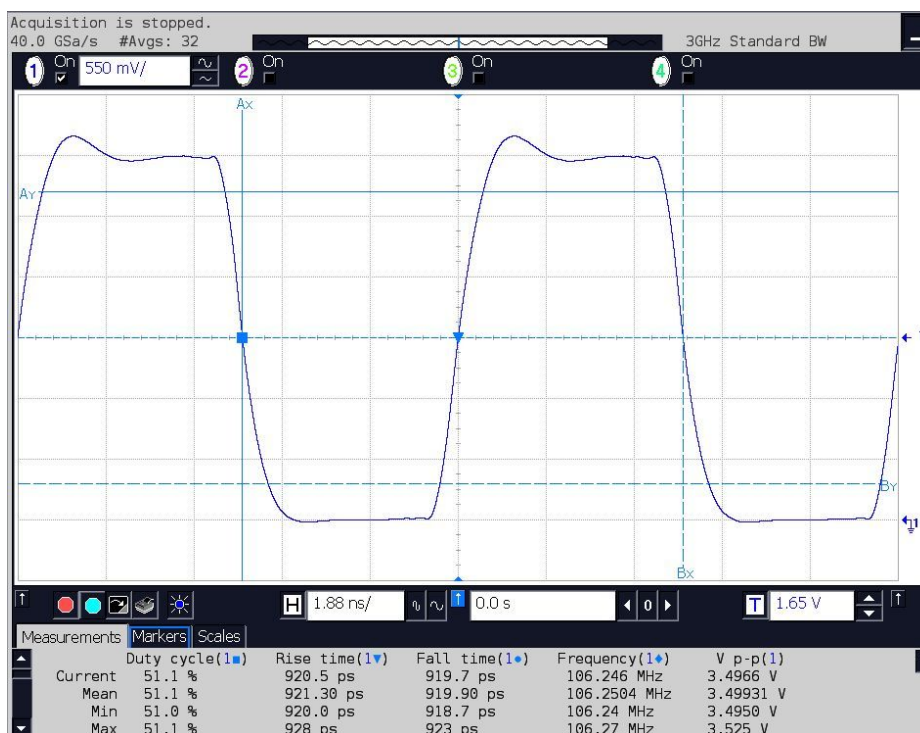
Phase Noise

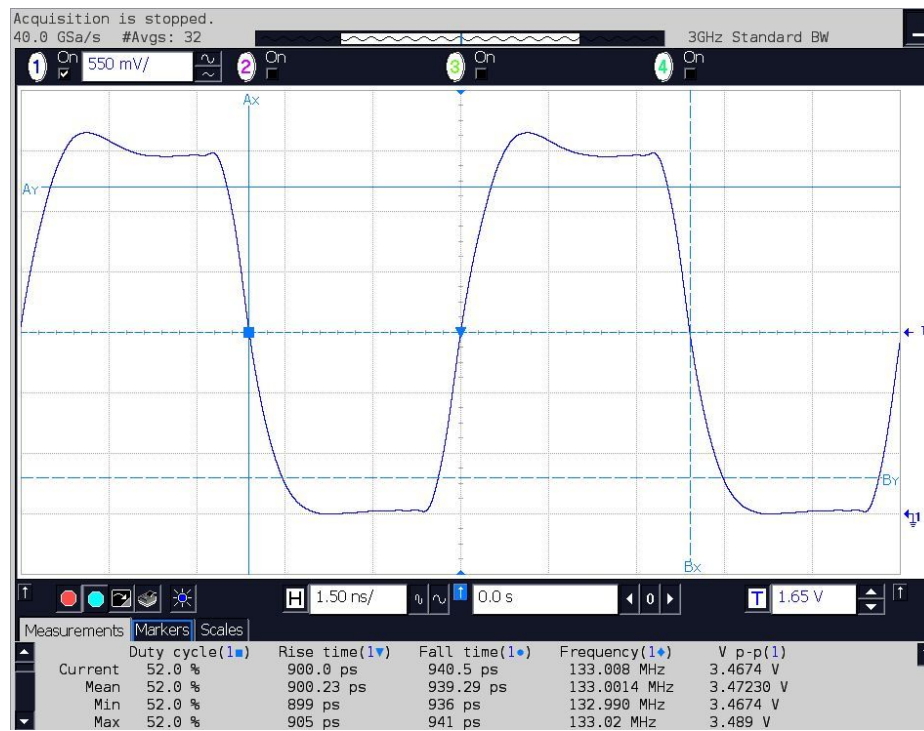


Measurement equipment: Signal Source Analyzer Agilent E5052B

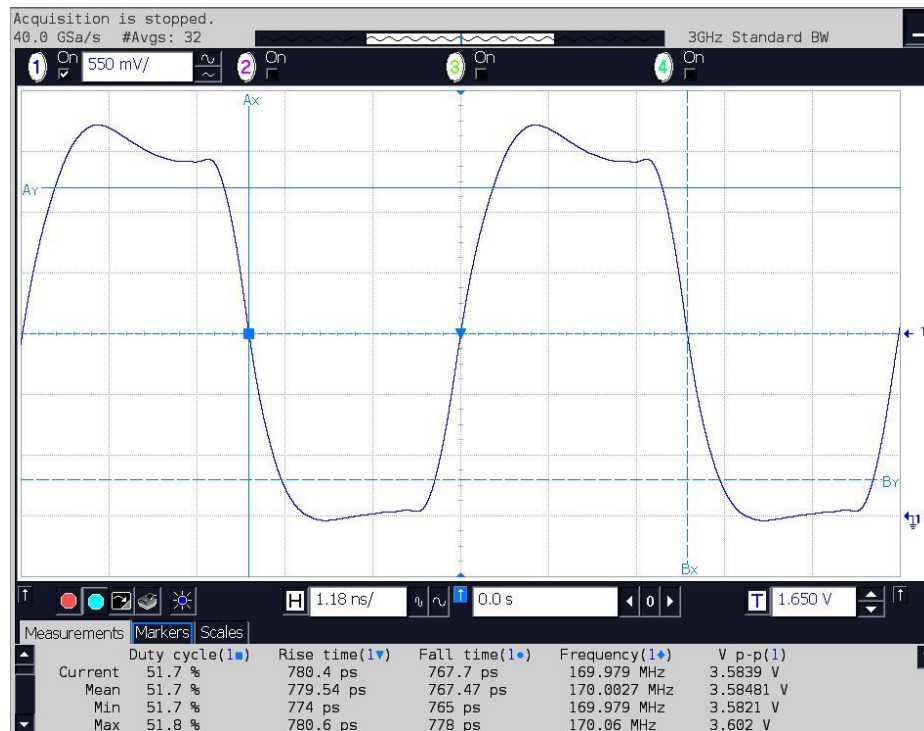
Output Waveform

5054HxA version, $V_{DD}=3.3V$, $f_{OUT}=50MHz$, $C_{LOUT}=15pF$, $T_a=25^{\circ}C$ 5054HxB version, $V_{DD}=3.3V$, $f_{OUT}=65MHz$, $C_{LOUT}=15pF$, $T_a=25^{\circ}C$

5054HxC version, $V_{DD}=3.3V$, $f_{OUT}=85MHz$, $C_{LOUT}=15pF$, $T_a=25^{\circ}C$ 5054HxD version, $V_{DD}=3.3V$, $f_{OUT}=106.25MHz$, $C_{LOUT}=15pF$, $T_a=25^{\circ}C$



5054HxE version, $V_{DD}=3.3V$, $f_{OUT}=133MHz$, $C_{LOUT}=15pF$, $T_a=25^{\circ}C$



5054xF version, $V_{DD}=3.3V$, $f_{OUT}=170MHz$, $C_{LOUT}=15pF$, $T_a=25^{\circ}C$

Measurement equipment: Agilent DSO80604B Oscilloscope
Agilent 1134A Differential Probe
Agilent E2678A Probe Head

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