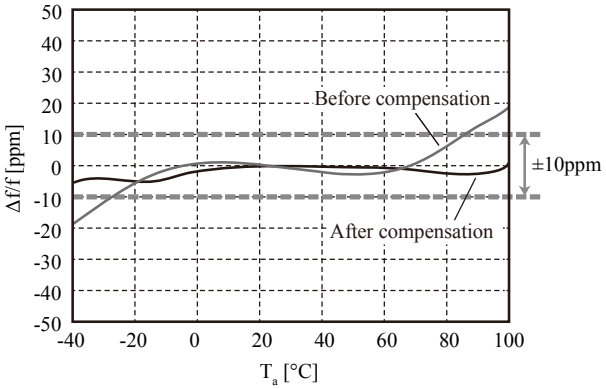
OVERVIEW

The 5043 series are high-stability clock oscillator ICs with built-in frequency adjustment functions. The frequency adjustment functions can be optimized, by the addition of a minimal adjustment process, to improve the frequency stability. The function is implemented using frequency adjustment data written to a built-in EEPROM over a 1-wire serial interface. The ICs are ideal for compact crystal oscillators for use in applications such as Wireless-LAN that require high frequency stability in the order of ±30 to ±10ppm. They use a pad layout suitable for flip chip bonding mounting.

FEATURES

- Realizing frequency stability improvement with minimal additional process
- Temperature compensation range / Operating temperature range: -40°C to +85°C
- Frequency adjustment functions built-in
  <Frequency-temperature characteristics compensation function>
  AT-cut crystal, 3rd order frequency-temperature characteristics compensation, with independent low-temperature and high-temperature compensation settings
  - Center frequency adjustment function
  - Temperature rotation compensation function
  - Low-temperature characteristics compensation
  - High-temperature characteristics compensation
- Rewritable EEPROM built-in
- 6 pads: same as general clock oscillator ICs
- Operating supply voltage range: 2.25V to 3.63V
- Recommended oscillation frequency range (for fundamental oscillation): 20MHz to 55MHz
- Frequency divider built-in
  Selectable by version: f_0, $f_0/2$
- Standby function
  High-impedance in standby mode, oscillator stops
- CMOS output
- 15pF output load capacitance
- Pad layout for flip chip bonding
- Wafer form (WF5043AxB)

FREQUENCY CHARACTERISTICS COMPENSATION BEFORE and AFTER ADJUSTMENT



APPLICATIONS

- 3.2mm×2.5mm, 2.5mm×2.0mm, 2.0mm×1.6mm size miniature crystal oscillator modules
- Wireless-LAN and applications requiring high-stability clock oscillators

SERIES CONFIGURATION

Version name	Operating supply voltage range [V]	Recommended oscillation frequency range*1 [MHz]	Output frequency
5043A1B	2.25 to 3.63	20 to 55	f_0
5043A2B			$f_0/2$

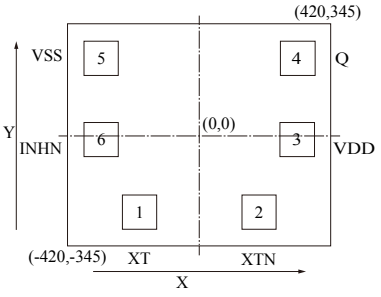
*1. The recommended oscillation frequency range is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the recommended oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

ORDERING INFORMATION

Device	Package	Version name
WF5043AxB-4	Wafer form	WF5043A□B-4 Form WF : Wafer form Frequency divider function 1: f_0 2: $f_0/2$ Operating supply voltage A:2.25 to 3.63V

PAD LAYOUT

(Unit: µm)



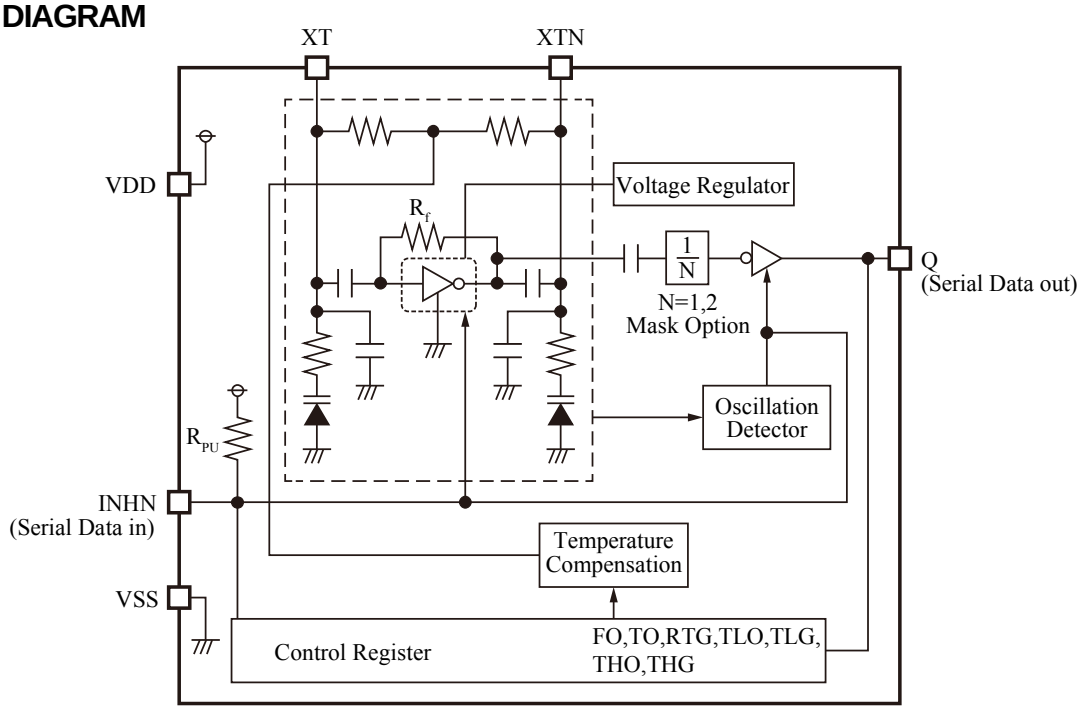
Chip size: 0.84mm × 0.69mm
Wafer size: 6inch
Wafer thickness: 130µm ± 15µm
PAD size: 80µm × 80µm
Chip base: V_{SS} level

PIN DESCRIPTION and PAD COORDINATE

No.	PIN	I/O*1	Description	PAD coordinate [µm]	
				X	Y
1	XT	I	Crystal connection pins	-225.2	-253.5
2	XTN	O	Crystal is connected between XT and XTN.	225.2	-253.5
3	VDD	-	(+) supply voltage	328.5	-5.0
4	Q	O	Output pin (Output one of f_0, $f_0/2$)	328.5	223.8
5	VSS	-	(-) ground	-328.5	223.8
6	INHN	I	Input pin controlled output state (oscillator stops and output pin becomes Hi-Z when LOW), power-saving pull-up resistor built-in	-328.5	-5.0

*1. I: Input pin O: Output pin

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range*1	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Program read/write input voltage range*1	V_{PP}	Between INHN and VSS	-0.3 to +16.5	V
Input voltage range*1*2	V_{IN}	Input pins	-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	Output pins	-0.3 to V_{DD}+0.3	V
Output current*1	I_{OUT}	Q pin	±20	mA
Storage temperature range*3	T_{STG}	Wafer form	-65 to +150	°C
EEPROM maximum writes	N_{EW}		100	times

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Supply voltage	V_{DD}	Between VDD and VSS*2	2.25		3.63	V
Input voltage	V_{IN}	Input pins（XT, INHN）	V_{SS}		V_{DD}	V
Operating temperature	T_a		-40		+85	°C
Oscillation frequency*1	f_0		20		55	MHz
Output frequency	f_{OUT}	Q pin	10		55	MHz
Output load capacitance	C_{LOUT}	Q pin			15	pF

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5043 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
DC Characteristics

V_{DD}=2.25 to 3.63V, V_{SS}=0V, T_a= -40 to +85°C, C_{LOUT}=15pF unless otherwise noted.

Parameter	Symbol	Condition		Rating MIN	Rating TYP	Rating MAX	Unit
Operating current consumption*1	I_{DD}	5043A1B ($f_{OUT}=f_0$) measurement circuit 1, no load INHN="HIGH", f_0=48MHz	V_{DD}=2.5V		1.4	2.8	mA
			V_{DD}=3.3V		1.7	3.4	
		5043A2B ($f_{OUT}=f_0/2$) measurement circuit 1, no load INHN="HIGH", f_0=48MHz	V_{DD}=2.5V		1.1	2.2	mA
			V_{DD}=3.3V		1.4	2.7	
Standby current	I_{ST}	measurement circuit 1, INHN="LOW"				10	µA
HIGH-level output voltage	V_{OH}	measurement circuit 3, Q pin, I_{OH}=-4mA		V_{DD}-0.4			V
LOW-level output voltage	V_{OL}	measurement circuit 3, Q pin, I_{OL}=4mA				0.4	V
Output leakage current	I_Z	measurement circuit 4 INHN="LOW"	Q=V_{DD}			10	µA
			Q=V_{SS}	-10			
HIGH-level input voltage	V_{IH}	measurement circuit 5, INHN pin		0.7V_{DD}			V
LOW-level input voltage	V_{IL}	measurement circuit 5, INHN pin				0.3V_{DD}	V
INHN pull-up resistance	R_{PU1}	measurement circuit 6	INHN=V_{SS}	0.4	1.5	10	MΩ
	R_{PU2}		INHN=0.7V_{DD}	50	100	200	kΩ

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no load consumption current and f_{OUT} is the output frequency.

$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA]+C_{LOUT}[pF]\times V_{DD}[V]\times f_{OUT}[MHz]\times 10^{-3}$

AC Characteristics

Clock Output Characteristics (Q pin)

V_{DD}=2.25 to 3.63V, V_{SS}=0V, T_a= -40 to +85°C, C_{LOUT}=15pF unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Output duty cycle*1	DUTY	measurement circuit 1, threshold voltage 0.5V_{DD} DUTY = T_W/T×100	45	50	55	%
Rise time	t_r	measurement circuit 1, 0.1V_{DD}→0.9V_{DD}			4.5	ns
Fall time	t_f	measurement circuit 1, 0.9V_{DD}→0.1V_{DD}			4.5	ns
Output disable delay time	t_{OD}	measurement circuit 2*2, INHN= "HIGH"→"LOW"			100	ns

*1. This parameter is measured using the NPC's standard crystal. Note that the values will vary with the crystal characteristics used or mounting conditions.
*2. Measurement circuit 2 takes an external input on the XT pin, without using a crystal.

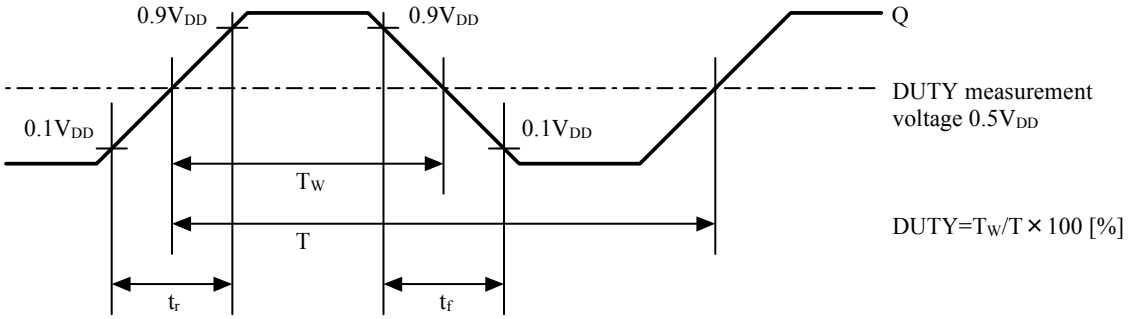


Figure 1. Output switching waveform

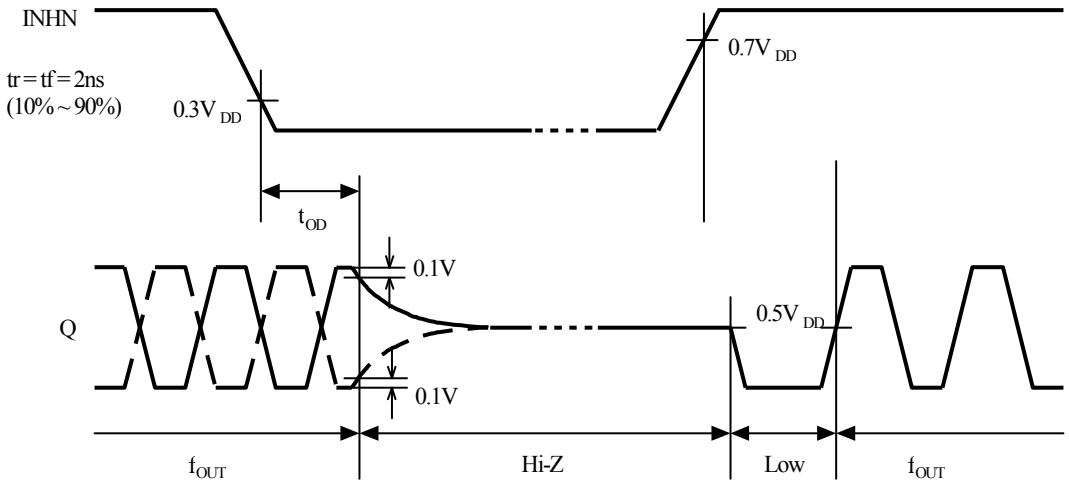
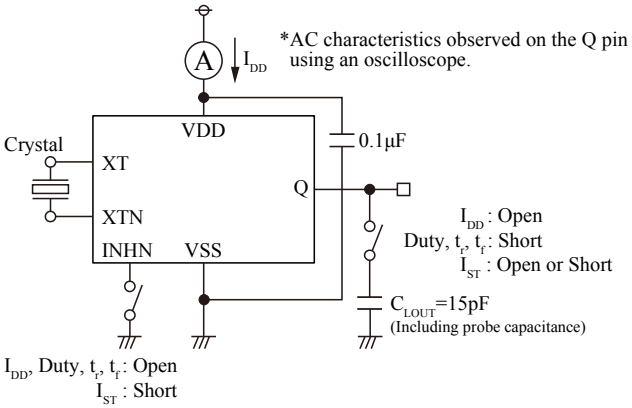


Figure 2. Output disable timing chart

MEASUREMENT CIRCUITS

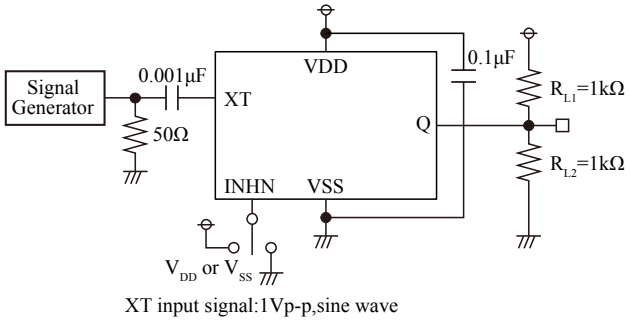
MEASUREMENT CIRCUIT 1

Measurement Parameter: I_{DD}, I_{ST}, DUTY, t_r, t_f



MEASUREMENT CIRCUIT 2

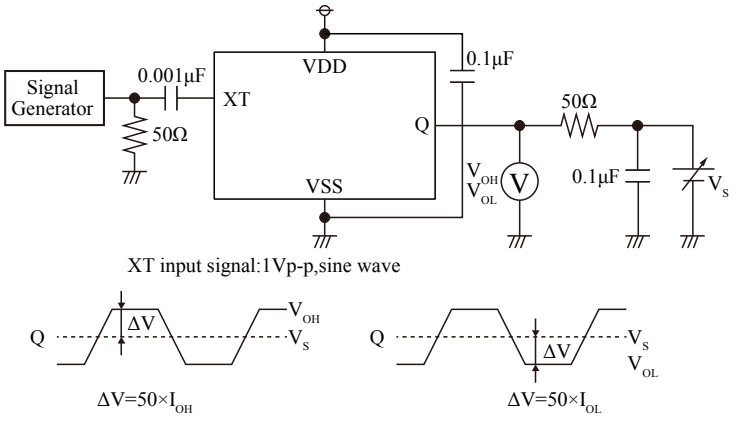
Measurement Parameter: t_{OD}



XT input signal:1Vp-p,sine wave

MEASUREMENT CIRCUIT 3

Measurement Parameter: V_{OH}, V_{OL}

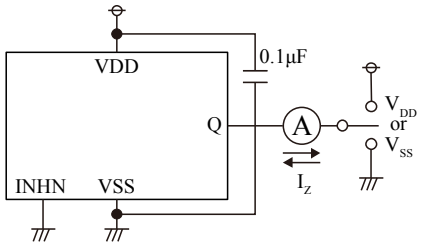


XT input signal:1Vp-p,sine wave

$\Delta V=50\times I_{OH}$ $\Delta V=50\times I_{OL}$

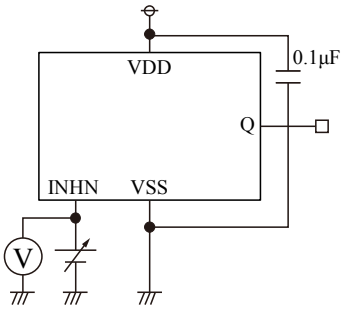
MEASUREMENT CIRCUIT 4

Measurement Parameter: I_Z



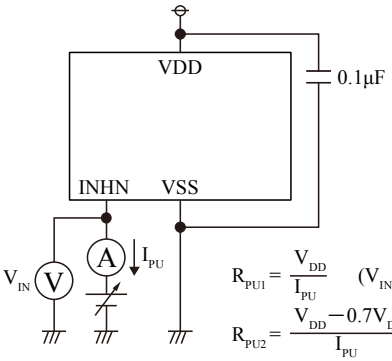
MEASUREMENT CIRCUIT 5

Measurement Parameter: V_{IH}, V_{IL}



MEASUREMENT CIRCUIT 6

Measurement Parameter: R_{PU1}, R_{PU2}



$R_{PU1}=\frac{V_{DD}}{I_{PU}}$ $(V_{IN}=0V)$

$R_{PU2}=\frac{V_{DD}-0.7V_{DD}}{I_{PU}}$ $(V_{IN}=0.7V_{DD})$

FUNCTIONAL DESCRIPTION

Frequency Adjustment Function

The 5043 series ICs have a built-in oscillator frequency adjustment function. The frequency adjustment settings are written to and stored in internal EEPROM, making the devices easy to setup. A typical compensation sequence is shown below.

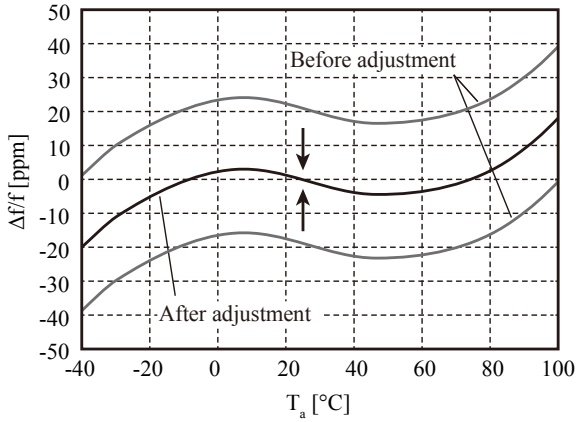


Figure 3. Center frequency adjustment

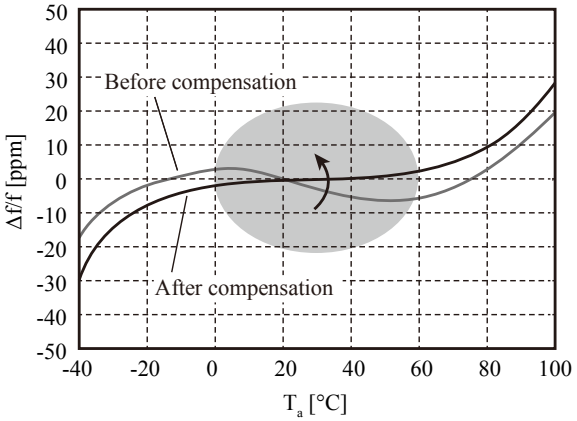


Figure 4. Temperature rotation compensation

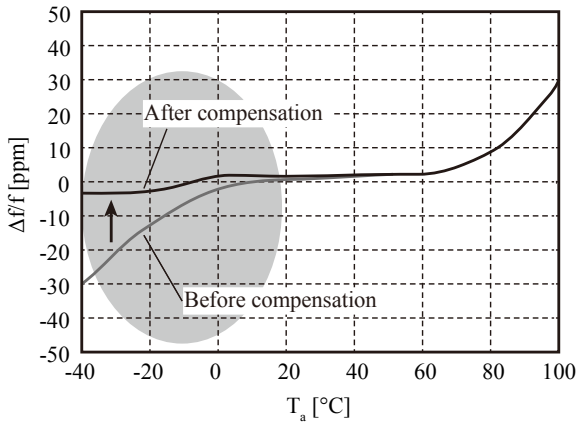


Figure 5. Low-temperature characteristics compensation

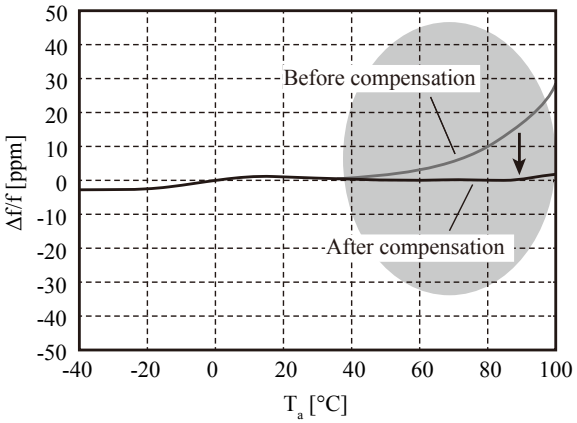


Figure 6. High-temperature characteristics compensation

Power-saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (OPEN, HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5043 series have an oscillation detection circuit.

The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

USAGE NOTES

Consideration for Mounting IC

Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5043 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

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