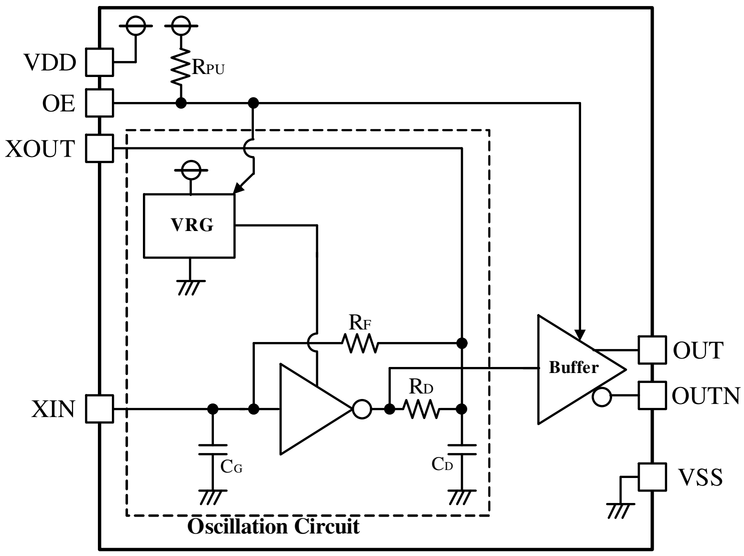
1. OVERVIEW

The CF7060xxV/WF7060xxV series are differential output oscillator ICs of the LVDS output type.
They support 125degree operation and wide range of output frequencies.
They are suitable for high frequency applications such as high speed communication devices.
They use an oscillation circuit suitable for small crystal elements, therefore suitable for a small package oscillation module.

2. FEATURES

■Operating supply voltage:	2.25V to 3.63V	
■Recommended oscillation frequency (f_0):	3rd overtone frequency	100MHz to 320MHz
	Fundamental frequency	100MHz to 320MHz
■Output frequency (f_{OUT}):	f_0	
■Oscillator capacitances:	C_G, C_D built-in	
■Output level:	LVDS	
■Standby function:	Oscillator stops, Hi-Z outputs, Power saving pull-up resistor built-in (OE output)	
■Oscillation detection circuit built-in		

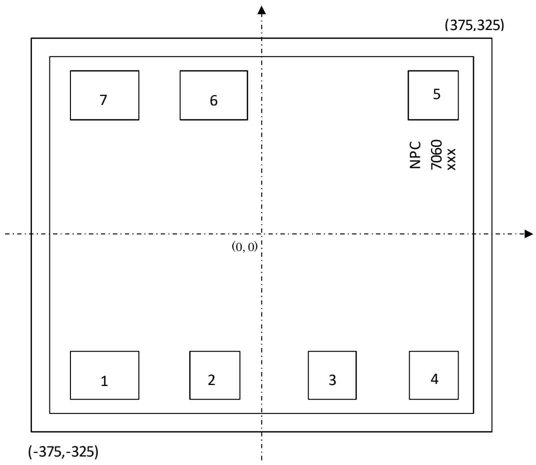
3. BLOCK DIAGRAM



4. PAD LAYOUT

(1) Chip size*1: X=0.75mm, Y=0.65mm
(2) Rear surface potential: V_{SS} level
(3) Pad size: No. 1, 6, 7:100μm × 80μm
No. 2, 3, 4, 5:80μm × 80μm
(4) Chip dimensions

*1. Chip size is measured between scribe line centers.



Pad Coordinates (Origin in chip center), Unit: [μm]

No.	X	Y	Name
1	-271	-231	VDD
2	-77	-231	XIN
3	115	-231	XOUT
4	281	-231	OE
5	281	231	VSS
6	-93	231	OUTN
7	-271	231	OUT

5. PAD DESCRIPTION

Number	Name	I/O*1	Function
1	VDD	-	(+) Supply voltage
2	XIN	I	Oscillator connections
3	XOUT	O	
4	OE	I	Output enable. Outputs are disabled when OE is V_{SS} level. Disabled state: Oscillator stopped, Hi-Z outputs
5	VSS	-	(-) Supply voltage
6	OUTN	O	output (inverting output) Disabled state: Hi-Z
7	OUT	O	output Disabled state: Hi-Z

*1. I : Input, O : Output

6. VERSION LINEUP

7060xxx
- Output level
- Output freqency
- Oscillation frequency range

(1) Version name 1st character (oscillation frequency range)

Version	Oscillation mode	Recommended C0 value (pF)*1	Oscillator capacitance (pF)*2		Oscillation frequency (reference values) f_0 (MHz)
			C_G	C_D	
D	3rd overtone Fundamental	1.0~ 2.0*3	4	11	100~135
E	3rd overtone Fundamental	1.0~ 2.0*3	4	9	135~175
F	3rd overtone Fundamental	1.0~ 2.0*3	2	4	175~250
G	3rd overtone Fundamental	1.0~ 2.0*3	0	1	250~320

*1. This is the recommended range based on the circuit design.
*2. Values do not include parasitic capacitance.
*3. This version has a C0 cancel circuit to ensure negative resistance at high frequency.
A self-oscillation becomes easy to happen coldly, so please be careful and do initial evaluation.

(2) Version name 2nd character (output frequency)

Version	Output frequency (f_{OUT})
1	f_0

(3) Version name 3rd character (Output level)

Version	Output level
V	LVDS

7. ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit	Notes
Supply voltage range	V_{DD}	Between VDD and VSS	-0.3 ~ +4.5	V	*1
Input voltage range1	V_{IN1}	OE	-0.3 ~ V_{DD}+0.3	V	*1、*2
Input voltage range2	V_{IN2}	XIN	-0.3 ~ +2.5	V	*1、*2
Output voltage range1	V_{OUT1}	OUT,OUTN	-0.3 ~ V_{DD}+0.3	V	*1、*2
Output voltage range2	V_{OUT2}	XOUT	-0.3 ~ +2.5	V	*1、*2
Junction temperature	T_j		+150	°C	*3
Storage temperature	T_{STG}	Chip, wafer form	-55 ~ +150	°C	*4

*1. Absolute maximum ratings are the values that must never exceed even for a moment. This product may suffer breakdown if any one of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored alone in nitrogen or vacuum atmosphere.

8. RECOMMENDED OPERATING CONDITIONS

V_{SS}=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillation frequency*1	f_0	-	100	-	320	MHz
Output frequency	f_{OUT}	-	100	-	320	MHz
Operating supply voltage	V_{DD}	VDD and VSS*2	2.25	-	3.63	V
Input voltage	V_{IN1}	OE	0	-	V_{DD}	V
	V_{IN2}	XIN	0	-	2.0	V
Operating temperature	T_a	-	-40	-	+125	°C
Output load resistance	R_L	Between OUT and OUTN	99	100	101	Ω

*1. The oscillation frequency range is a target based on evaluation results for the crystal element used for NPC characteristics verification, and does not represent a guarantee of the oscillation frequency band. The oscillation characteristics can vary significantly depending on the characteristics and mounting conditions of the crystal. Accordingly, oscillation characteristics should be thoroughly evaluated for each crystal.
*2. For stable operation of this product, please mount ceramic chip capacitor that is more than 0.01uF between VDD and VSS in close proximity to IC (within 3mm). Wiring pattern between IC and capacitor should be as thick as possible.
* Since it may influence the reliability if it is used out of the recommended operating conditions range, this product should be used within this range.

9. ELECTRICAL CHARACTERISTICS

9.1. DC Characteristics

Measurement circuits 1 and 2 in "Conditions" are shown in "12. MEASUREMENT CIRCUITS."

V_{DD}=2.25 to 3.63V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption	I_{DDD}	Measurement circuit 1, OE=Open f_0=125MHz, D1Vver	V_{DD}=3.3V	-	17.0	23.5	mA
	I_{DDE}	Measurement circuit 1, OE=Open f_0=156MHz, E1Vver	V_{DD}=3.3V	-	17.5	24.0	mA
	I_{DDF}	Measurement circuit 1, OE=Open f_0=200MHz F1Vver	V_{DD}=3.3V	-	22.0	30.0	mA
	I_{DDG}	Measurement circuit 1, OE=Open f_0=312MHz G1Vver	V_{DD}=3.3V	-	25.0	35.0	mA
Standby current	I_{STB}	Measurement circuit 1, OE= V_{SS}		-	-	30	µA
High-level output voltage	V_{OH}	Measurement circuit 2,OUT/OUTN		-	1.43	1.60	V
Low-level output voltage	V_{OL}	Measurement circuit 2, OUT/OUTN		0.90	1.10	-	V
Differential output voltage	V_{OD}	Measurement circuit 2, OUT/OUTN		247	330	454	mV
Differential output voltage error	ΔV_{OD}	Measurement circuit 2		-	-	50	mV
Offset voltage	V_{OS}	Measurement circuit 2, OUT-OUTN		1.125	1.250	1.375	V
Offset voltage error	ΔV_{OS}	Measurement circuit 2		-	-	50	mV

V_{DD}=2.25~3.63V, V_{SS}=0V, T_a=-40~+125°C

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High-level input	V_{IH}	Measurement circuit 1, OE	0.7V_{DD}	-	-	V
Low-level input voltage	V_{IL}	Measurement circuit 1, OE	-	-	0.3V_{DD}	V
OE pull-up resistance	R_{PU1}	Measurement circuit 1	0.5	1	2	MΩ
	R_{PU2}	Measurement circuit 1	30	70	150	kΩ
Oscillator feedback resistance (D1V ver.)	R_{FD}	Design value	1.8	2.3	2.9	kΩ
Oscillator feedback resistance (E1V ver.)	R_{FE}	Design value	1.8	2.3	2.9	kΩ
Oscillator feedback resistance (F1V ver.)	R_{FF}	Design value	2.4	3.1	3.9	kΩ
Oscillator feedback resistance (G1V ver.)	R_{FG}	Design value	1.5	1.9	2.4	kΩ
Oscillator capacitance (D1V ver.)	C_{GD}	Design value, Excludes parasitic capacitance	3.2	4.0	4.8	pF
	C_{DD}		8.8	11.0	13.2	
Oscillator capacitance (E1V ver.)	C_{GE}	Design value, Excludes parasitic capacitance	3.2	4.0	4.8	pF
	C_{DE}		7.2	9.0	10.8	
Oscillator capacitance (F1V ver.)	C_{GF}	Design value, Excludes parasitic capacitance	1.6	2.0	2.4	pF
	C_{DF}		3.2	4.0	4.8	
Oscillator capacitance (G1V ver.)	C_{GG}	Design value, Excludes parasitic capacitance	0.0	0.0	0.0	pF
	C_{DG}		0.8	1.0	1.2	

9.2. AC Characteristics

Measurement circuits 3 and 4 in "Conditions" are shown in "12. MEASUREMENT CIRCUITS."

V_{DD}=2.25 to 3.63V, V_{SS}=0V, T_a=-40 to +125°C unless otherwise noted

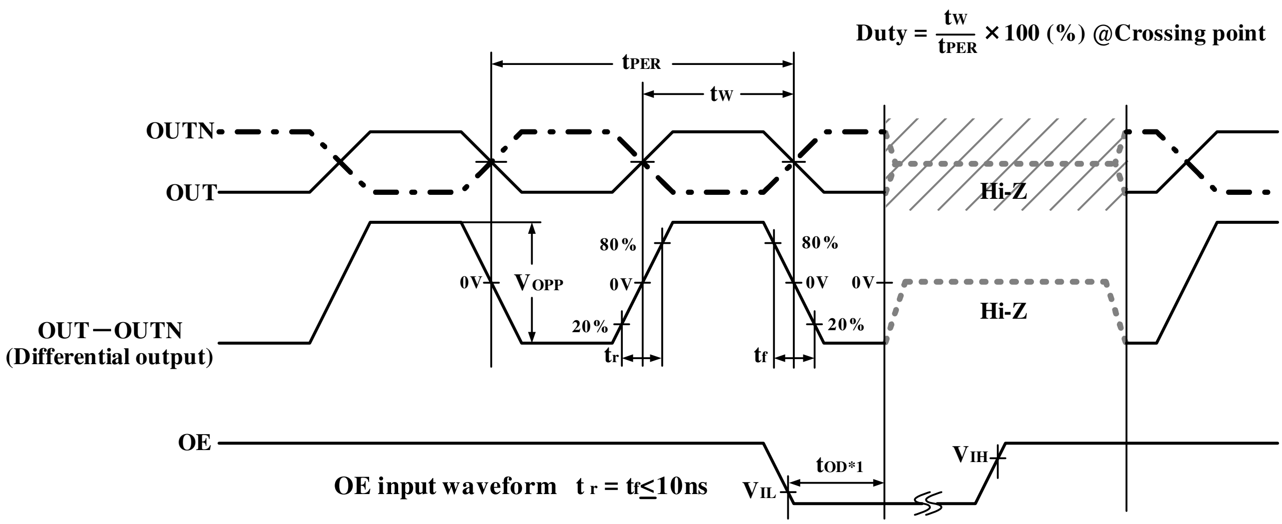
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output duty cycle	Duty	Measurement circuit 3 Measured at 0V crossover point of differential output signal	45	-	55	%
Output amplitude	V_{OPP}	Measurement circuit 3 Differential output signal	0.494	-	-	V
Output rise time	t_r	Measurement circuit 3 Measured between 20% and 80% amplitude of differential output signal	-	150	300	ps
Output fall time	t_f	Measurement circuit 3 Measured between 80% and 20% amplitude of differential output signal	-	150	300	ps
Output disable time	t_{OD}	Measurement circuit 4 Time measured OE=V_{IL} (falling edge) and outputs going Hi-Z (see timing diagram for details)	-	-	200	ns

*1. Since shipping inspection is not possible, it is guaranteed by characterization.

* The ratings above are values obtained by measurements using an NPC evaluation standard crystal element, standard testing jig, and evaluation package.
Ratings may have wide tolerances due to crystal element characteristics, evaluation jig, and package parasitic capacitance, so thorough evaluation is recommended.

9.3. Timing Diagram

The timing diagram applies to the “Conditions” in the table in “9.2. AC Characteristics.”

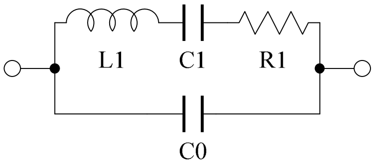


*1. When OE turns into LOW from HIGH, the output becomes Hi-Z.

図 9. LVDS Timing diagram

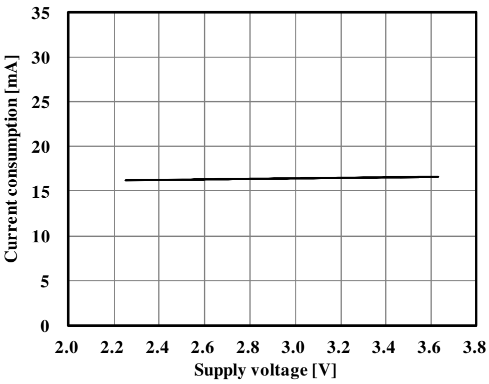
10. REFERENCE CHARACTERISTICS (Typical 7060 Characteristics)

The following characteristics assume the use of the following crystal element.
The characteristics will vary depending on the crystal used and the measurement conditions.

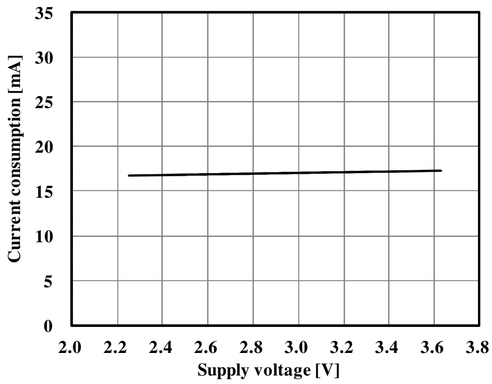


Parameter	f_0=122MHz	f_0=155.25MHz	f_0=200MHz	f_0=312.5MHz
C0(pF)	1.7	1.5	2.0	1.9
R1(Ω)	9	11	8.8	18
Oscillation mode	Fundamental	Fundamental	Fundamental	Fundamental

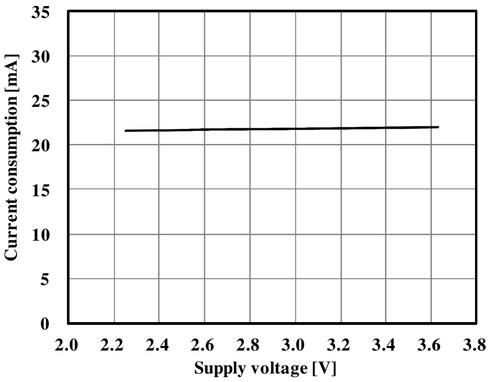
10.1. Current Consumption



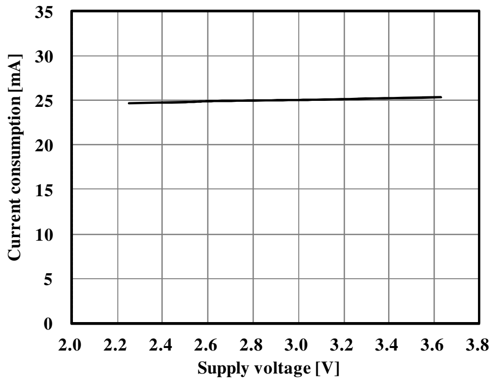
7060D1V, f_{OUT}=122MHz, T_a=25°C



7060E1V, f_{OUT}=155.52MHz, T_a=25°C

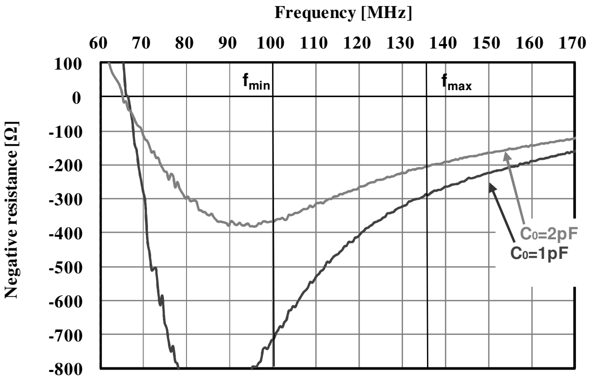


7060F1V, f_{OUT}=200MHz, T_a=25°C

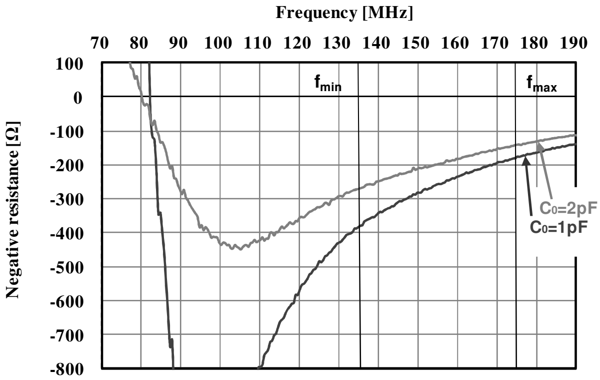


7060G1V, f_{OUT}=312.5MHz, T_a=25°C

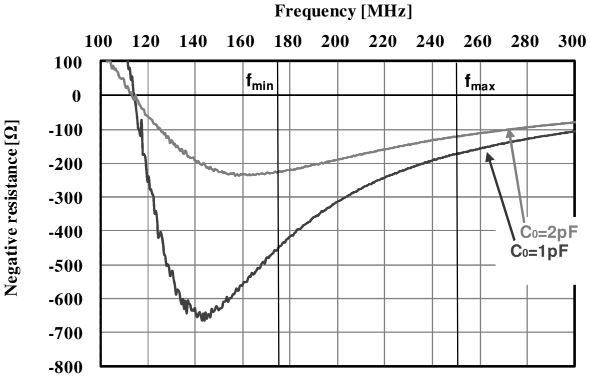
10.2. Negative Resistance



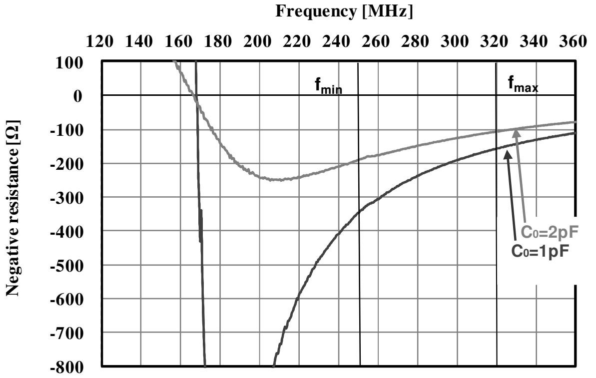
7060D1V, V_{DD}=3.3V, T_a=25°C



7060E1V, V_{DD}=3.3V, T_a=25°C

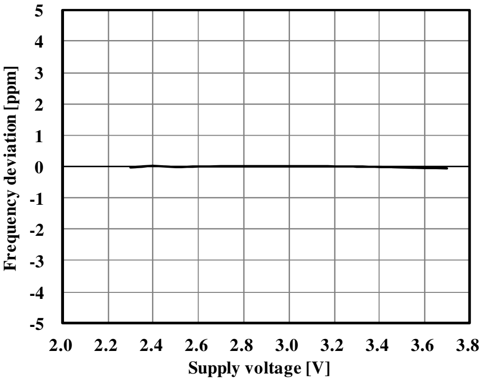


7060F1V, V_{DD}=3.3V, T_a=25°C

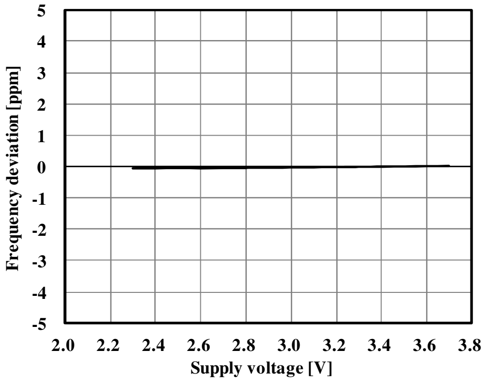


7060G1V, V_{DD}=3.3V, T_a=25°C

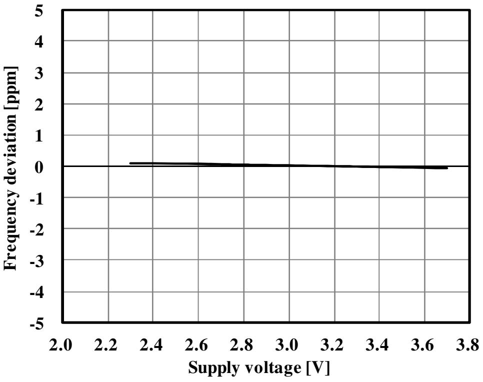
10.3. Frequency Deviation vs. Voltage



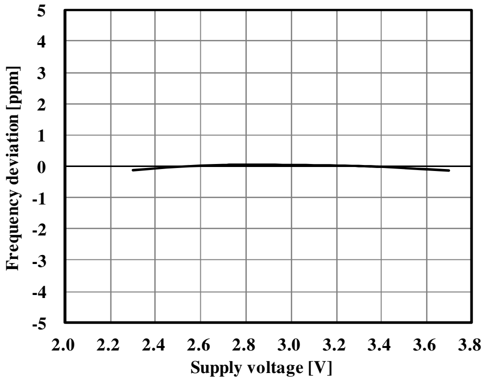
7060D1V, f_{OUT}=122MHz, T_a=25°C, 3.3V std.



7060E1V, f_{OUT}=155.52MHz, T_a=25°C, 3.3V std.



7060F1V, f_{OUT}=200MHz, T_a=25°C, 3.3V std.



7060G1V, f_{OUT}=312.5MHz, T_a=25°C, 3.3V std.

10.4. Drive Level

7060D1V, f_{OUT}=125MHz, T_a=25°C

V_{DD}[V]	Drive level [uW]
2.5	104.6
3.3	104.5

7060E1V, f_{OUT}=155.52MHz, T_a=25°C

V_{DD}[V]	Drive level [uW]
2.5	131.4
3.3	131.1

7060F1V, f_{OUT}=200MHz, T_a=25°C

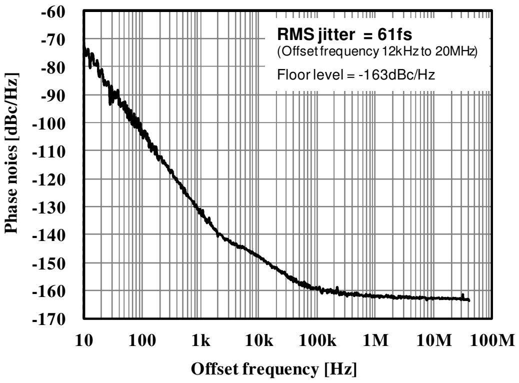
V_{DD}[V]	Drive level [uW]
2.5	234.2
3.3	234.5

7060G1V, f_{OUT}=312.5MHz, T_a=25°C

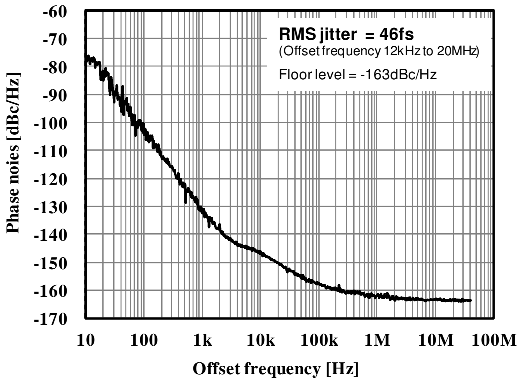
V_{DD}[V]	Drive level [uW]
2.5	638.2
3.3	633.1

10.5. Phase Noise

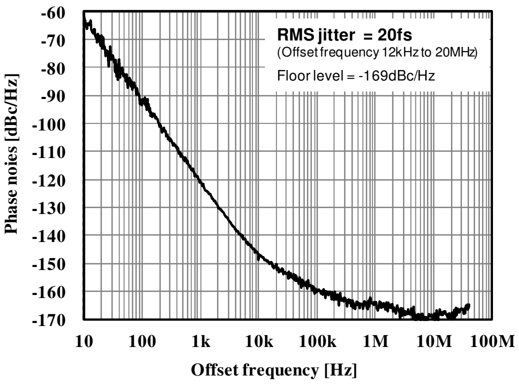
Measurement instrument: Agilent E5052B Signal Source Analyzer



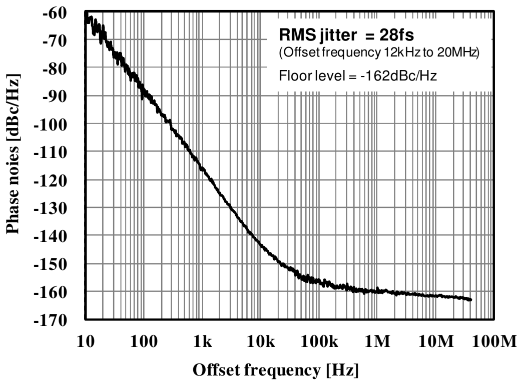
7060D1V, f_{OUT}=122MHz, V_{DD}=3.3V, T_a=25°C



7060E1V, f_{OUT}=155.52MHz, V_{DD}=3.3V, T_a=25°C



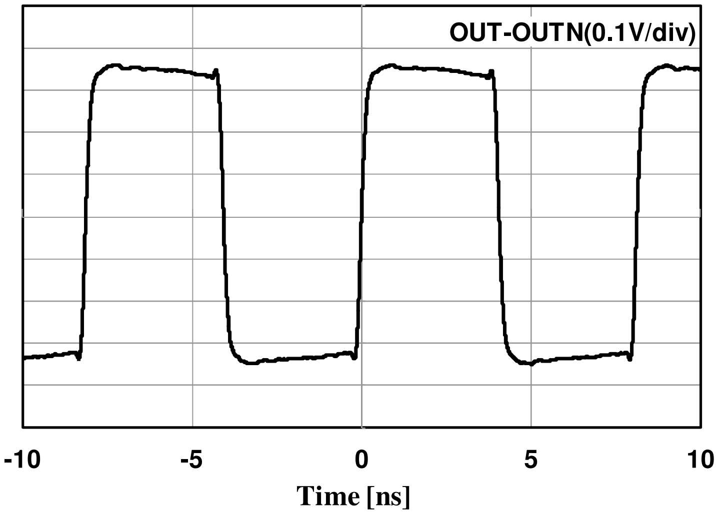
7060F1V, f_{OUT}=200MHz, V_{DD}=3.3V, T_a=25°C



7060G1V, f_{OUT}=312.5MHz, V_{DD}=3.3V, T_a=25°C

10.6. Output Waveforms

Measuring instrument: Agilent 80604B Oscilloscope

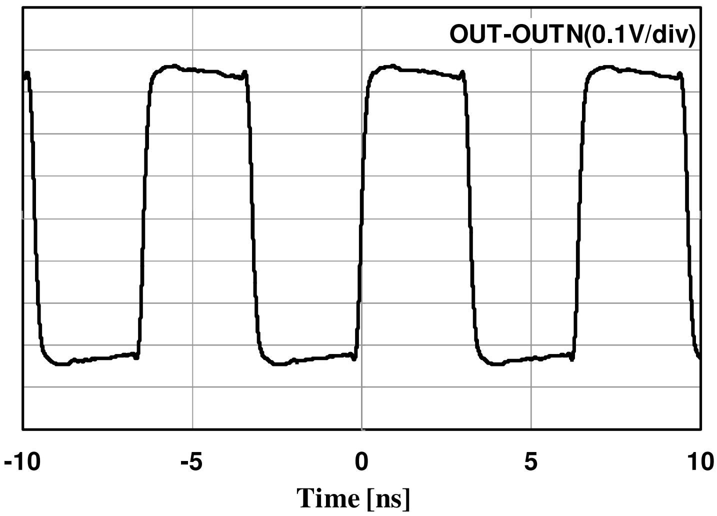


Duty = 50.5%

t_r = 187ps

t_f = 186ps

7060D1V, f_{OUT}=125MHz, V_{DD}=3.3V, T_a=25°C

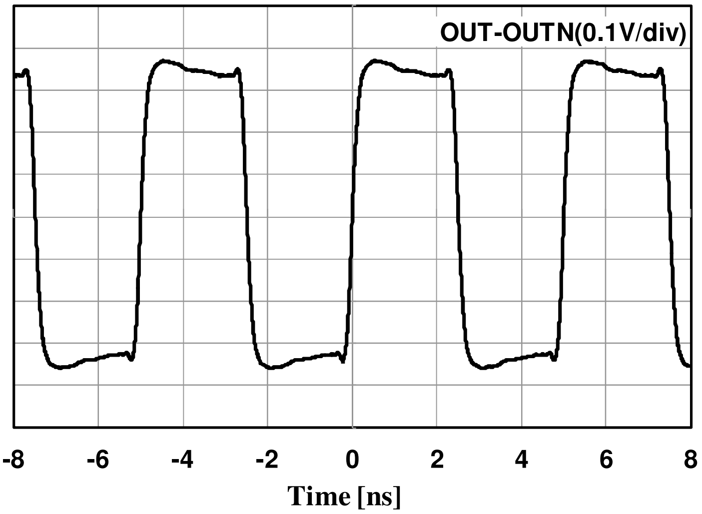


Duty = 50.8%

t_r = 189ps

t_f = 185ps

7060E1V, f_{OUT}=155.52MHz, V_{DD}=3.3V, T_a=25°C

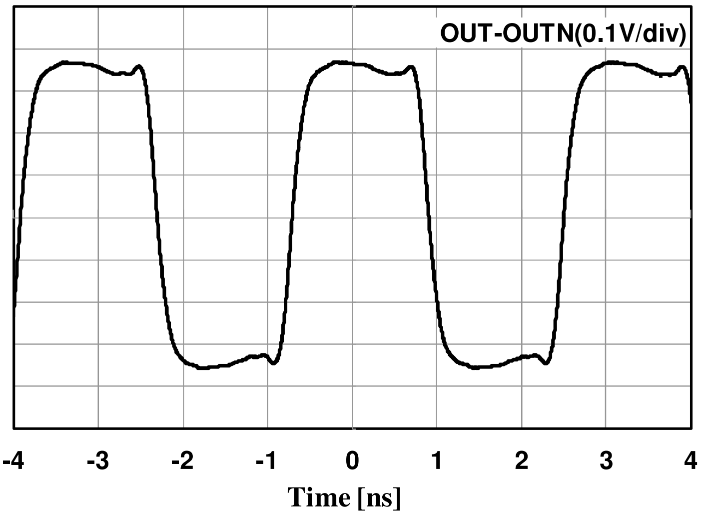


7060F1V, f_{OUT}=200MHz, V_{DD}=3.3V, T_a=25°C

Duty = 50.5%

t_r = 186ps

t_f = 191ps



7060G1V, f_{OUT}=312.5MHz, V_{DD}=3.3V, T_a=25°C

Duty = 50.1%

t_r = 185ps

t_f = 183ps

11. FUNCTIONAL DESCRIPTION

11.1. OE Function

When OE turns into V_{SS}, the OUT/OUTN outputs stop and become high impedance. This function is used to disable the operation of the device.

OE input	OUT/OUTN outputs	Oscillator circuit
V_{DD} or Open	f_0 output	Operating
V_{SS}	Hi-Z	Stopped

11.2. Power Saving Pull-up Resistor

The pull-up resistor built in the OE pin switches to RPU1 or RPU2 depending on the input level (“VDD” or “VSS”).

Fixing the OE pin to the VSS level increases the pull-up resistance value (RPU1) and reduces current consumption.

When the OE pin is used with VDD or open, the pull-up resistance value becomes small (RPU2) and it is less susceptible to external noise.

This fixes the inside of the OE pin to the VDD level and avoids the problem of output stopping suddenly.

11.3. Oscillation Detection Function

The IC has a built-in oscillation detection circuit.

The oscillation detection circuit disables the output circuit when the oscillator starts until the oscillation becomes stable. This function avoids the danger of unstable oscillation when the oscillator starts after power is first applied or the output is enabled.

11.4. C0 cancellation circuit

Oscillation circuit with a built-in C0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C0. It reduces the C0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C0.

This cancellation circuit makes it easier to maintain the oscillation margin.

12. MEASUREMENT CIRCUITS

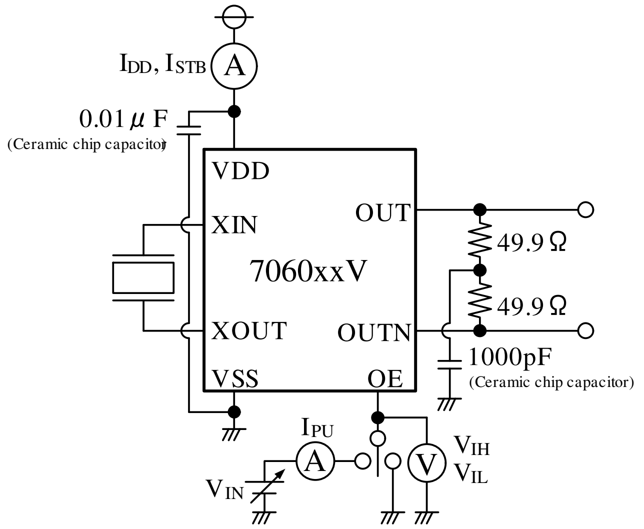
These measurement circuits are used for DC and AC characteristics evaluation.

***** Cautions for output waveform *****

To obtain good waveform characteristics, place a ceramic chip capacitor of 0.01 µF (or more) between the VDD and VSS pins of the IC (within about 3 mm).

12.1. LVDS

- **Measurement circuit 1 Measurement parameters: I_{DD}, I_{STB}, V_{IH}, V_{IL}, R_{PU1}, R_{PU2}**



$R_{PU1} = \frac{V_{DD}}{I_{PU}}$ ($V_{IN} = V_{SS}$)

$R_{PU2} = \frac{V_{DD} - 0.7V_{DD}}{I_{PU}}$ ($V_{IN} = 0.7V_{DD}$)

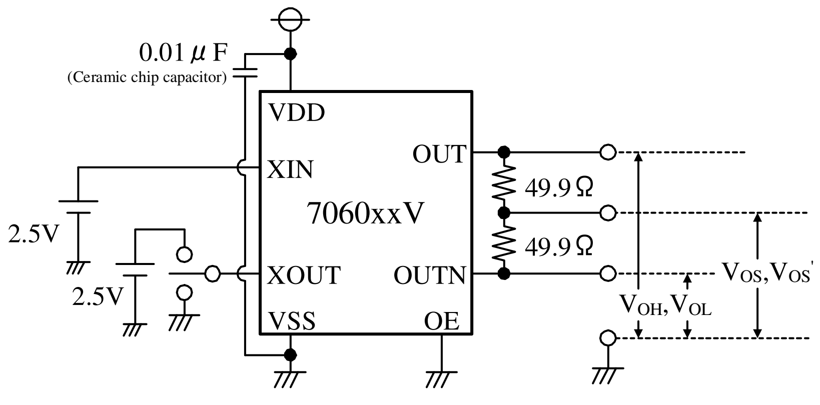
V_{IH} : $V_{SS} \rightarrow V_{DD}$ voltage that changes output state

V_{IL} : $V_{DD} \rightarrow V_{SS}$ voltage that changes output state

I_{STB} : OE=V_{SS}

Fig 12-1. Measurement circuit 1

- **Measurement circuit 2 Measurement parameters: V_{OH}, V_{OL}, V_{OD}, V_{OS}**



XOUT=V_{DD} { OUT =High, OUTN=Low }

XOUT=V_{SS} { OUT =Low, OUTN=High }

V_{OD} = OUT(High) - OUTN(Low)

V_{OD}' = OUTN(High) - OUT(Low)

$\Delta V_{OD} = |V_{OD} - V_{OD}'|$

V_{OS} : OUT=High, OUTN=Low

V_{OS}' : OUT=Low, OUTN=High

$\Delta V_{OS} = |V_{OS} - V_{OS}'|$

Fig 12-2. Measurement circuit 2

- **Measurement circuit 3 Measurement parameters: Duty, V_{OPP}, t_r, t_f**

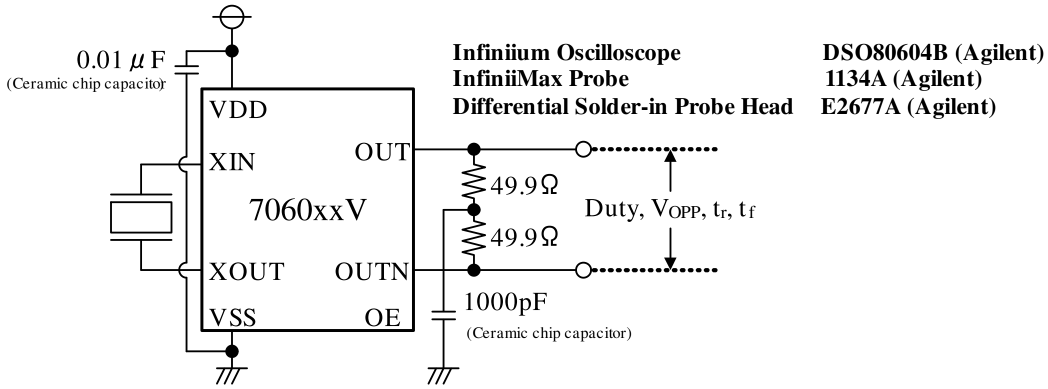


Fig 12-3. Measurement circuit 3

- **Measurement circuit 4 Measurement parameters: t_{OD}**

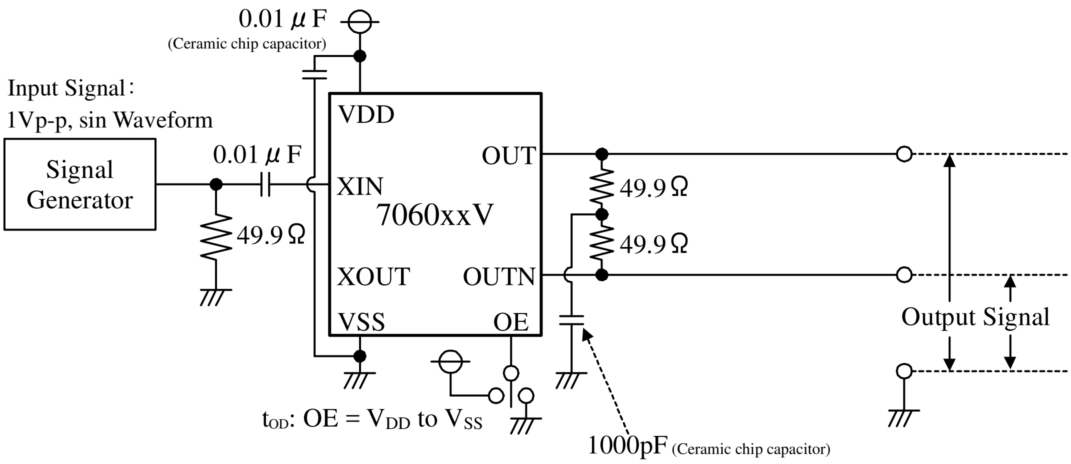
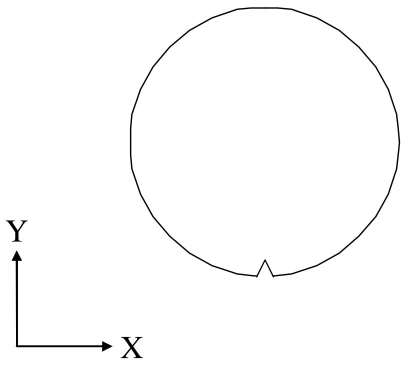


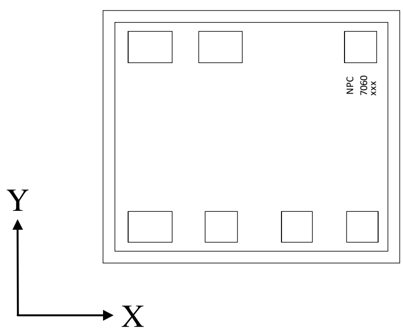
図 12-4. Measurement circuit 4

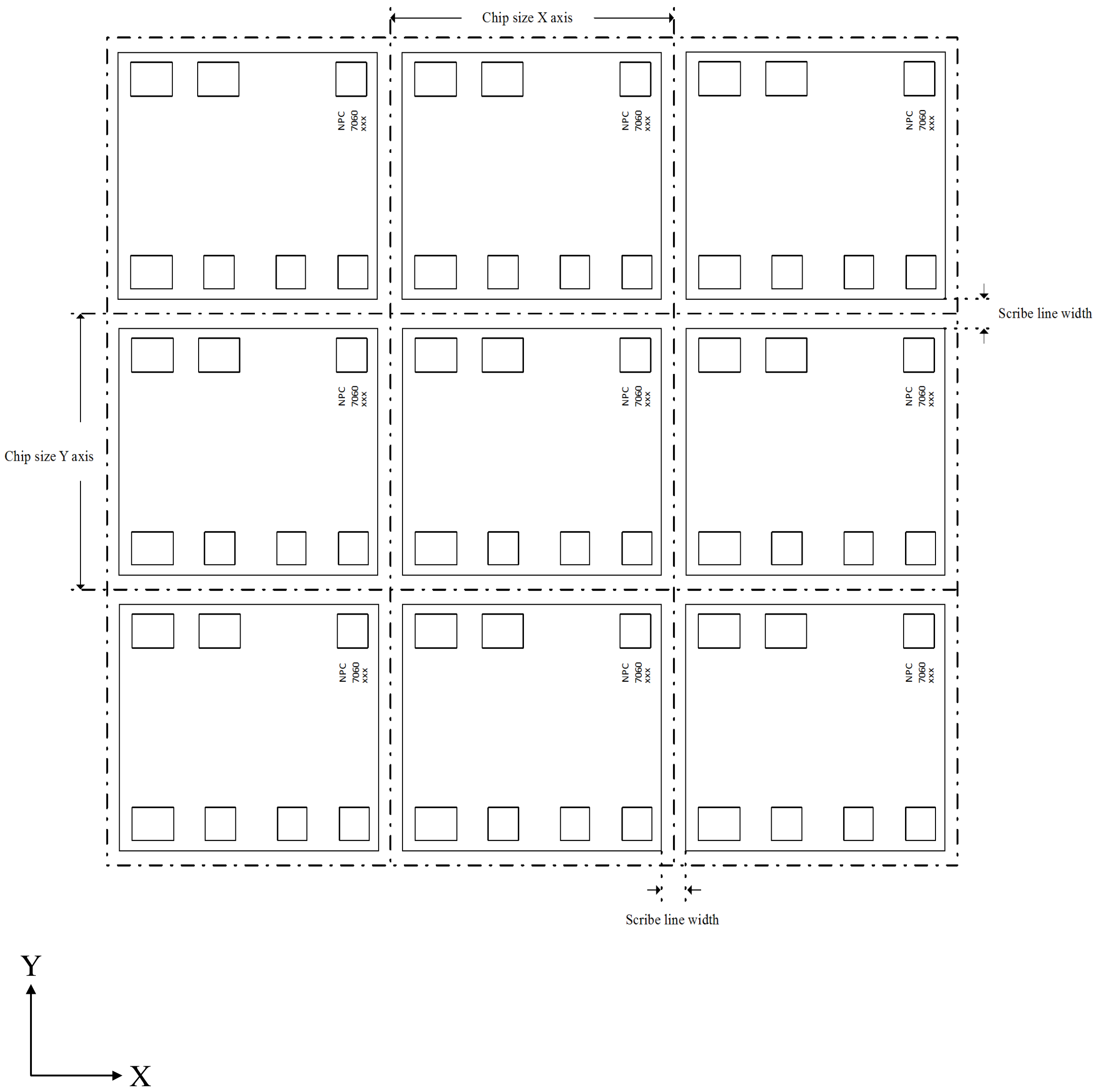
13. WAFER SURFACE DIAGRAM

Wafer size: 200mm±0.5mm

Scribe line width: 60μm

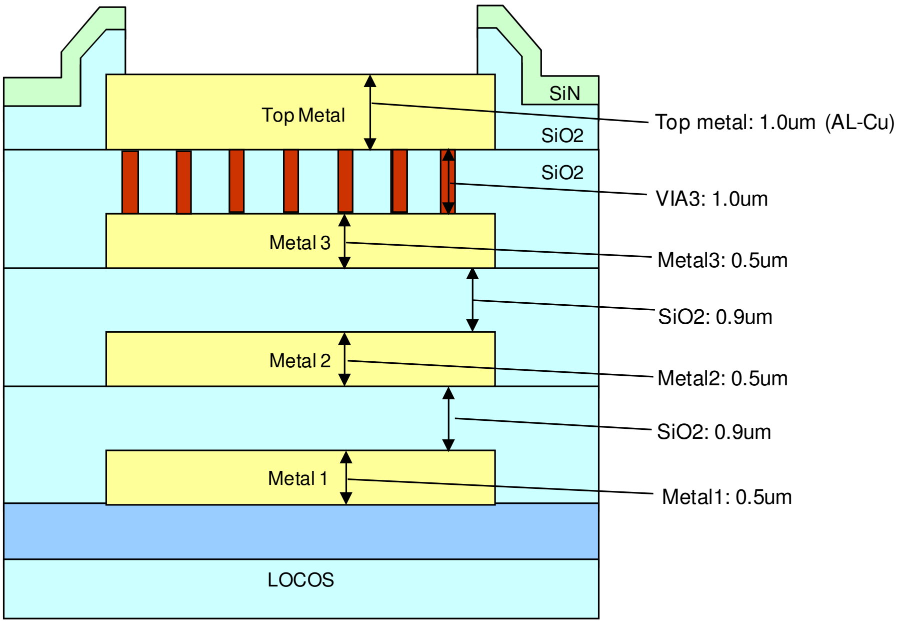






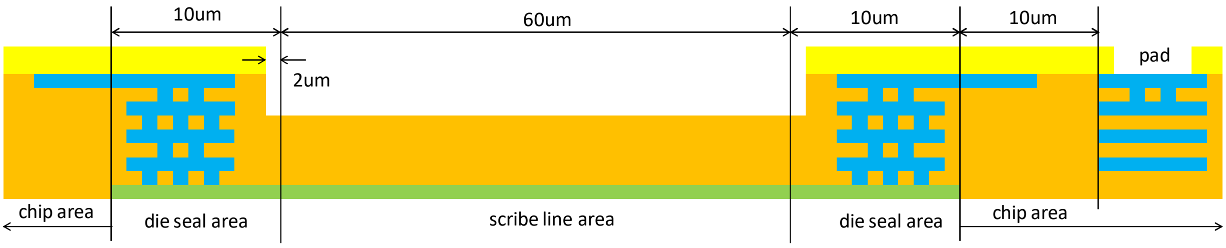
14. CROSS SECTION STRUCTURE

14.1. PAD Cross Section Structure



*Film thickness of mention is a value in the designs as above and is not the actual value in the chip.

14.2. Seal Ring and Scribe Line Cross Section Structure



*Width of mention is a value in the designs as above and is not the actual value in the chip.

<Notes on UBM formation>

In UBM (Under Bump Metal) formation to the mounting pad electrode by electroless plating, UBM is similarly formed on the scribe line TEG and the metal exposed part of the accessory. So mask process covering the scribe line is required to prevent these effects.

15. USAGE AND PRECAUTIONS

This product is designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools, and measurement equipment. This product is not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment.
If you wish to use this product in equipment requiring extremely high level of reliability, please contact our sales department or representative in advance.

In the event that this product is used in such equipment, please take scrupulous care and apply fail-safe techniques including redundancy and malfunction prevention in order to prevent damage to life, health, property, or infrastructure etc. in case there is some malfunction in the product.

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