OVERVIEW

The 5077 series are LV-PECL output VCXO ICs that provide a wide frequency pulling range. They employ bipolar oscillator circuit and recently developed varicap diode fabrication process that provides a low phase noise characteristic and a wide frequency pulling range without any external components. The 5077 series are ideal for wide pulling range, low phase noise, VCXO modules.

FEATURES

- VCXO with recently developed varicap diode built-in
- Oscillator: Fundamental frequency oscillation
- Output frequency: 30 to 170MHz
- Operating supply voltage range: 2.97 to 3.63V
- Oscillator frequency range (for fundamental oscillation):
  60 to 100MHz (Ax version)
  100 to 170MHz (Bx version)
- -40 to +85°C operating temperature range
- Differential LV-PECL output
- Frequency divider built-in
  Selectable by version: f_{OSC}, $f_{OSC}/2$
- Output enable (OE) active selectable function
  Selectable Hi-Active or Low-Active by bonding wire
- Wide frequency pulling range (typ)
  (±150ppm)@A1 version, V_C=1.65±1.65V, f=77.76MHz (γ=356, C0=3.0pF)
  ±130ppm@B1 version, V_C=1.65±1.65V, f=155.52MHz (γ=327, C0=1.4pF)
- Low phase noise (typ) : (-130dBc/Hz)@A1 version, 1kHz Offset, f=77.76MHz (γ=356, C0=3.0pF)
  (-148dBc/Hz)@A1 version, 10MHz Offset, f=77.76MHz
  -125dBc/Hz@B1 version, 1kHz Offset, f=155.52MHz (γ=327, C0=1.4pF)
  -148dBc/Hz@B1 version, 10MHz Offset, f=155.52MHz

APPLICATIONS

SONET/SDH, Ethernet, Fibre Channel

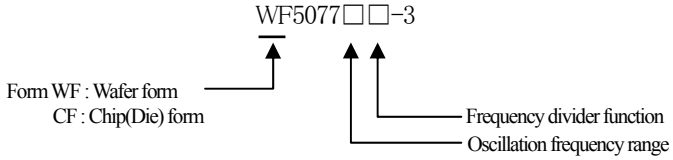
SERIES CONFIGURATION

Version Name[*1]	Recommended operating frequency range (f_{OSC})[*2] [MHz]	Output frequency (f_{OUT})
(5077A1)	60MHz to 100MHz	f_{OSC}
(5077A2)	60MHz to 100MHz	$f_{OSC}/2$
5077B1	100MHz to 170MHz	f_{OSC}
(5077B2)	100MHz to 170MHz	$f_{OSC}/2$

*1. The version name with parentheses is being developed.

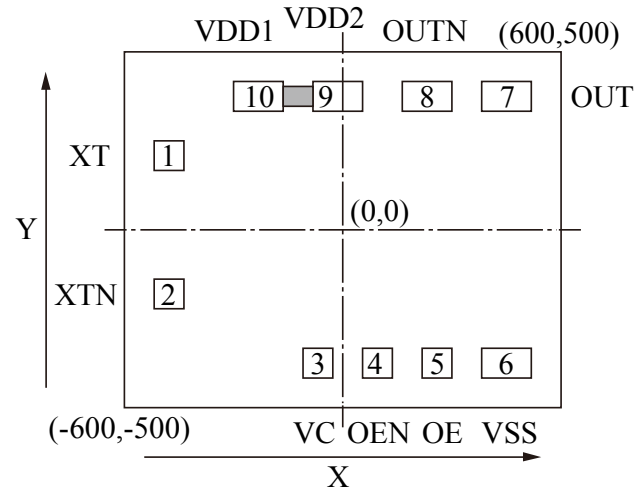
*2. The recommended oscillation frequency is a yardstick value derived from the resonator used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to resonator characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
The recommended characteristics for the crystal element are:
Ax versions: R1 < 20Ω, C0 < 1.5pF
Bx versions: R1 < 20Ω, C0 < 1.5pF

ORDERING INFORMATION

Device	Package	Version name
WF5077xx-3	Wafer form	
CF5077xx-3	Chip form	

PAD LAYOUT

(Unit: μm)



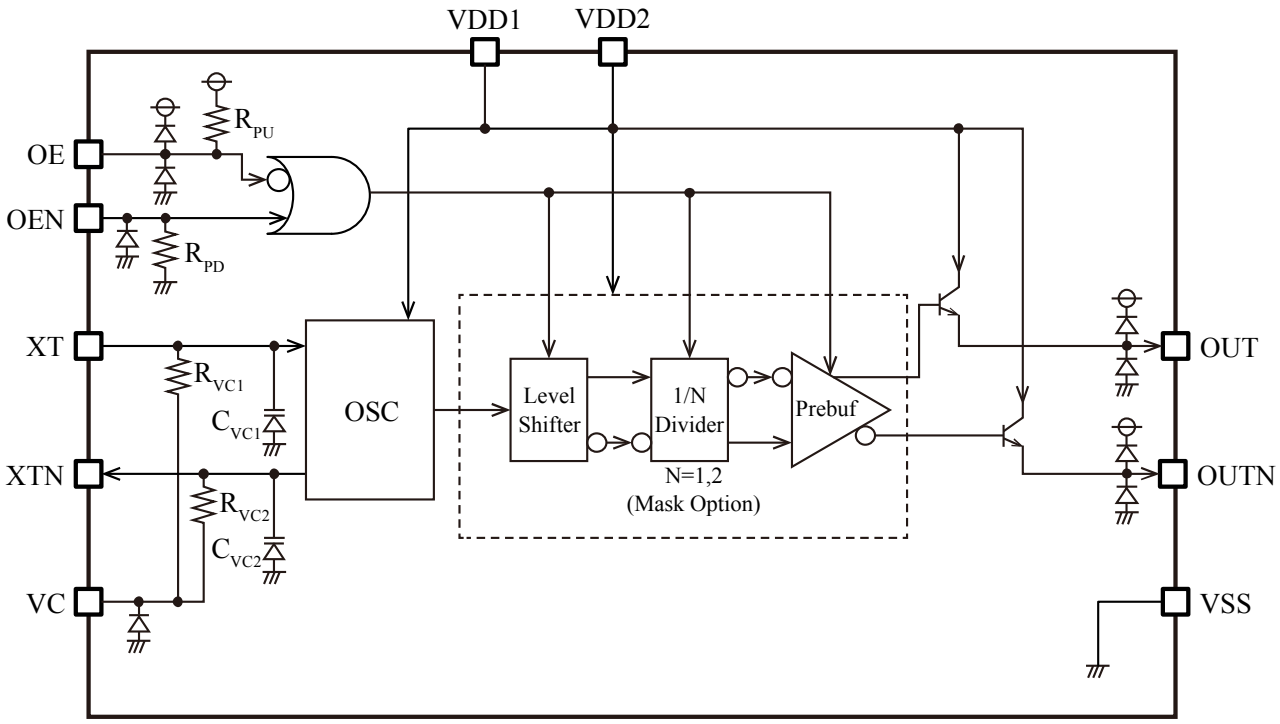
Chip size: 1.2mm×1.0mm
Chip thickness: 180μm
PAD size: 80μm×80μm (PAD No.1, 2, 3, 4, 5 pins)
110μm×80μm (PAD No.6, 7, 8, 9, 10 pins)
Chip base: V_{SS} potential

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O*1	Description	Pad Coordinates (Unit : μm)	
				X	Y
1	XT	I	Crystal connection pin	-490	206.6
2	XTN	O		-490	-110.2
3	VC	I	Control voltage input pin	-54.8	-390
4	OEN	I	Output enable input pin (built-in pull-down resistor)	127.8	-390
5	OE	I	Output enable input pin (built-in pull-up resistor)	291.2	-390
6	VSS	-	(-) ground	475	-390
7	OUT	O	Clock output pin (differential output)	459	390
8	OUTN	O	Clock output pin (differential reversing output)	229.2	390
9	VDD2*2	-	(+) supply voltage for output buffer	35.8	390
10	VDD1*2	-	(+) supply voltage	-122.5	390

*1.I: input, O: output
*2. It recommends to do wire bonding each voltage pin of package though VDD1 and VDD2 are connected by wire in the chip.

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range*1	V_{DD}	VDD1, VDD2 pins	-0.3 to +5.0	V
Input voltage range*1*2	V_{IN}	XT, OE, OEN, VC pins	-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	XTN, OUT, OUTN pins	-0.3 to V_{DD}+0.3	V
Junction temperature*3	T_j		+125	°C
Storage temperature range*4	T_{STG}	Wafer, Chip form	-55 to +125	°C

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Operating supply voltage	V_{DD}	Between VDD1, VDD2 and VSS pins*2	2.97	3.3	3.63	V
Input voltage	V_{IN}	OE, OEN, VC pins	0		V_{DD}	V
Operating temperature	T_a		-40		+85	°C
Output load	R_L	Terminated to V_{DD}-2V	49.5	50.0	50.5	Ω
Oscillator frequency range*1	f_{OSC}	5077Ax	60		100	MHz
		5077Bx	100		170	
Output frequency range	f_{OUT}	5077A1	60		100	MHz
		5077A2	30		50	
		5077B1	100		170	
		5077B2	50		85	

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD1, VDD2 and VSS in order to obtain stable operation of 5077 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
A1, A2 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +85°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating MIN	Rating TYP	Rating MAX	Unit
Current consumption1	I_{DD1}	measurement circuit 1, terminated to V_{DD}-2V, OE,OEN=Open			59	80	mA
Current consumption2	I_{DD2}	measurement circuit 1, terminated to V_{DD}-2V, OE=Low or OEN=High oscillator: operating, output: stopped			1.2	2.5	mA
High-level output voltage (DC level)	V_{OH}	measurement circuit 2, V_{DD}=3.3V, OUT/OUTN pins	T_a=0 to +85°C	2.275	2.350	2.420	V
			T_a=-40 to 0°C	2.215	2.295	2.420	
Low-level output voltage (DC level)	V_{OL}	measurement circuit 2, V_{DD}=3.3V, OUT/OUTN pins	T_a=0 to +85°C	1.490	1.600	1.680	V
			T_a=-40 to 0°C	1.490	1.605	1.745	
Output leakage current	I_Z	measurement circuit 4, SW1,2=High or Low OE=Low or OEN=High OUT/OUTN pins, T_a=25°C		-1		1	µA
High-level input voltage	V_{IH}	measurement circuit 3, OE/OEN pins		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 3, OE/OEN pins				0.3V_{DD}	V
Pull-up resistance	R_{PU}	measurement circuit 3, OE pin		50	100	200	kΩ
Pull-down resistance	R_{PD}	measurement circuit 3, OEN pin		50	100	200	kΩ
Oscillator block built-in resistance	R_{VC1}	Between VC and XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC and XTN, measurement circuit 5		100	200	300	
Input leakage resistance	R_{VIN}	VC pin, T_a=25°C, measurement circuit 6		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C=0.3V	5.88	6.53	7.18	pF
			V_C=1.65V	3.51	4.13	4.75	
			V_C=3.0V	1.80	2.25	2.70	
	C_{VC2}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C=0.3V	8.82	9.80	10.78	pF
			V_C=1.65V	5.27	6.20	7.13	
			V_C=3.0V	2.70	3.38	4.06	
Maximum modulation frequency	F_M	-3dB frequency, T_a=25°C, design value V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 9, Crystal : 77.76MHz		20	40		kHz

B1, B2 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +85°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating			Unit
				MIN	TYP	MAX	
Current consumption1	I_{DD1}	measurement circuit 1, terminated to V_{DD}-2V, OE,OEN=Open			60	80	mA
Current consumption2	I_{DD2}	measurement circuit 1, terminated to V_{DD}-2V, OE=Low or OEN=High oscillator: operating, output: stopped			2.3	3.5	mA
High-level output voltage (DC level)	V_{OH}	measurement circuit 2, V_{DD}=3.3V, OUT/OUTN pins	T_a=0 to +85°C	2.275	2.350	2.420	V
			T_a=-40 to 0°C	2.215	2.295	2.420	
Low-level output voltage (DC level)	V_{OL}	measurement circuit 2, V_{DD}=3.3V, OUT/OUTN pins	T_a=0 to +85°C	1.490	1.600	1.680	V
			T_a=-40 to 0°C	1.490	1.605	1.745	
Output leakage current	I_Z	measurement circuit 4, SW1,2=High or Low OE=Low or OEN=High OUT/OUTN pins, T_a=25°C		-1		1	µA
High-level input voltage	V_{IH}	measurement circuit 3, OE/OEN pins		0.7V_{DD}			V
Low-level input voltage	V_{IL}	measurement circuit 3, OE/OEN pins				0.3V_{DD}	V
Pull-up resistance	R_{PU}	measurement circuit 3, OE pin		50	100	200	kΩ
Pull-down resistance	R_{PD}	measurement circuit 3, OEN pin		50	100	200	kΩ
Oscillator block built-in resistance	R_{VC1}	Between VC and XT, measurement circuit 5		100	200	300	kΩ
	R_{VC2}	Between VC and XTN, measurement circuit 5		100	200	300	
Input leakage resistance	R_{VIN}	VC pin, T_a=25°C, measurement circuit 6		10			MΩ
Oscillator block built-in capacitance	C_{VC1}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C=0.3V	3.92	4.36	4.80	pF
			V_C=1.65V	2.35	2.76	3.17	
			V_C=3.0V	1.20	1.50	1.80	
	C_{VC2}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C=0.3V	5.88	6.53	7.18	pF
			V_C=1.65V	3.51	4.13	4.75	
			V_C=3.0V	1.80	2.25	2.70	
Maximum modulation frequency	F_M	-3dB frequency, T_a=25°C, design value V_{DD}=3.3V, V_C=1.65V±1.65V, measurement circuit 9, Crystal : 155.52MHz		20	40		kHz

Switching Characteristics

A1, A2 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +85°C unless otherwise noted

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Duty cycle	Duty1	Measured at output cross point T_a=25°C, V_{DD}=3.3V, measurement circuit 7	45	50	55	%
	Duty2	Measured at 50% of output amplitude T_a=25°C, V_{DD}=3.3V, measurement circuit 7	45	50	55	%
Output amplitude	V_{OPP}	Peak to peak of output waveform Single-ended output signal, measurement circuit 7	0.4			V
Output rise time	t_r	20% to 80% of output amplitude Single-ended output signal, measurement circuit 7		0.3	1.0	ns
Output fall time	t_f	80% to 20% of output amplitude Single-ended output signal, measurement circuit 7		0.3	1.0	ns
Output enable propagation delay*1	t_{OE}	T_a=25°C, design value, measurement circuit 8			20	µs
Output disable propagation delay	t_{OD}	T_a=25°C, design value, measurement circuit 8			200	ns

*1. Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated. The recommended crystal element characteristics are R1 < 20Ω and C0 < 1.5pF.

B1, B2 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +85°C unless otherwise noted

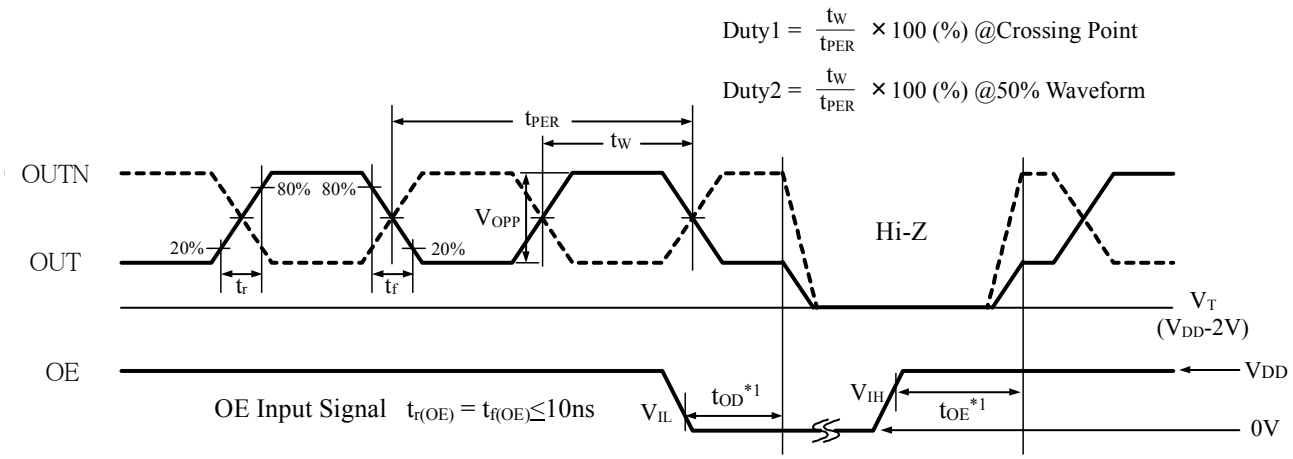
Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Duty cycle	Duty1	Measured at output cross point T_a=25°C, V_{DD}=3.3V, measurement circuit 7	45	50	55	%
	Duty2	Measured at 50% of output amplitude T_a=25°C, V_{DD}=3.3V, measurement circuit 7	45	50	55	%
Output amplitude	V_{OPP}	Peak to peak of output waveform Single-ended output signal, measurement circuit 7	0.4			V
Output rise time	t_r	20% to 80% of output amplitude Single-ended output signal, measurement circuit 7		0.3	1.0	ns
Output fall time	t_f	80% to 20% of output amplitude Single-ended output signal, measurement circuit 7		0.3	1.0	ns
Output enable propagation delay*1	t_{OE}	T_a=25°C, design value, measurement circuit 8			20	µs
Output disable propagation delay	t_{OD}	T_a=25°C, design value, measurement circuit 8			200	ns

*1. Rating may vary depending on the power supply used, values of bypass capacitors, and other factors.

Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated. The recommended crystal element characteristics are R1 < 20Ω and C0 < 1.5pF.

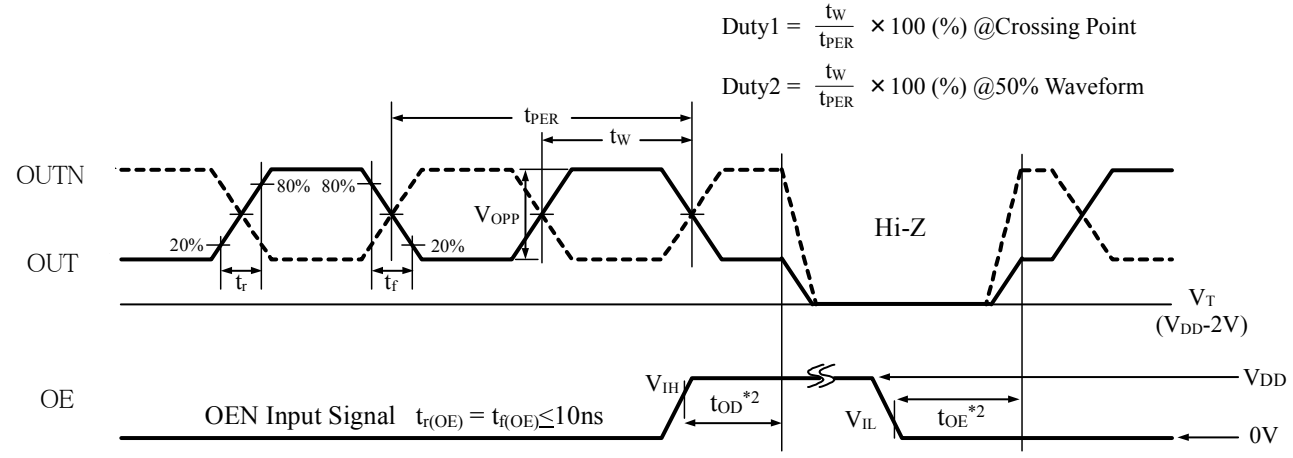
Timing chart

[Used OE pin]



*1. On an OE falling edge, the outputs go high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) has elapsed. When this occurs, the output signal is pulled down to V_T (termination voltage) by the load resistance. On an OE rising edge, the output starts after the output enable propagation delay (t_{OE}) has elapsed.

[Used OEN pin]



*2. On an OE falling edge, the outputs go high impedance (Hi-Z) after the output disable propagation delay (t_{OD}) has elapsed. When this occurs, the output signal is pulled down to V_T (termination voltage) by the load resistance. On an OE rising edge, the output starts after the output enable propagation delay (t_{OE}) has elapsed.

FUNCTIONAL DESCRIPTION

OE Function

OE pin (built-in pull-up resistor)	OEN pin (built-in pull-down resistor)	Oscillator	Output
High/Open	Low/Open	Operating	Operating
Low	Open	Operating	Stopped (Hi-Z)
Open	High	Operating	Stopped (Hi-Z)
Low	High	Unavailable TEST mode (V_{OH}, V_{OL})	

Oscillation Start-up Detector Function

The 5077 series also feature an oscillation start-up detector circuit. This circuit functions to disable the outputs until the oscillation starts. This prevents unstable oscillator output at oscillator start-up when power is applied.

MEASUREMENT CIRCUITS

These are measurement circuits for electrical characteristics and switching characteristics.

■ Note: Bypass capacitors specified in each measurement circuit below should be connected between VDD1, VDD2, V_T and VSS. Load resistance specified in each measurement circuit below should be connected to OUT and OUTN pins (excluding measurement circuit 4, 5, 6).

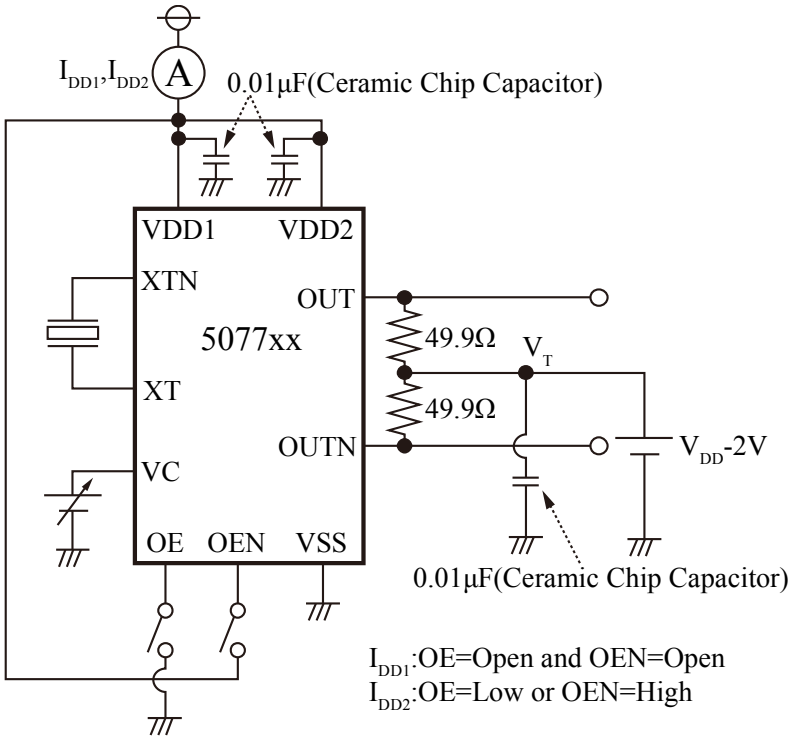
Circuit wiring of bypass capacitors and load resistance should be connected as short as possible (within approximately 3mm). If the circuit wiring is long, the required characteristics may not be realized. Also, if the values of bypass capacitors and load resistance differ from the description in this document or are not connected, the required characteristics may not be realized.

* The capacitor and resistor used in measurement circuits below;

GRM188B11H103K (MURATA)	0.01μF
RN732ATTD49R9B25 (KOA)	49.9Ω

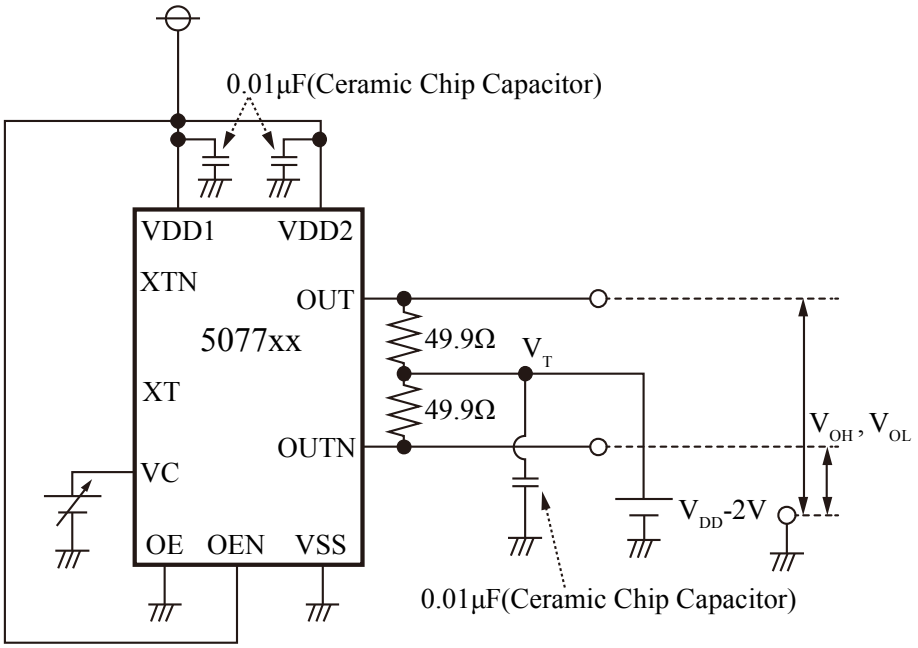
MEASUREMENT CIRCUIT 1

Measurement Parameters: I_{DD1}, I_{DD2}



MEASUREMENT CIRCUIT 2

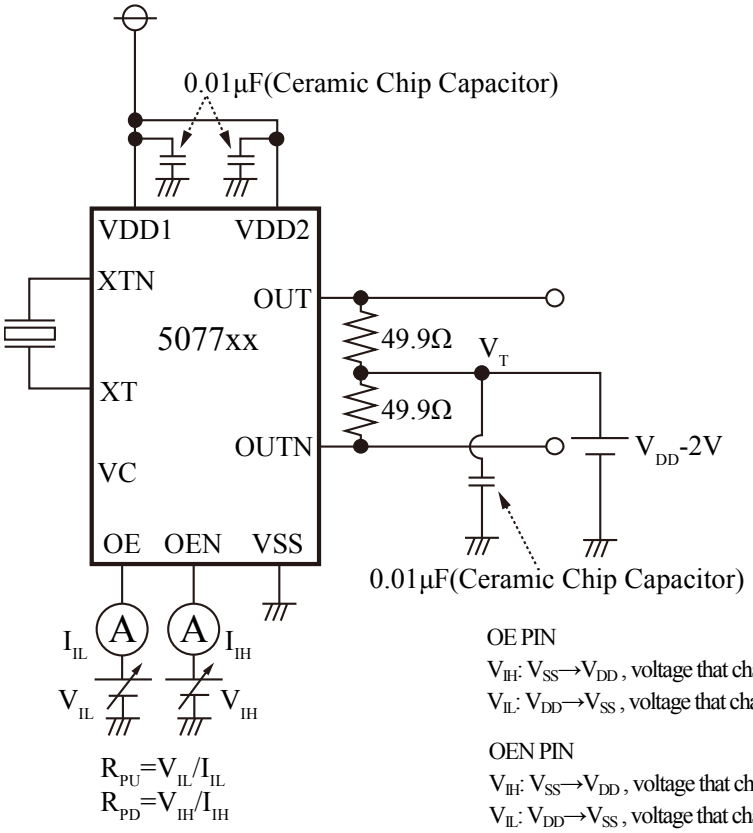
Measurement Parameters: V_{OH}, V_{OL}



V_C=High:OUT=V_{OH},OUTN=V_{OL}
V_C=Low:OUT=V_{OL},OUTN=V_{OH}

MEASUREMENT CIRCUIT 3

Measurement Parameters: R_{PU}, R_{PD}, V_{IH}, V_{IL}



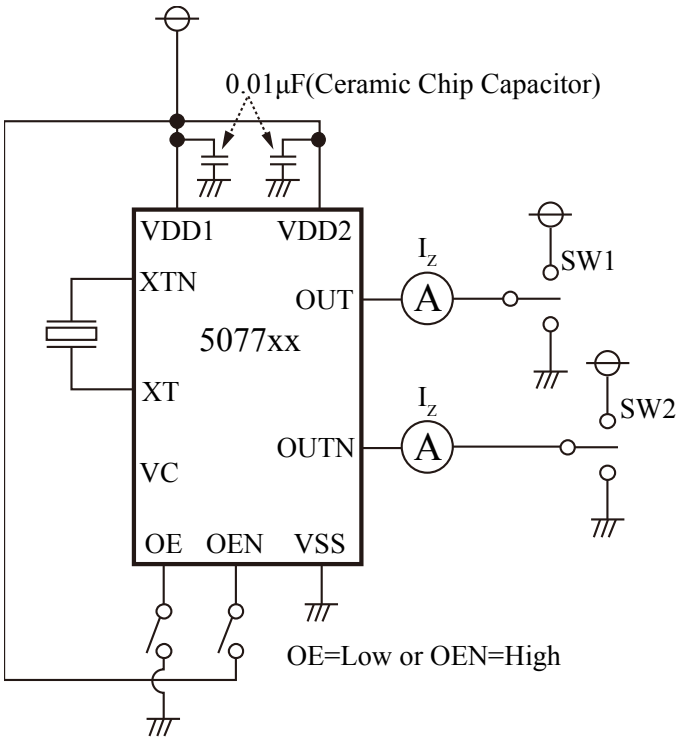
R_{PU}=V_{IL}/I_{IL}
R_{PD}=V_{IH}/I_{IH}

OE PIN
V_{IH}: V_{SS}→V_{DD} , voltage that changes enable output state
V_{IL}: V_{DD}→V_{SS} , voltage that changes disable output state

OEN PIN
V_{IH}: V_{SS}→V_{DD} , voltage that changes disable output state
V_{IL}: V_{DD}→V_{SS} , voltage that changes enable output state

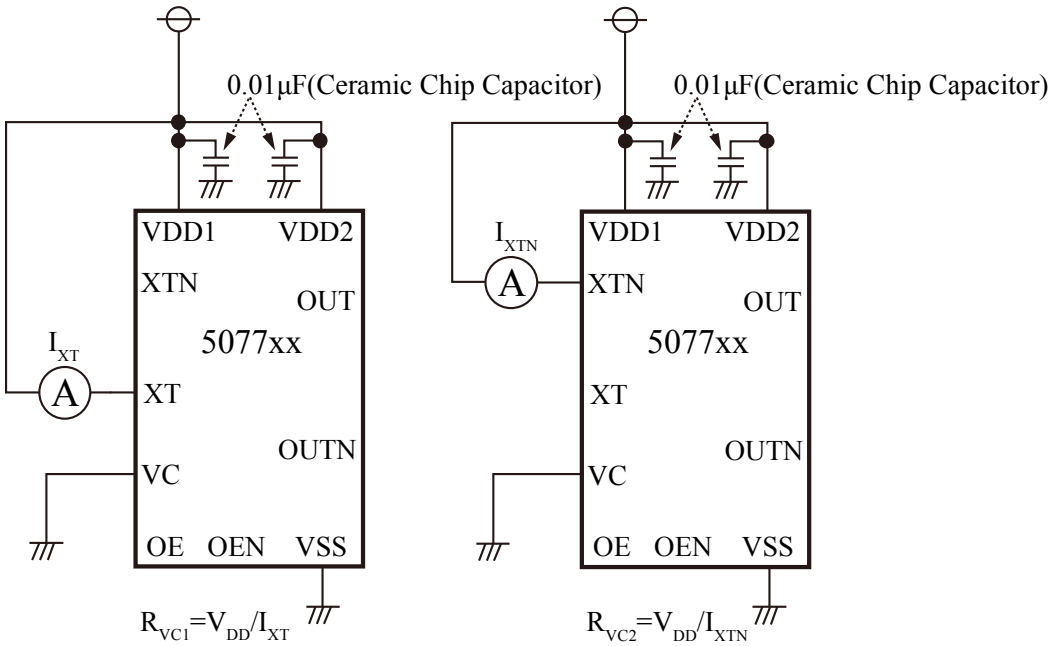
MEASUREMENT CIRCUIT 4

Measurement Parameters: I_Z



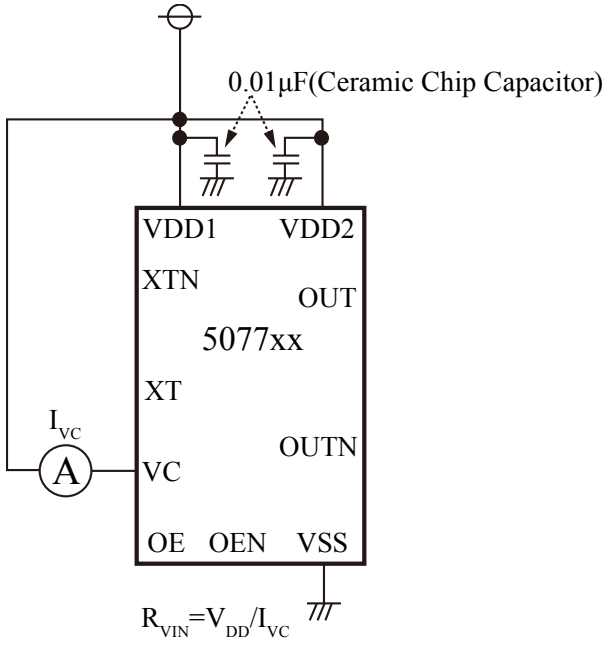
MEASUREMENT CIRCUIT 5

Measurement Parameters: R_{VC1}, R_{VC2}



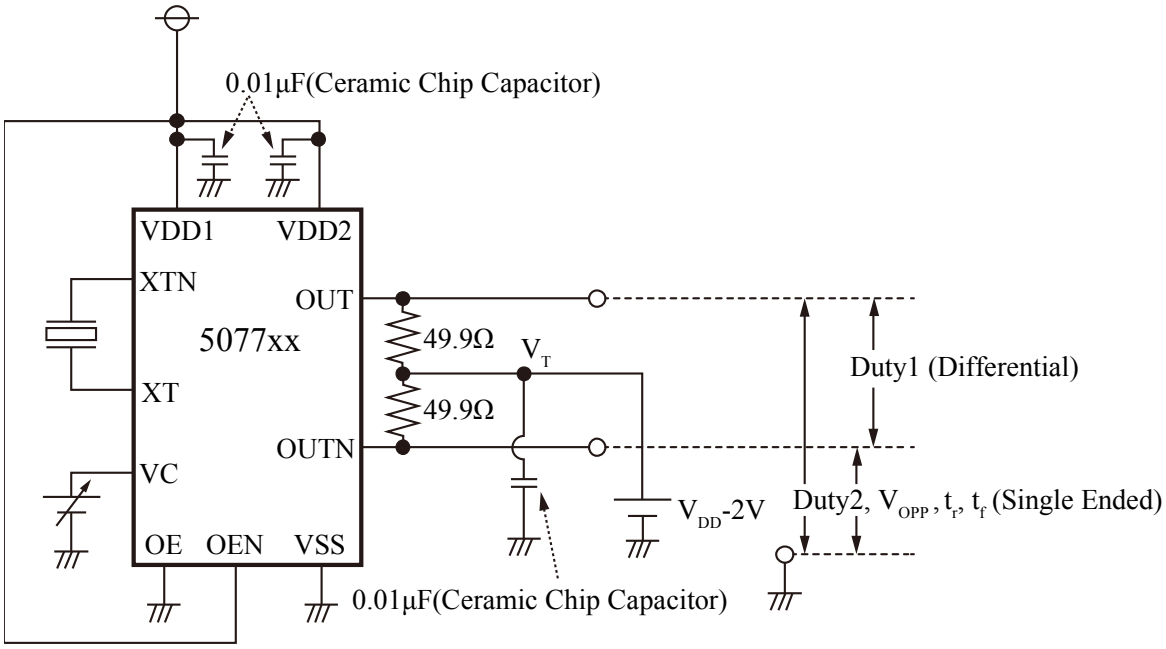
MEASUREMENT CIRCUIT 6

Measurement Parameters: R_{VIN}



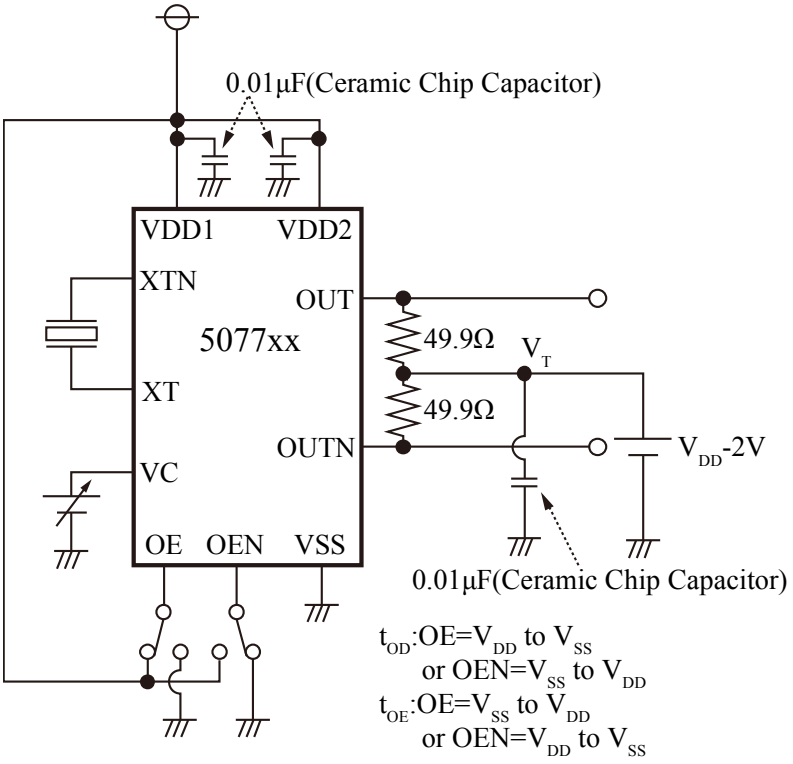
MEASUREMENT CIRCUIT 7

Measurement Parameters: Duty1, Duty2, V_{OPP}, t_r, t_f



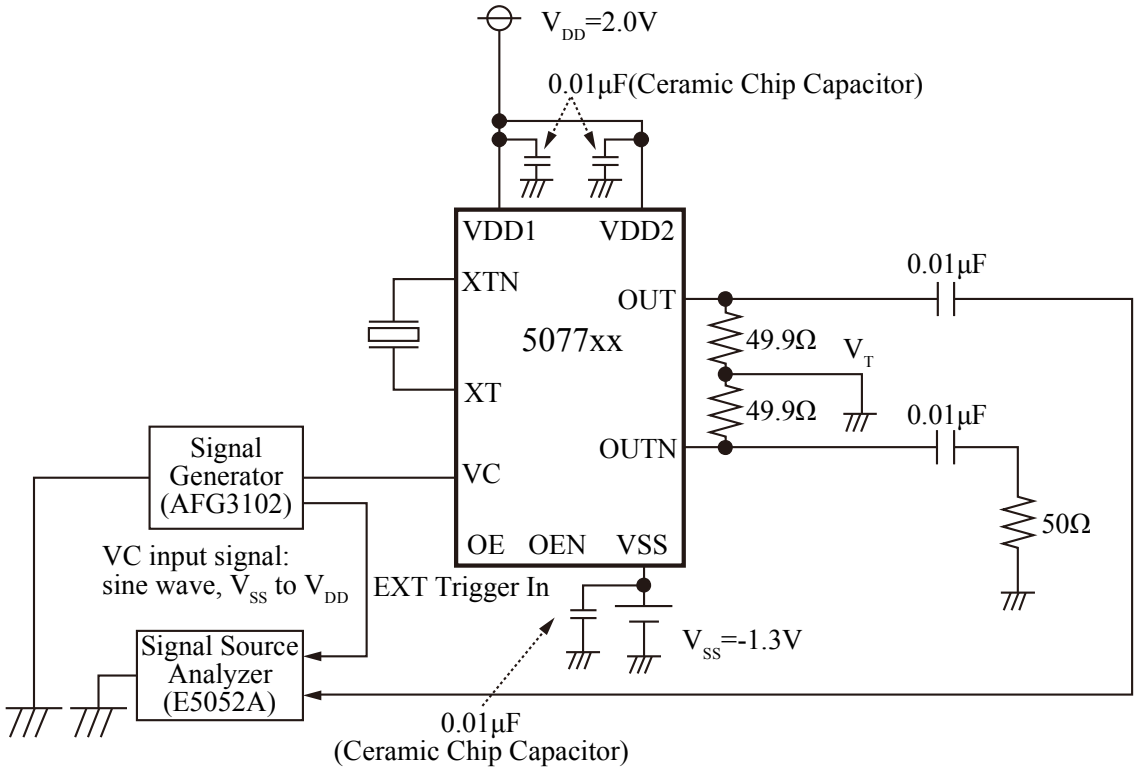
MEASUREMENT CIRCUIT 8

Measurement Parameters: t_{OE}, t_{OD}



MEASUREMENT CIRCUIT 9

Measurement Parameters: F_M



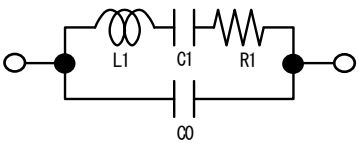
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

Crystal used for measurement

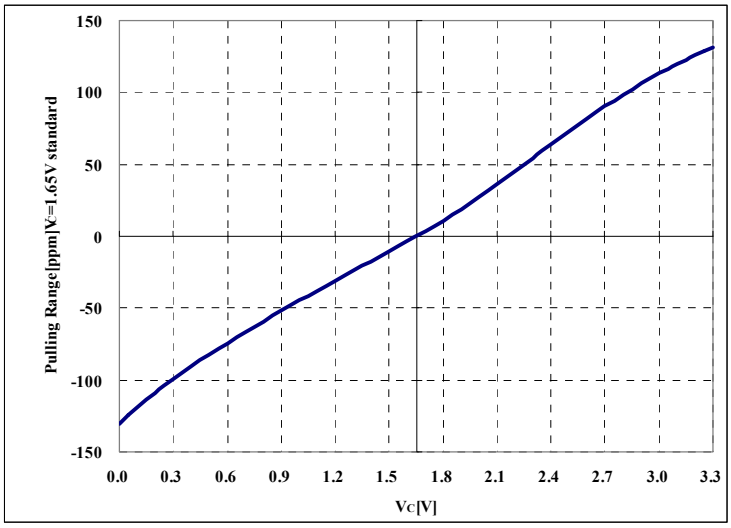
Parameter	A1	B1
f_{OSC}(MHz)	77.76	155.52
C0(pF)	3.0	1.4
γ(=C0/C1)	356	327
R1(Ω)	9.9	11.9

Crystal parameters



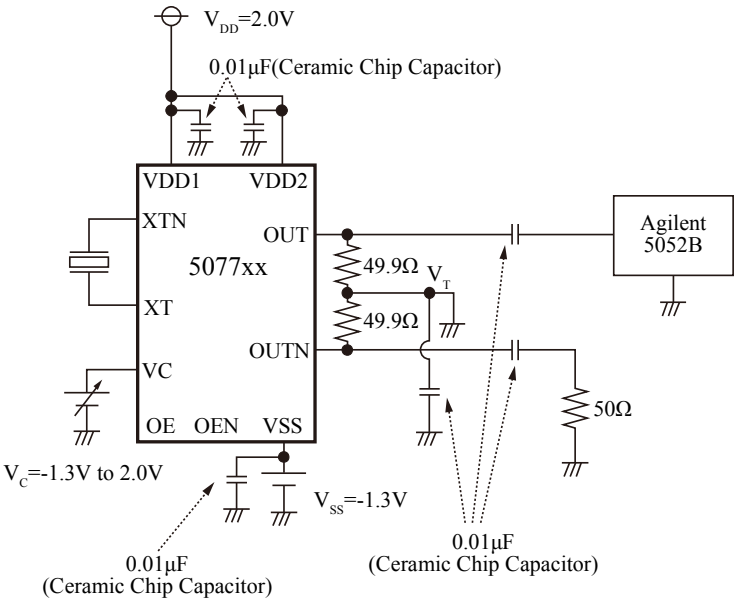
Pulling Range

[5077B1]V_{DD}=2.0V,V_{SS}=-1.3V,T_a=25°C,f_{OSC}=155.52MHz,V_C*1



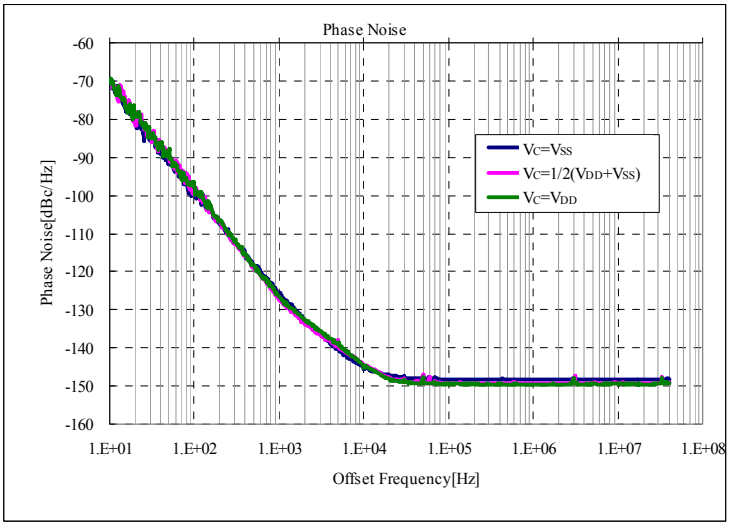
*1: V_C voltage graph adjusted for V_{SS}=0V.

[Measurement circuit diagram]

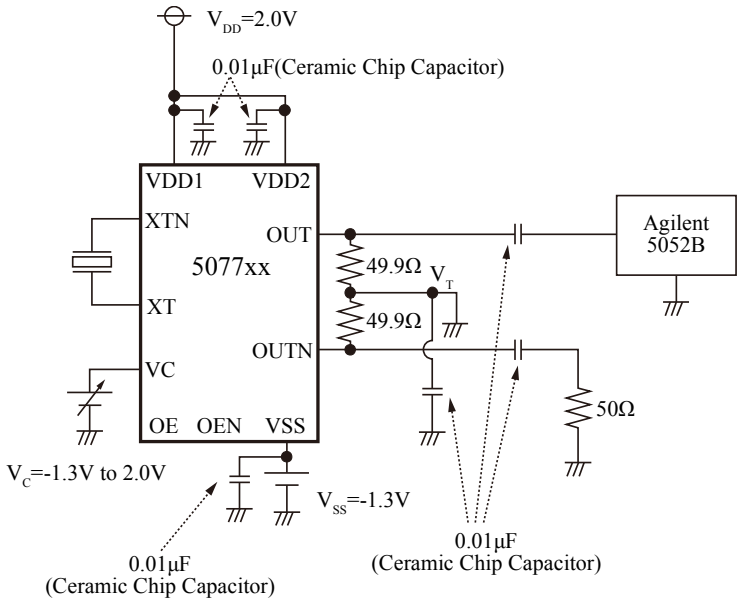


Phase Noise

[5077B1]V_{DD}=2.0V,V_{SS}=-1.3V,T_a=25°C, f_{OSC} =155.52MHz

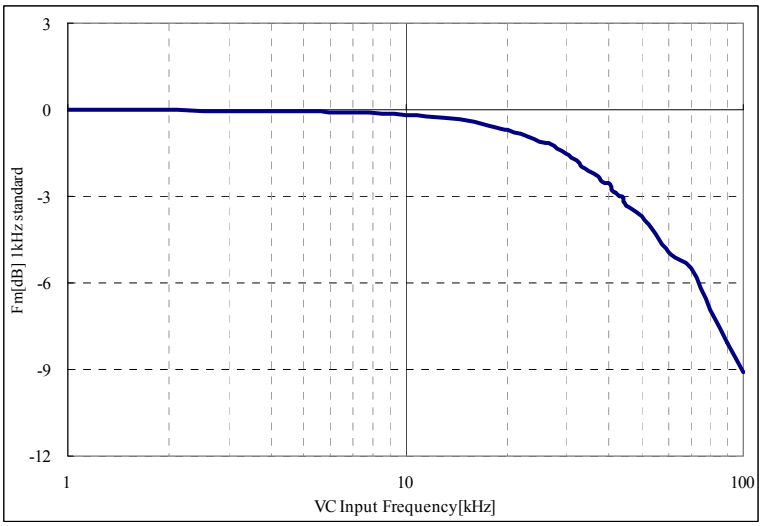


[Measurement circuit diagram]



Modulation Bandwidth

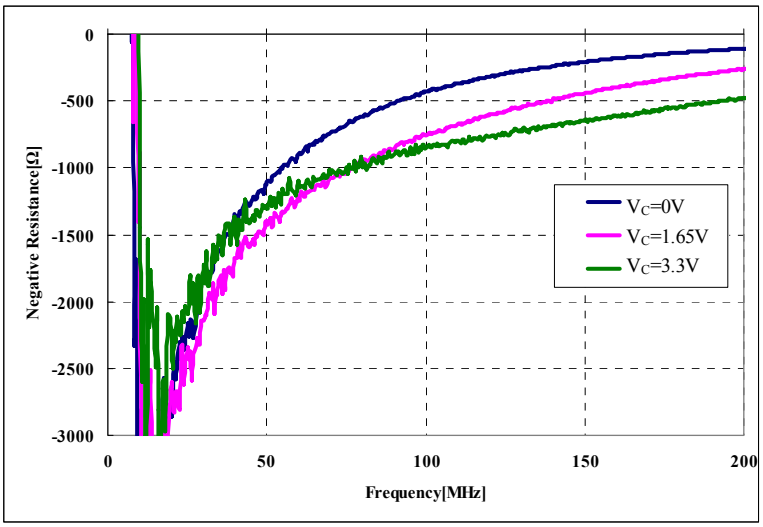
[5077B1]V_{DD}=2.0V,V_{SS}=-1.3V,T_a=25°C, f_{OSC} =155.52MHz



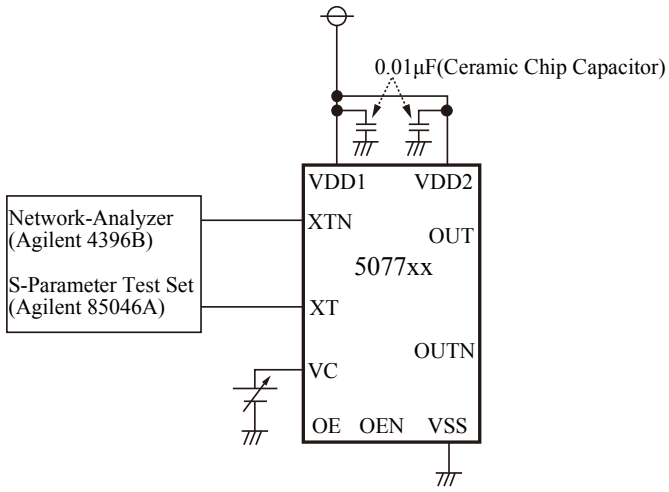
[Measurement circuit diagram] Measurement circuit 9

Negative Resistance

[5077B1]V_{DD}=3.3V,T_a=25°C,C0=0pF



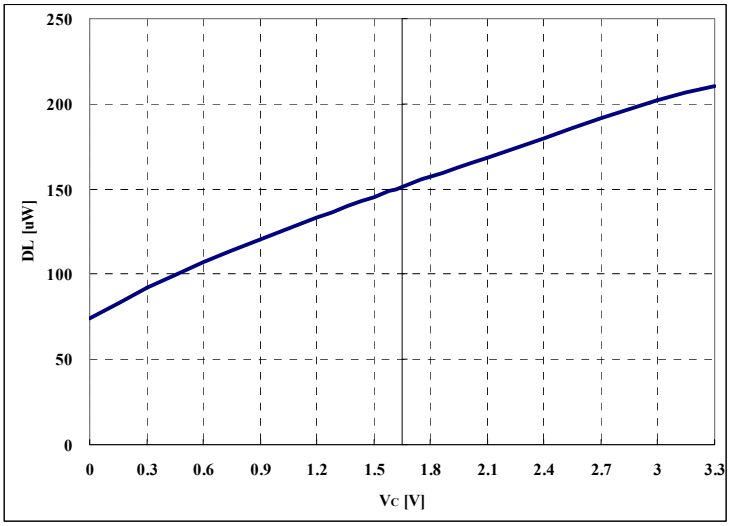
[Measurement circuit diagram]



Measurement results using 4396B Agilent analyzer on NPC test jig. Measurements will vary with test jig and measurement environment.

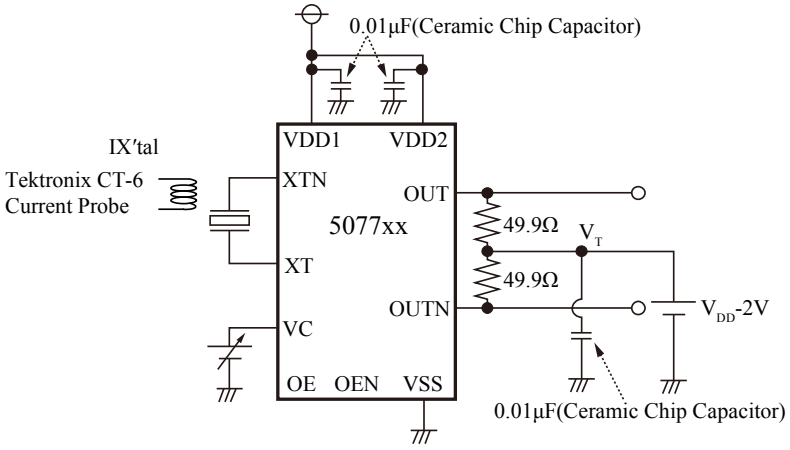
Drive Level

[5077B1]V_{DD}=3.3V,T_a=25°C, f_{OSC}=155.52MHz, V_C *1



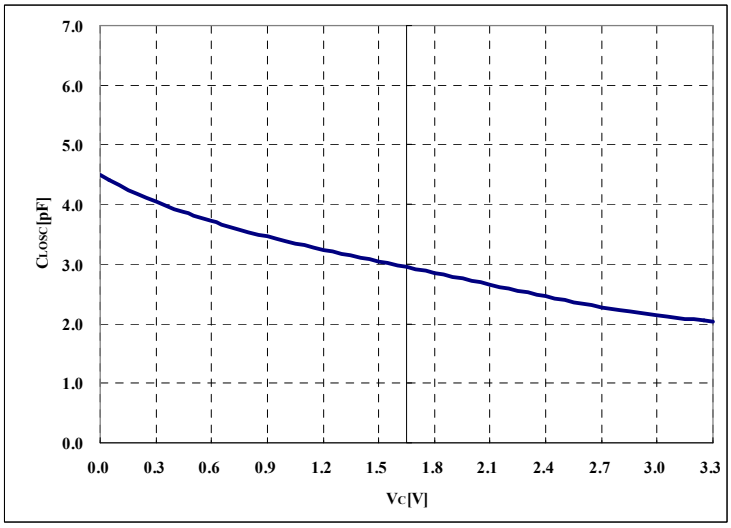
*1: V_C voltage graph adjusted for V_{SS}=0V.

[Measurement circuit diagram]



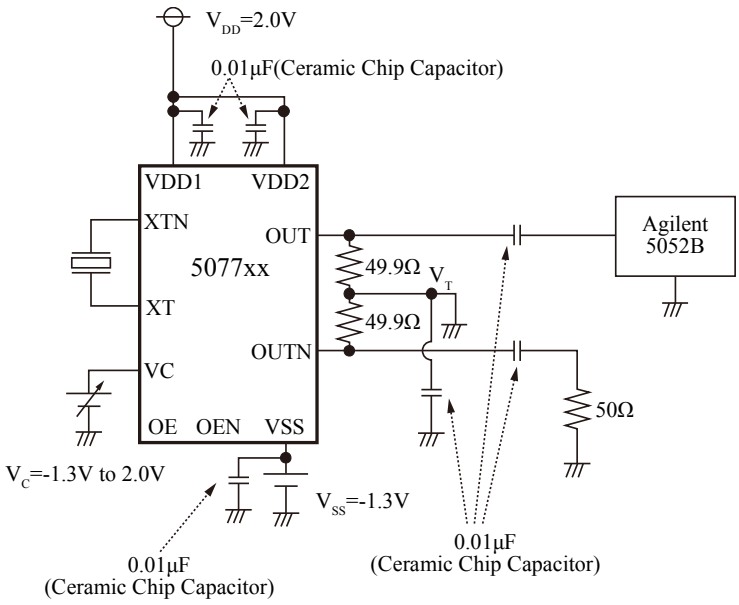
Oscillator CL Characteristics

[5077B1]V_{DD}=2.0V,V_{SS}=-1.3V, T_a=25°C, f_{OSC}=155.52MHz, V_C *1



*1: V_C voltage graph adjusted for V_{SS}=0V.

[Measurement circuit diagram]



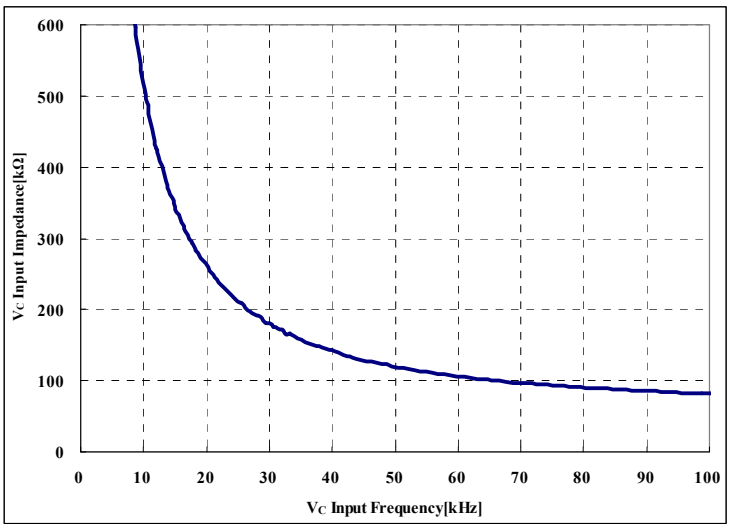
CL_{OSC}: Oscillator circuit equivalent capacitance determined by oscillator frequency

$$CLosc = \frac{C1}{\left(\frac{f_{OSC}}{fs}\right)^2 - 1} - C0$$

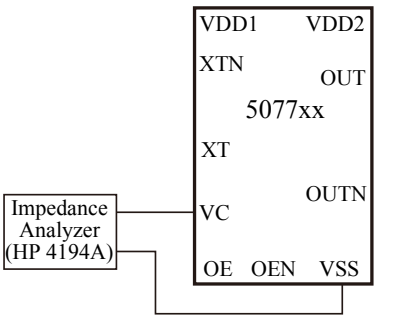
C1: Crystal element equivalent series capacitance
C0: Crystal element equivalent parallel capacitance
fs: Crystal element series resonance frequency

VC Terminal Input Impedance

[5077B1]T_a=25°C,V_C=0V



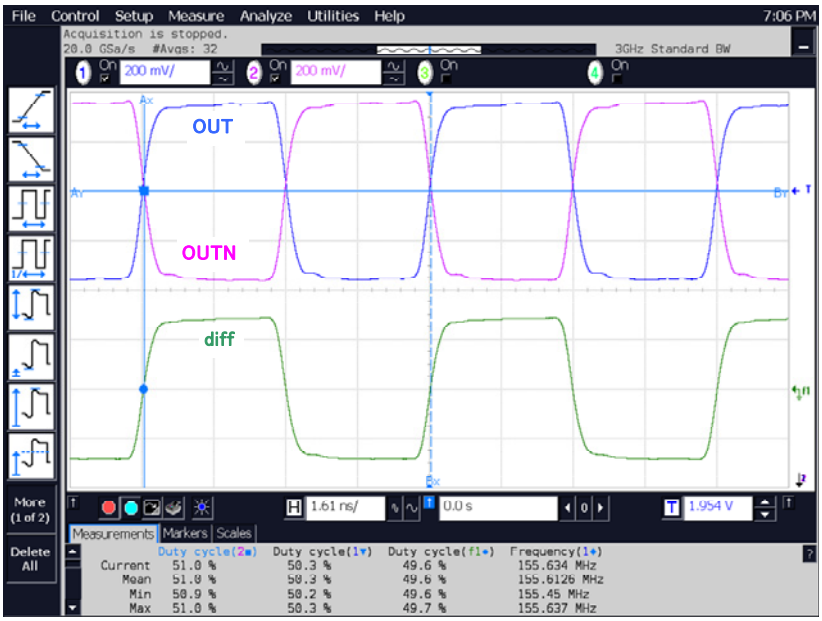
[Measurement circuit diagram]



VC input signal: 1kHz to 100kHz, 0.1V_{P-P}

Output Waveform

[5077B1]V_{DD}=3.3V,V_C=1.65V,T_a=25°C, f_{OSC} =155.52MHz

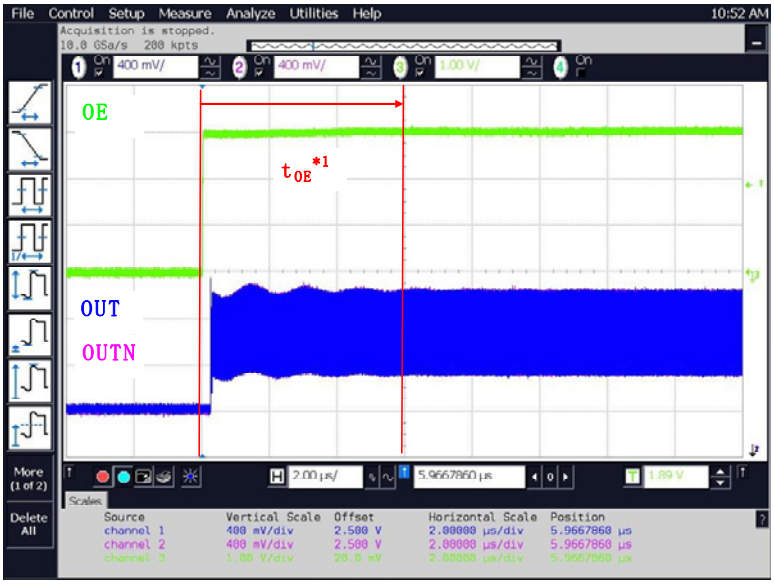


[Measurement circuit diagram] Measurement circuit 7

Measurement equipment: Oscilloscope DSO80604B(Agilent), Differential probe 1134A (Probe head E2678A)

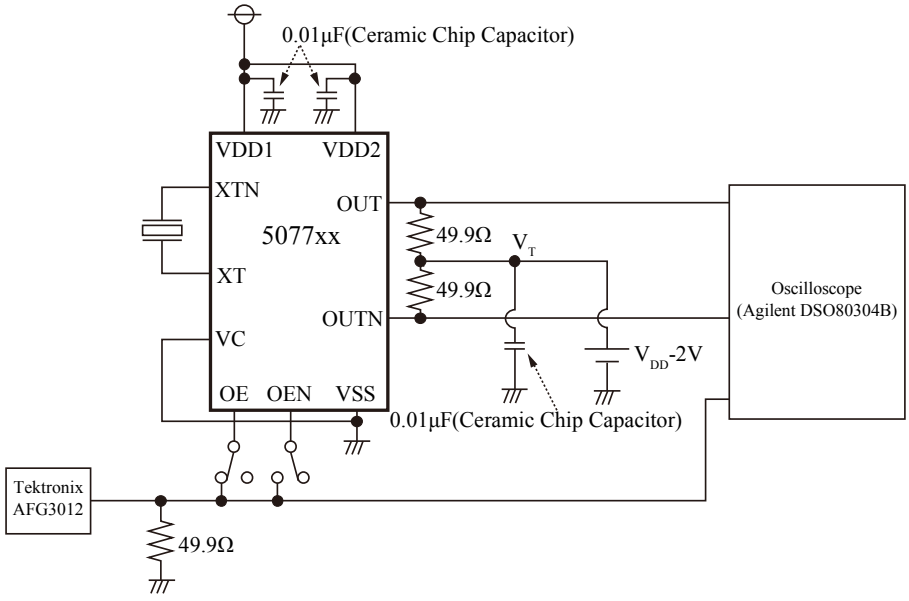
Output Enable Propagation Delay

[5077B1]V_{DD}=3.3V,V_C=1.65V,T_a=25°C, f_{OSC} =155.52MHz



*1: t_{OE} is the time required for the output level to stabilize, and which varies depending on the power supply used, bypass capacitor values, and other factors.
Measurement equipment: Power supply voltage PW18-1.8AQYB(KENWOOD)

[Measurement circuit diagram]



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SEIKO NPC CORPORATION

1-9-9, Hatchobori, Chuo-ku,
Tokyo 104-0032, Japan
Telephone: +81-3-5541-6501
Facsimile: +81-3-5541-6510
http://www.npc.co.jp/
Email:sales@npc.co.jp

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