OVERVIEW

The 5062 series are 2.5V/3.3V operation, HCSL output oscillator ICs. They support 100MHz to 175MHz 3rd overtone oscillation and 25MHz to 175MHz fundamental oscillation. They employ oscillator circuit appropriate for miniature 3rd overtone crystal, making these devices ideal for crystal oscillator modules of miniature package. The 5062 series can be used to construct wide frequency range HCSL output oscillators and low drive level by regulator drive of the oscillator circuit.

FEATURES

- Operating supply voltage range: 2.25 to 3.63V
- Recommended oscillation frequency range (varies with version)
  25MHz to 175MHz fundamental oscillation
  100MHz to 175MHz 3rd overtone oscillation
- -40 to +85°C operating temperature range
- HCSL output
- Oscillation capacitors C_G, C_D built-in
- Standby function
  High impedance in standby mode, oscillator stops
- Power-saving pull-up resistor built-in (OE pin)
- Wafer form (WF5062xx)
- Chip form (CF5062xx)

SERIES CONFIGURATION

Oscillation mode	Recommended oscillation frequency range*1 [MHz]	C_0 cancellation circuit	Recommended C_0 value*2 [pF]	Version name*3
fundamental	25 to 100	No	to 1.5 (to 2.0)*4	(5062L6)
	100 to 175			(5062M6)
3rd overtone fundamental	100 to 140	Yes	1.0 to 2.0 (0.8 to 2.5)*4	5062D6
	140 to 175			5062E6

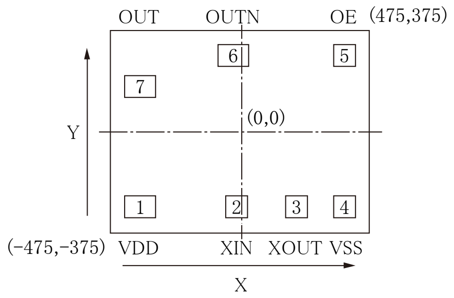
*1. The oscillation frequency is a yardstick value derived from the crystal used for Seiko NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. The oscillator circuit is optimized for 5032 to 3225 size crystal. In use of 7050 size crystal with large C_0 value, because the risk that oscillation margin is insufficient increases, it must be carefully evaluated.
*3. The version name in parentheses is being developed.
*4. Values in ( ) are full range values. If using these ranges, careful evaluation is recommended before implementation.

ORDERING INFORMATION

Device	Package	Version Name
WF5062xx-3	Wafer form	WF5062□□-3 Form WF:Wafer form CF:Chip(Die) form Output frequency 6 : f_0 Oscillation frequency L : 25 to 100MHz M : 100 to 175Hz D : 100 to 140MHz E : 140 to 175MHz
CF5062xx-3	Chip form	

PAD LAYOUT

(Unit: µm)



Chip size: 0.95mm×0.75mm

Chip thickness : 180µm

PAD size : 110µm×80µm (No.1, 6, 7)

80µm×80µm (No.2, 3, 4, 5)

Chip base : Vss level

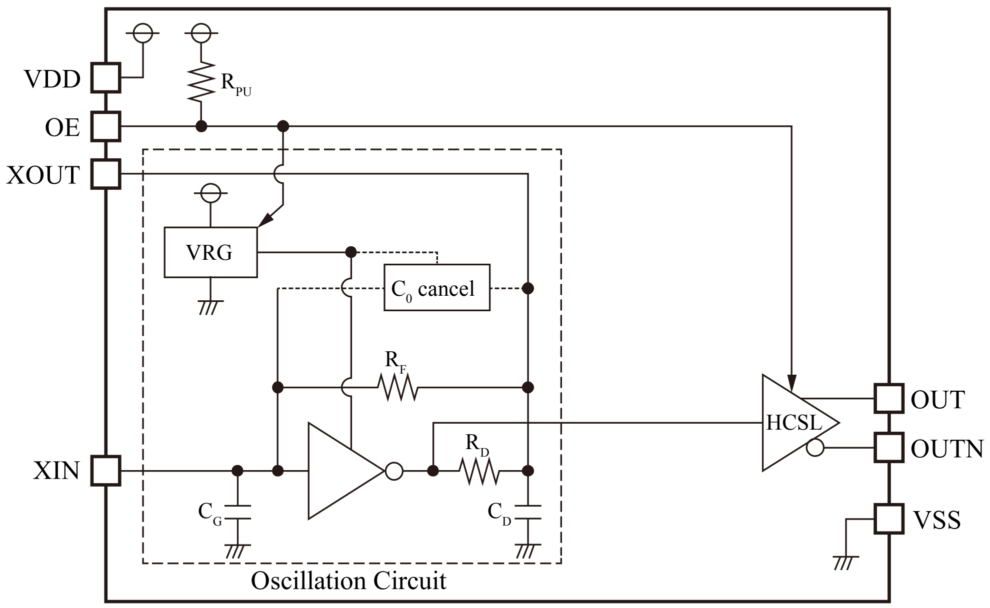
· Coordinates at the chip center are (0,0).

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O*1	Function	PAD coordinates [µm]	
				X	Y
1	VDD	-	(+) supply voltage	-363.7	-283.5
2	XIN	I	Crystal connection pins Crystal is connected between XIN and XOUT.	-11.7	-283.5
3	XOUT	O		208.2	-283.5
4	VSS	-	(-) ground	383.5	-283.5
5	OE	I	Input pin controlled output state (oscillator stops when Low), Power-saving pull-up resistor built-in	383.5	283.5
6	OUTN	O	HCSL output pin (Inverting output)	-29.1	283.5
7	OUT	O	HCSL output pin (Non-inverting output)	-368.5	168.2

*1. I: Input pin O: Output pin

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

Vss=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range*1	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range*1*2	V_{IN}	Input pins	-0.3 to VDD+0.3	V
Output voltage range*1*2	V_{OUT}	Output pins	-0.3 to VDD+0.3	V
Junction temperature*3	T_j		+125	℃
Storage temperature range*4	T_{STG}	Chip form, Wafer form	-55 to +125	℃

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

Vss=0V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillator frequency*1	f_0	5062L6	(25)		(100)	MHz
		5062M6	100		175	
		5062D6	100		140	
		5062E6	140		175	
Output frequency	f_{OUT}	5062L6	(25)		(100)	MHz
		5062M6	100		175	
		5062D6	100		140	
		5062E6	140		175	
Operating supply voltage	V_{DD}	Between VDD and VSS*2	2.25		3.63	V
Input voltage	V_{IN}	Input pins	0		V_{DD}	V
Operating temperature	T_a		-40		+85	℃
Output load	R_L	OUT pin, OUTN pin, Terminated to V_{SS}	49.5		50.5	Ω

Values in parentheses ( ) are temporary.
*1. The oscillation frequency is a yardstick value derived from the crystal used for Seiko NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5062 series. Furthermore, the better characteristic can be obtained by connecting the bypass capacitor of about 10μF. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
DC Characteristics

V_{DD}=2.25 to 3.63V, V_{SS}=0V, T_a= -40 to +85°C unless otherwise noted.

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption (L6 ver.)	I_{DDL}_3.3V	Measurement circuit 1, OE=Open	V_{DD}=3.3V		(31.0)	(39.0)	mA
	I_{DDL}_2.5V	f_0=100MHz	V_{DD}=2.5V		(28.0)	(35.0)	
Current consumption (M6 ver.)	I_{DDM}_3.3V	Measurement circuit 1, OE=Open	V_{DD}=3.3V		35.0	45.0	mA
	I_{DDM}_2.5V	f_0=156.25MHz	V_{DD}=2.5V		31.0	41.0	
Current consumption (D6 ver.)	I_{DDD}_3.3V	Measurement circuit 1, OE=Open	V_{DD}=3.3V		39.0	49.0	mA
	I_{DDD}_2.5V	f_0=125MHz	V_{DD}=2.5V		35.5	45.5	
Current consumption (E6 ver.)	I_{DDE}_3.3V	Measurement circuit 1, OE=Open	V_{DD}=3.3V		40.0	50.0	mA
	I_{DDE}_2.5V	f_0=156.25MHz	V_{DD}=2.5V		36.5	46.5	
Standby current	I_{STB}	Measurement circuit 1, OE=Low				15	μA
High-level output voltage	V_{OH}	Measurement circuit 2 OUT/OUTN pin		0.66		0.85	V
Low-level output voltage	V_{OL}			-0.15		0.15	V
Output leakage current	I_Z	Measurement circuit 3, OE=Low, OUT/OUTN pin				10	μA
High-level input voltage	V_{IH}	Measurement circuit 1, OE pin		$0.7V_{DD}$			V
Low-level input voltage	V_{IL}	Measurement circuit 1, OE pin				$0.3V_{DD}$	V
OE pin pull-up resistance	R_{PU1}	Measurement circuit 1		0.2	1	8	MΩ
	R_{PU2}	Measurement circuit 1		30	70	150	kΩ
Oscillator feedback resistance (L6 ver.)	R_{fL}			50	100	200	kΩ
Oscillator feedback resistance (M6 ver.)	R_{fM}			50	100	200	kΩ
Oscillator feedback resistance (D6 ver.)	R_{fD}			1.1	2.2	3.3	kΩ
Oscillator feedback resistance (E6 ver.)	R_{fE}			1.1	2.2	3.3	kΩ
Oscillator capacitance (L6 ver.)	C_{GL}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		9.6	12.0	14.4	pF
	C_{DL}			11.2	14.0	16.8	
Oscillator capacitance (M6 ver.)	C_{GM}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		1.6	2.0	2.4	pF
	C_{DM}			1.6	2.0	2.4	
Oscillator capacitance (D6 ver.)	C_{GD}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		1.6	2.0	2.4	pF
	C_{DD}			1.6	2.0	2.4	
Oscillator capacitance (E6 ver.)	C_{GE}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		0.8	1.0	1.2	pF
	C_{DE}			0.8	1.0	1.2	

Values in parentheses ( ) are temporary.

AC Characteristics

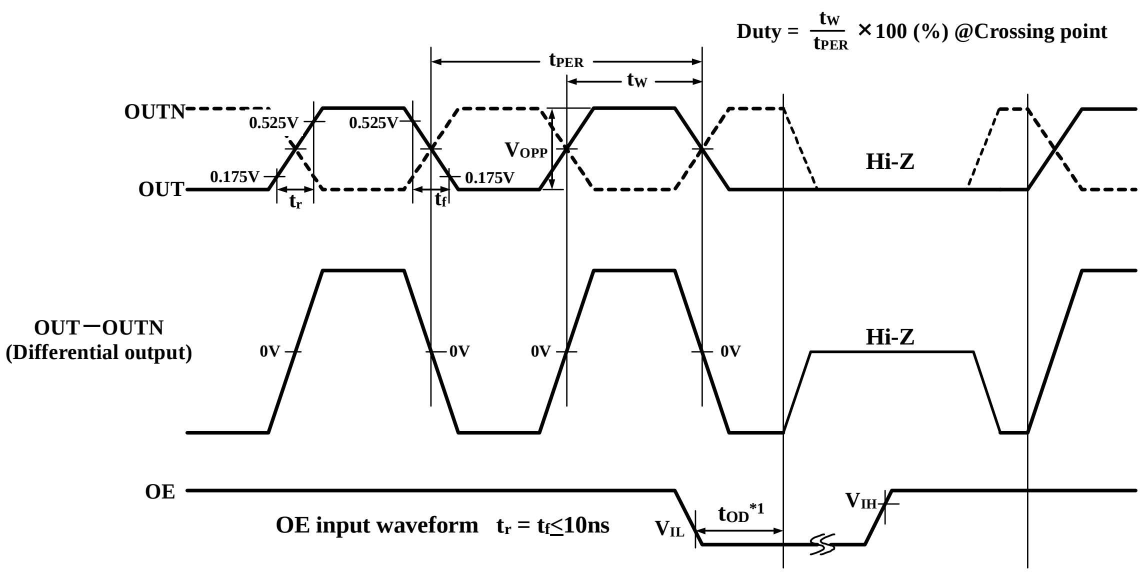
V_{DD} = 2.25 to 3.63V, V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Output duty cycle	Duty	Measurement circuit 4 Measured at differential output signal 0V (crossing point)		45		55	%
Output swing	V_{OPP}	Measurement circuit 4, single-ended output signal		0.4			V
Output rise time	t_r	Measurement circuit 4 Measured at 0.175V to 0.525V single-ended output signal	C_L=0pF (no load)		200	400	ps
			C_L=2pF*1		250	500	
Output fall time	t_f	Measurement circuit 4 Measured at 0.525V to 0.175V single-ended output signal	C_L=0pF (no load)		200	400	ps
			C_L=2pF*1		250	500	
Output disable time	t_{OD}	Measurement circuit 5 Time to becoming output Hi-Z at OE(fall)=V_{IL} (Refer to the timing chart for details.)				200	ns

*1. The parasitic capacitance such as the evaluation boards and packages is included in external load C_L.

Note. The above values are measured by using Seiko NPC standard crystal and jig for evaluation. It must be carefully evaluated so that the values can vary due to crystal characteristics, parasitic component of a mount board and a package.

Timing chart



*1. The OUT/OUTN output goes high impedance after the OE is fallen and then the output disable time "t_{OD}" has elapsed.
The output signal is pulled down to V_{SS} by load resistance.

Figure 1.Timing chart

FUNCTIONAL DESCRIPTION

OE Function

When OE goes Low, OUT/OUTN output is stopped and becomes high impedance.

OE	OUT/OUTN	Oscillator
High or Open	f_0	Operating
Low	Hi-Z	Stopped

Power Saving Pull-up Resistor

The OE pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (High or Low).
When OE is tied to Low level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When OE is left open circuit or tied to High level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of OE becomes High level. Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5062 series have an oscillation detection circuit.
The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by OE.

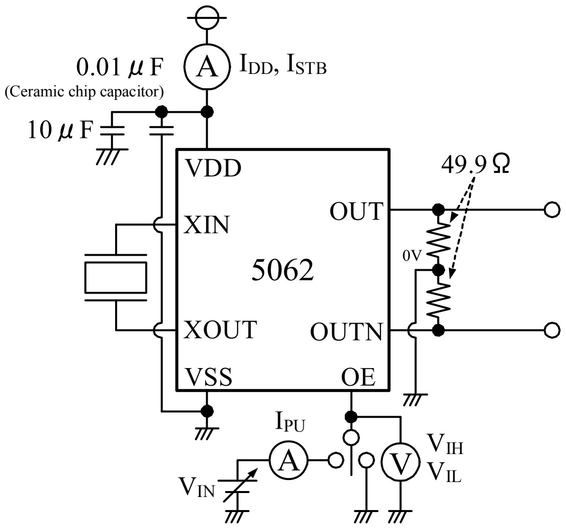
C_0 cancellation circuit

Oscillation circuit with a built-in C_0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C_0. It reduces the C_0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C_0.
This cancellation circuit makes it easier to maintain the oscillation margin.

MEASUREMENT CIRCUITS

MEASUREMENT CIRCUIT 1

Measurement Parameter: I_{DD}, I_{STB}, V_{IH}, V_{IL}, R_{PU1}, R_{PU2}



$$R_{PU1} = \frac{V_{DD}}{I_{PU}} \quad (V_{IN} = 0V)$$

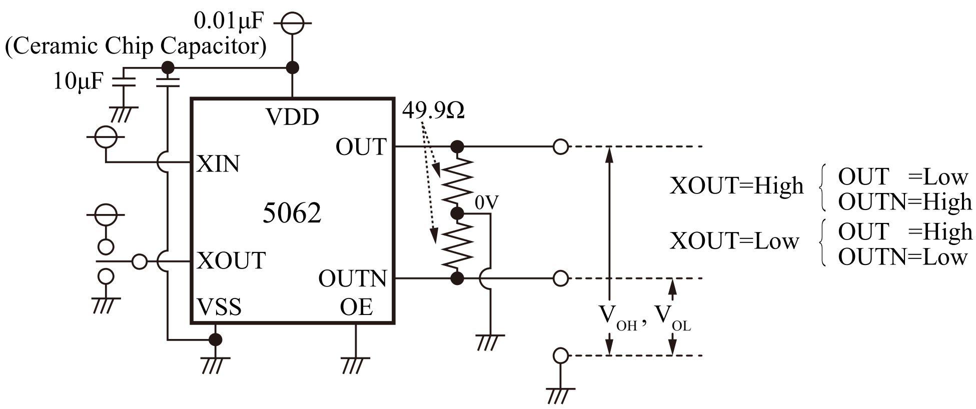
$$R_{PU2} = \frac{V_{DD} - 0.7V_{DD}}{I_{PU}} \quad (V_{IN} = 0.7V_{DD})$$

V_{IH} : $V_{SS} \rightarrow V_{DD}$ voltage that changes output state

V_{IL} : $V_{DD} \rightarrow V_{SS}$ voltage that changes output state

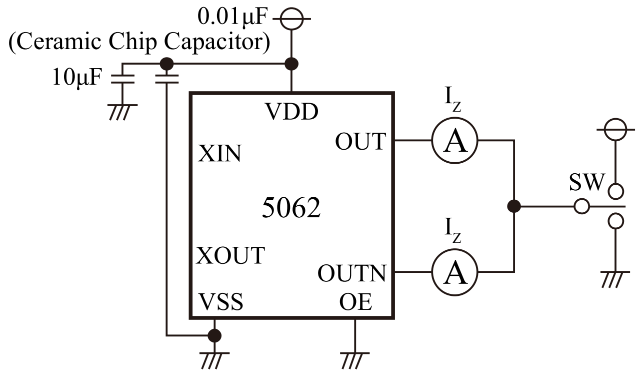
MEASUREMENT CIRCUIT 2

Measurement Parameter: V_{OH}, V_{OL}



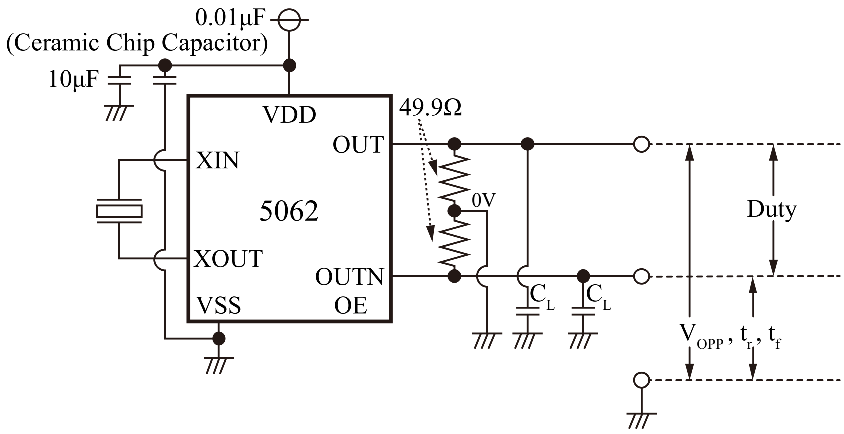
MEASUREMENT CIRCUIT 3

Measurement Parameters: I_Z



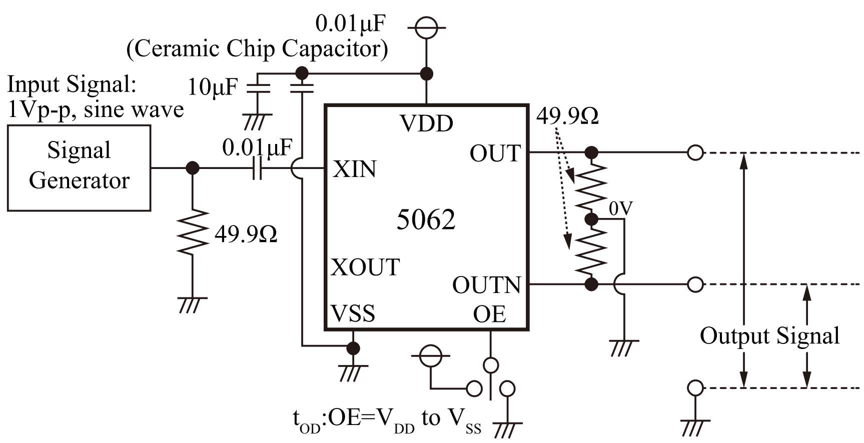
MEASUREMENT CIRCUIT 4

Measurement Parameter: Duty, V_{OPP}, t_r, t_f



MEASUREMENT CIRCUIT 5

Measurement Parameter: t_{OD}



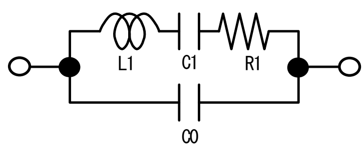
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

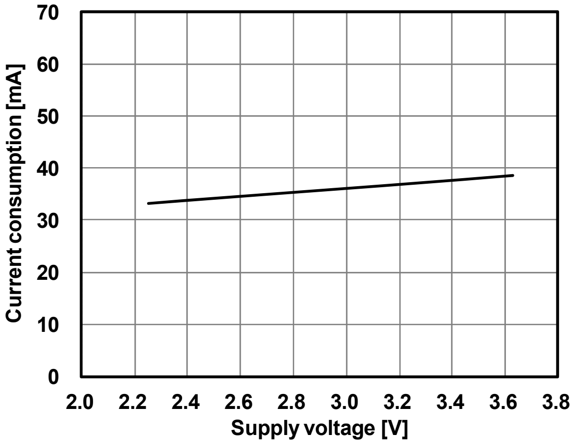
Crystal used for measurement (3rd overtone)

Parameter	f_0=125.00MHz	f_0=156.25MHz
C_0(pF)	1.8	1.2
R_1(Ω)	35	60

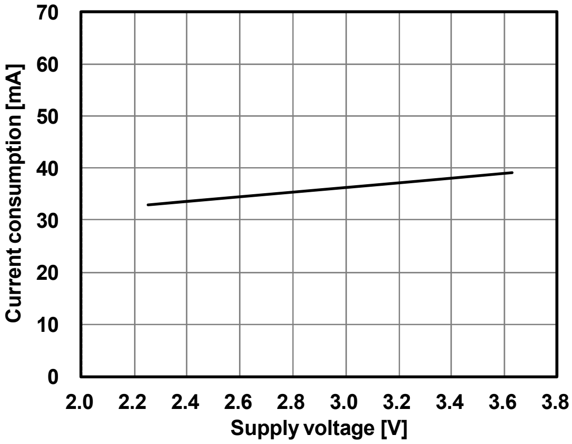
Crystal parameters



Current Consumption

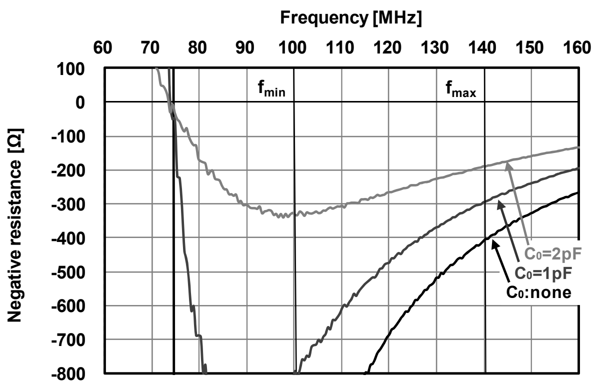


5062D6, f_{OUT}=125MHz, T_a=25°C

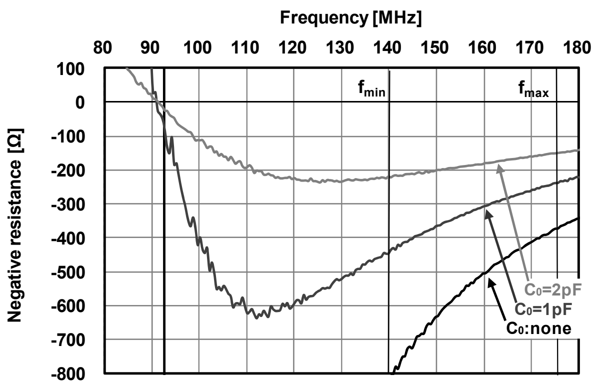


5062E6, f_{OUT}=156.25MHz, T_a=25°C

Negative Resistance



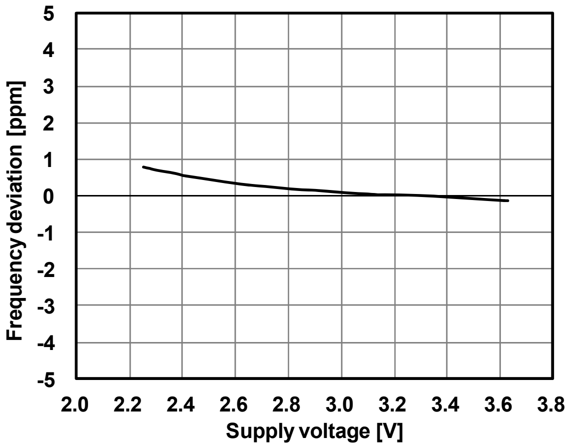
5062D6, T_a=25°C, V_{DD}=3.3V



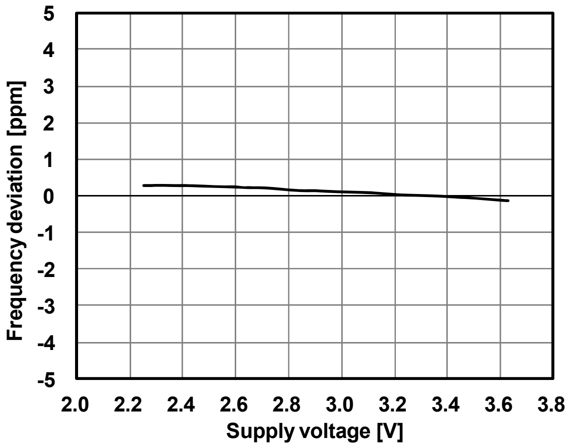
5062E6, T_a=25°C, V_{DD}=3.3V

The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XIN and XOUT pins. They were performed with Agilent 4396B using the NPC test jig.
They may vary in a measurement jig, and measurement environment.

Frequency Deviation by Voltage

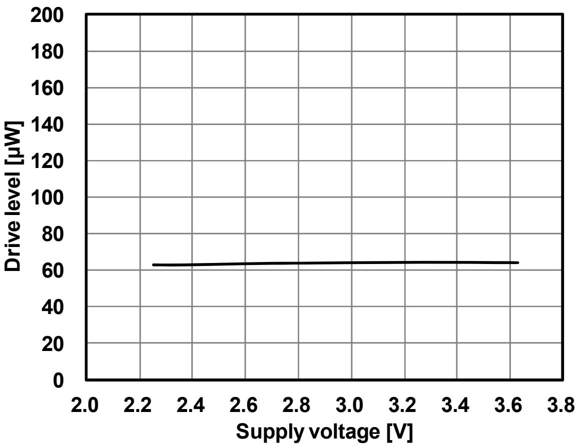


5062D6, f_{OUT}=125MHz, T_a=25°C, 3.3V std.

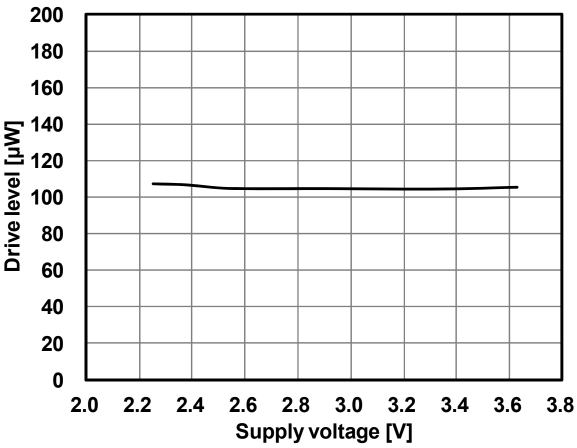


5062E6, f_{OUT}=156.25MHz, T_a=25°C, 3.3V std.

Drive Level

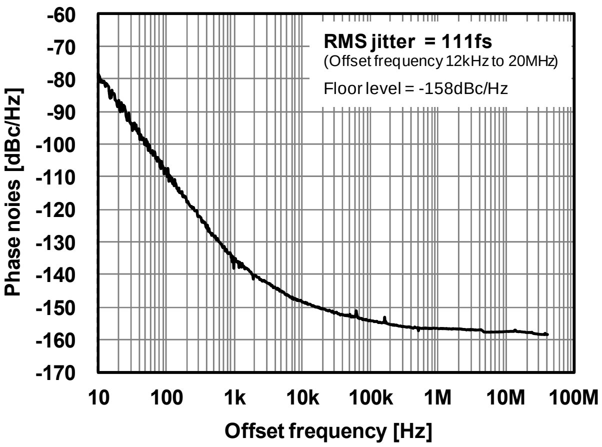


5062D6, f_{OUT}=125MHz, T_a=25°C

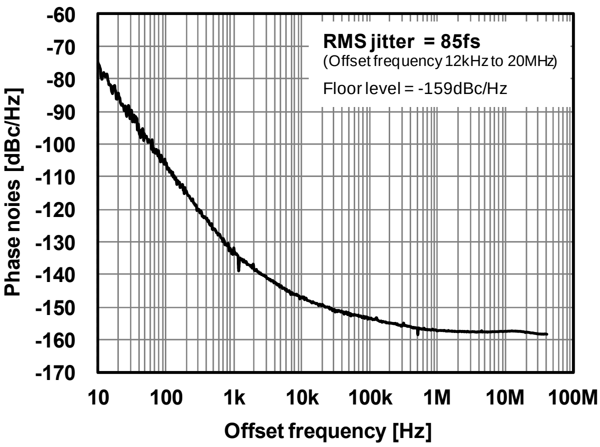


5062E6, f_{OUT}=156.25MHz, T_a=25°C

Phase Noise



5062D6, f_{OUT}=125MHz, T_a=25°C, V_{DD}=3.3V

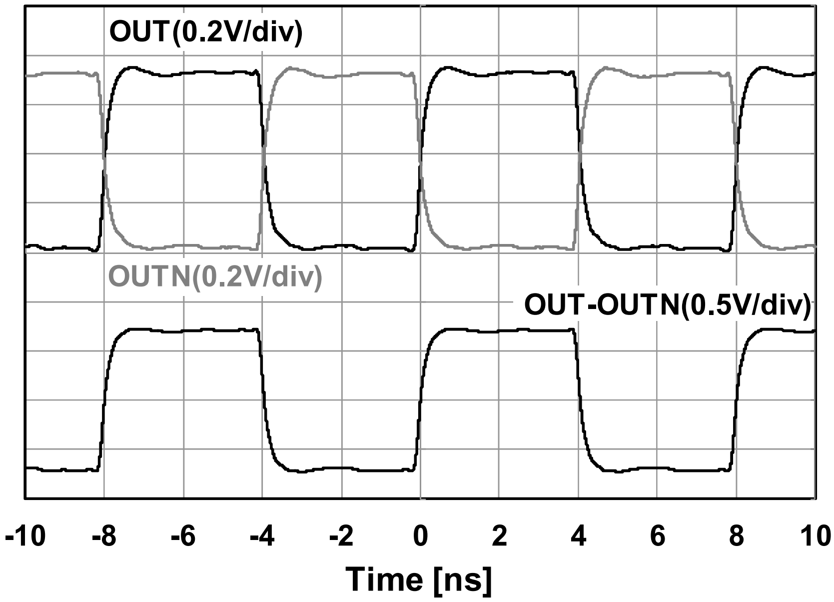


5062E6, f_{OUT}=156.25MHz, T_a=25°C, V_{DD}=3.3V

Measurement instrument: Agilent E5052B Signal Source Analyzer

Output Waveform

• Output load: no load (C_L=0pF)



Duty = 50.6%

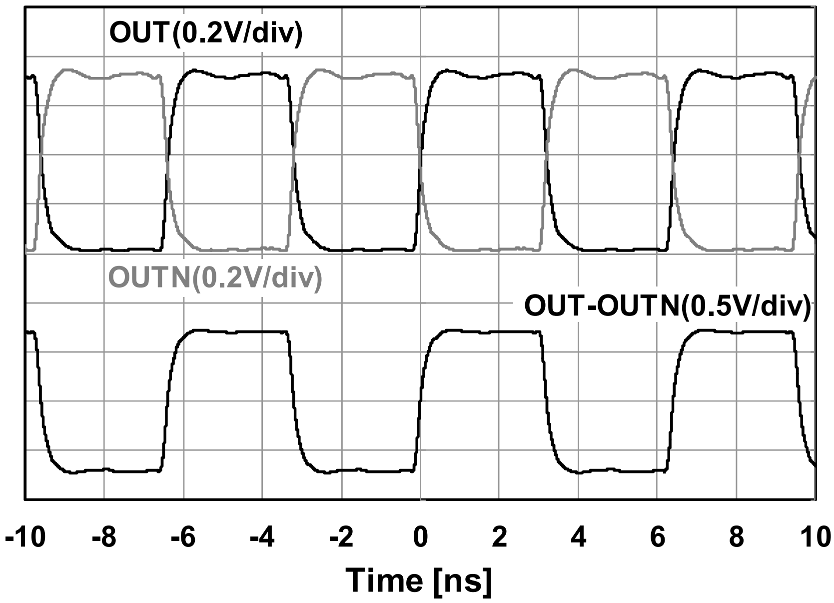
t_r(OUT) = 153ps

t_f(OUT) = 210ps

t_r(OUTN) = 157ps

t_f(OUTN) = 215ps

5062D6, f_{OUT}=125MHz, T_a=25°C, V_{DD}=3.3V, C_L=0pF (no load)



Duty = 49.9%

t_r(OUT) = 164ps

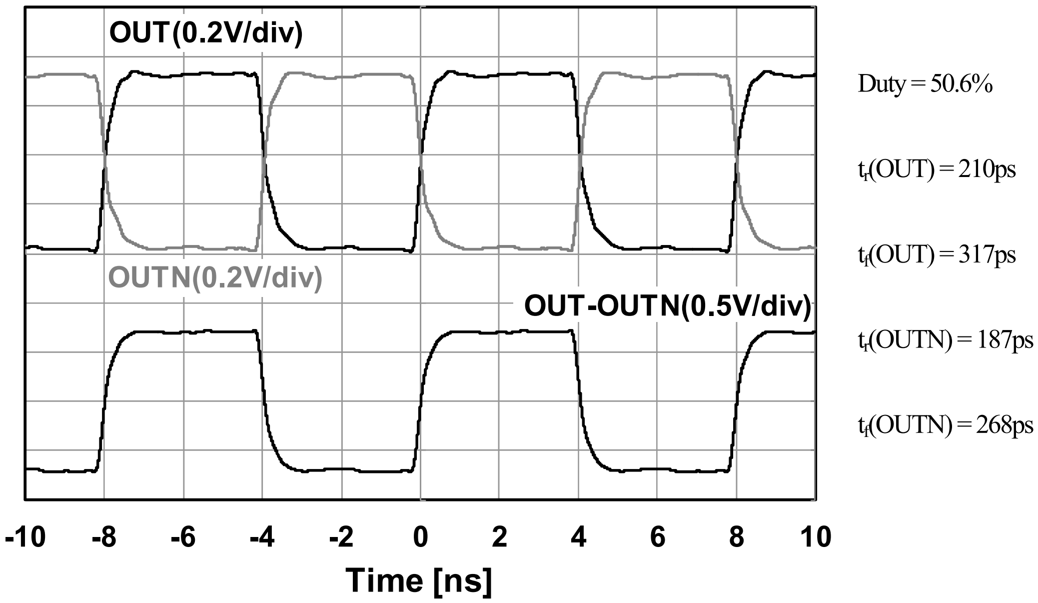
t_f(OUT) = 211ps

t_r(OUTN) = 159ps

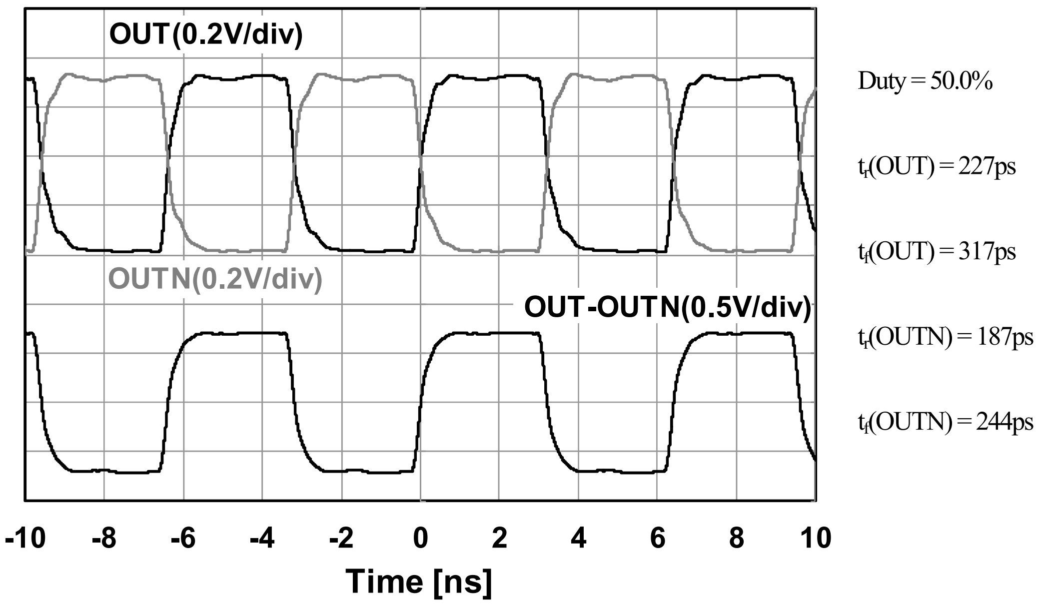
t_f(OUTN) = 208ps

5062E6, f_{OUT}=156.25MHz, T_a=25°C, V_{DD}=3.3V, C_L=0pF (no load)

• Output load: C_L=2pF
Since output waveform may be influenced if load capacitance is added, it must be carefully evaluated.



5062D6, f_{OUT}=125MHz, T_a=25°C, V_{DD}=3.3V, C_L=2pF



5062E6, f_{OUT}=156.25MHz, T_a=25°C, V_{DD}=3.3V, C_L=2pF

Measurement equipment: Oscilloscope DSO80604B (Agilent)
Differential probe 1134A (Agilent)
Probe head E2675A (Agilent)

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