5055A series

Crystal Oscillator Module ICs

OVERVIEW

The 5055A series are miniature crystal oscillator module ICs supported 20MHz to 40MHz fundamental oscillation.

The oscillator circuit stage has voltage regulator drive, significantly reducing current consumption and crystal drive current, compared with existing devices, and significantly reducing the oscillator characteristics supply voltage dependency. The lowest current consumption class in the industry* is realized as the crystal oscillation modules IC of CMOS output. The pad layout is arranged for flip chip mounting, these devices are ideal for miniature crystal oscillators for the applications such as portable equipment requested small size and low consumption current.

FEATURES

- The lowest current consumption class in the industry* (typ)
  Regulated voltage drive oscillator circuit for reduced power consumption and crystal drive current
  0.45mA@40MHz, V_{DD}=1.8V, no load
  0.65mA@40MHz, V_{DD}=2.5V, no load
  1.1mA@40MHz, V_{DD}=3.3V, no load
- Wide range of operating supply voltage: 1.60 to 3.63V
- Recommended oscillation frequency range (fundamental oscillator): 20 to 40MHz
- Optimized low crystal drive current oscillation for miniature crystal units
- Frequency divider built-in
  Selectable by version: f_{OSC}, $f_{OSC}/2$, $f_{OSC}/4$
- Wide output frequency range by multi-stage frequency divider : 5 to 40MHz
- Pad layout optimized for flip chip mounting
- -40 to 85°C operating temperature range
- Standby function
  High impedance in standby mode, oscillator stops
  Power-saving pull-up resistor built-in
- 50±5% output duty ($1/2V_{DD}$)
- ±3mA output drive capability
- 15pF output load capacitance
- Wafer form (WF5055Ax)

*According to our own research as at Nov, 2012

APPLICATIONS

- 3.2mm×2.5mm, 2.5mm×2.0mm, 2.0mm×1.6mm, 1.6mm×1.2mm size miniature crystal oscillator modules

SERIES CONFIGURATION

Version name	Operating supply voltage range [V]	Recommended oscillation frequency range*1 (fundamental) [MHz]	Built-in oscillation capacitance*2 [pF]		Output current [mA]	Output frequency
			C_G	C_D		
5055A1	1.60 to 3.63	20 to 40	2	3	±3	f_{OSC}
5055A2						$f_{OSC}/2$
5055A3						$f_{OSC}/4$

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

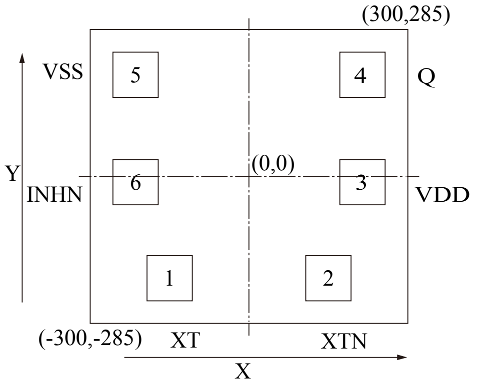
*2. The built-in oscillation capacitors do not contain parasitic capacitance.

ORDERING INFORMATION

Device	Package	Version name
WF5055Ax-4	Wafer form	WF5055A□-4 Form WF : Wafer form Frequency divider function 1: f_{OSC}, 2: $f_{OSC}/2$, 3: $f_{OSC}/4$

PAD LAYOUT

(Unit: µm)



Chip size: 0.60×0.57mm

Wafer thickness: 130µm

PAD size: 80µm

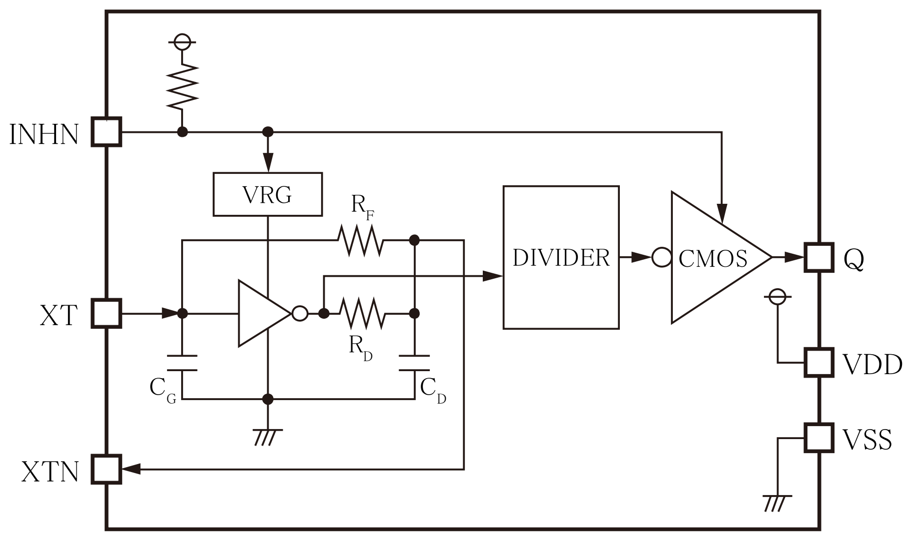
Chip base: V_{SS} level

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O*1	Description	PAD coordinate [µm]	
				X	Y
1	XT	I	Crystal connection pins Crystal is connected between XT and XTN.	-145.2	-193.5
2	XTN	O		145.2	-193.5
3	VDD	-	(+) supply voltage	208.5	-1.1
4	Q	O	Output one of f_{OSC}, $f_{OSC}/2$, $f_{OSC}/4$	208.5	193.5
5	VSS	-	(-) ground	-208.5	193.5
6	INHN	I	Input pin controlled output state (oscillator stops when LOW), power-saving pull-up resistor built-in	-208.5	-1.1

*1. I: Input pin O: Output pin

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range[*1]	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range[*1*2]	V_{IN}	Input pins	-0.3 to V_{DD}+0.3	V
Output voltage range[*1*2]	V_{OUT}	Output pins	-0.3 to V_{DD}+0.3	V
Output current[*3]	I_{OUT}	Q pin	±20	mA
Junction temperature[*3]	T_j		125	°C
Storage temperature range[*4]	T_{STG}	Wafer form	-65 to +125	°C

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Oscillator frequency[*1]	f_{OSC}	V_{DD}=1.60 to 3.63V	20		40	MHz
Output frequency	f_{OUT}	V_{DD}=1.60 to 3.63V, C_{LOUT}≤15pF	5		40	MHz
Operating supply voltage	V_{DD}	Between VDD and VSS[*2]	1.60		3.63	V
Input voltage	V_{IN}	Input pins	V_{SS}		V_{DD}	V
Operating temperature	T_a		-40		+85	°C
Output load capacitance	C_{LOUT}	Q output			15	pF

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5055A series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
DC Characteristics

V_{DD}=1.60 to 3.63V, V_{SS}=0V, T_a= -40 to +85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating MIN	Rating TYP	Rating MAX	Unit
Q pin HIGH-level output voltage	V_{OH}	measurement circuit 3, I_{OH}=-3mA		V_{DD}-0.4		V_{DD}	V
Q pin LOW-level output voltage	V_{OL}	measurement circuit 3, I_{OL}=3mA		0		0.4	V
INHN pin HIGH-level input voltage	V_{IH}	measurement circuit 4		0.7V_{DD}			V
INHN pin LOW-level input voltage	V_{IL}	measurement circuit 4				0.3V_{DD}	V
Q pin Output leakage current	I_Z	measurement circuit 5, INHN="Low"	Q=V_{DD}			10	µA
			Q=V_{SS}	-10			
Current consumption[*1]	I_{DD}	5055A1(f_{OSC}), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=40MHz, f_{OUT}=40MHz	V_{DD}=3.3V		1.1	1.75	mA
			V_{DD}=2.5V		0.65	1.05	
			V_{DD}=1.8V		0.45	0.7	
		5055A2(f_{OSC}/2), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=40MHz, f_{OUT}=20MHz	V_{DD}=3.3V		0.85	1.45	mA
			V_{DD}=2.5V		0.5	0.85	
			V_{DD}=1.8V		0.35	0.6	
		5055A3(f_{OSC}/4), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=40MHz, f_{OUT}=10MHz	V_{DD}=3.3V		0.8	1.35	mA
			V_{DD}=2.5V		0.45	0.8	
			V_{DD}=1.8V		0.3	0.55	
Standby current	I_{ST}	measurement circuit 1, INHN="Low"				10	µA
INHN pin pull-up resistance	R_{PU1}	measurement circuit 6		0.8	3	24	MΩ
	R_{PU2}	measurement circuit 6		30	70	150	kΩ
Oscillator feedback resistance	R_f			50	100	200	kΩ
Oscillator capacitance	C_G	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		1.6	2.0	2.4	pF
	C_D			2.4	3.0	3.6	

*1.The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no load consumption current and f_{OUT} is the output frequency.

$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA] + C_{LOUT}[pF] \times V_{DD}[V] \times f_{OUT}[MHz] \cdot 10^{-3}$

AC Characteristics

V_{DD} = 1.60 to 3.63V, V_{SS} = 0V, T_a = -40 to +85°C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Q pin Output rise time	t_{r1}	measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=2.25 to 3.63V		2.0	6.0	ns
	t_{r2}	measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=1.60 to 2.25V		3.0	8.0	
Q pin Output fall time	t_{f1}	measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=2.25 to 3.63V		2.0	6.0	ns
	t_{f2}	measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=1.60 to 2.25V		3.0	8.0	
Q pin Output duty cycle	DUTY	measurement circuit 1, T_a=25°C, C_{LOUT}=15pF	45	50	55	%
Q pin Output disable delay time	t_{OD}	measurement circuit 2, T_a=25°C, C_{LOUT}≤15pF			200	ns

Timing chart

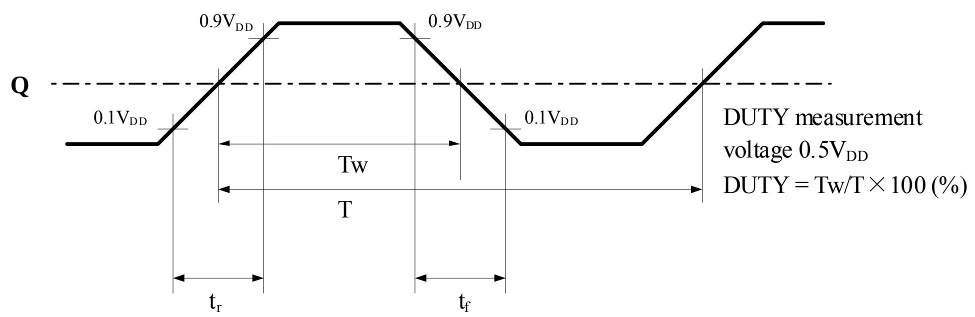
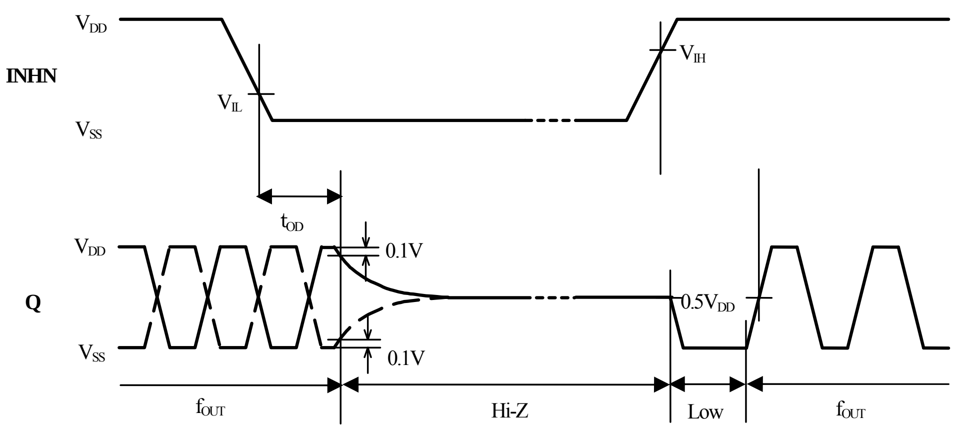


Figure 1. Output switching waveform



When INHN goes HIGH to LOW, the Q output becomes high impedance.

When INHN goes LOW to HIGH, the Q output goes LOW once and then becomes normal output operation after having detected oscillation signals.

Figure 2. Output disable and oscillation start timing chart

FUNCTIONAL DESCRIPTION

INHN Function

Q output is stopped and becomes high impedance.

INHN	Q	Oscillator
HIGH or Open	f_{OUT}	Operating
LOW	Hi-Z	Stopped

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5055A series have an oscillation detection circuit.

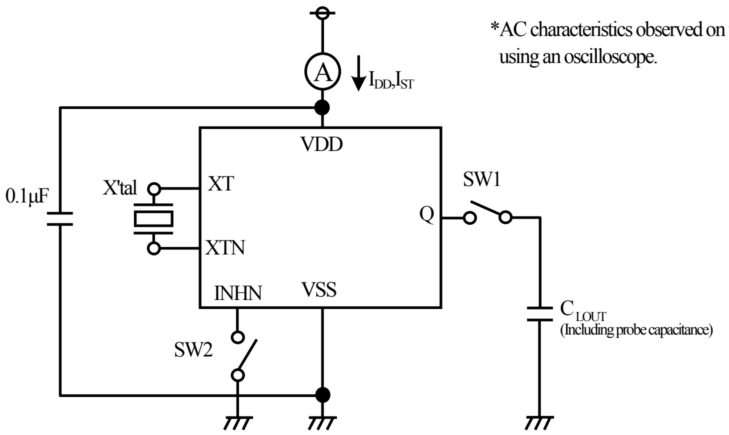
The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

MEASUREMENT CIRCUITS

MEASUREMENT CIRCUIT 1

Measurement Parameter: I_{DD}, I_{ST}, DUTY t_r, t_f

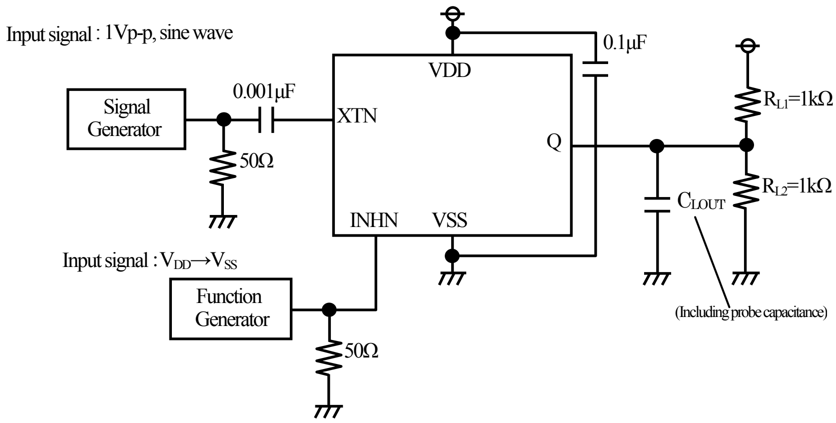
*AC characteristics observed on the Q pin using an oscilloscope.



Parameter	SW1	SW2
I_{DD}	OFF	OFF
I_{ST}	ON or OFF	ON
DUTY, t_r, t_f	ON	OFF

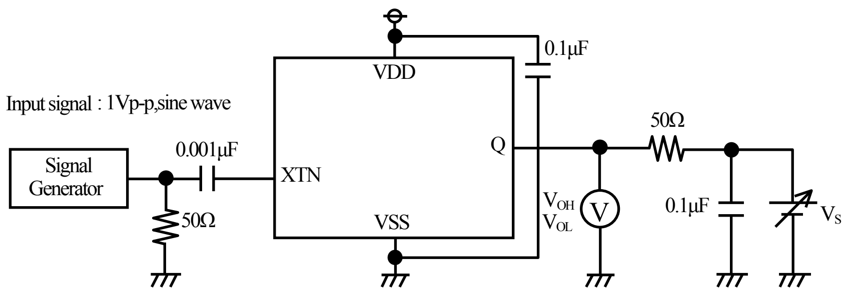
MEASUREMENT CIRCUIT 2

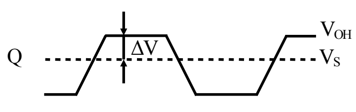
Measurement Parameter: t_{OD}



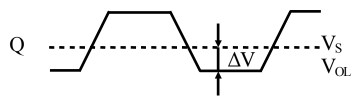
MEASUREMENT CIRCUIT 3

Measurement Parameter: V_{OH} , V_{OL}





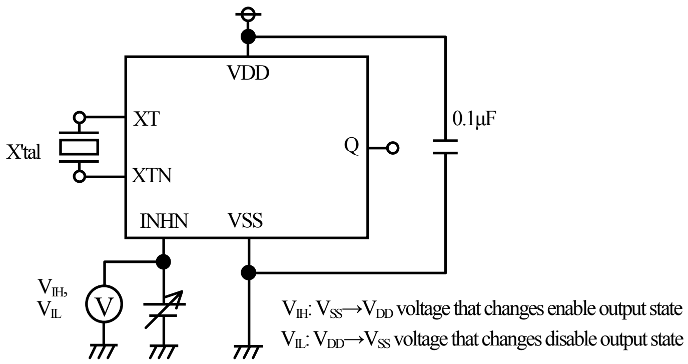
V_S adjusted so that $\Delta V=50\times I_{OH}$



V_S adjusted so that $\Delta V=50\times I_{OL}$

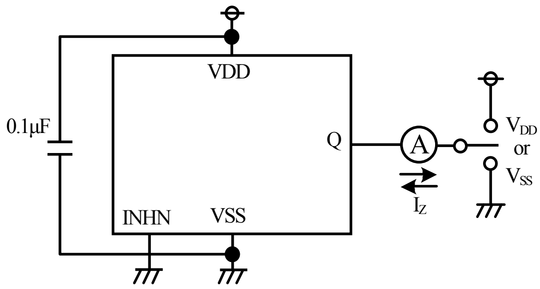
MEASUREMENT CIRCUIT 4

Measurement Parameter: V_{IH}, V_{IL}



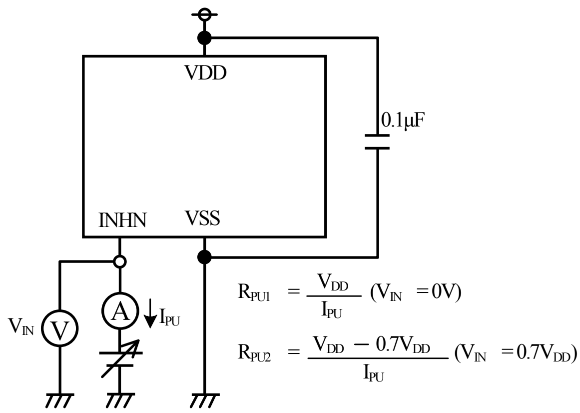
MEASUREMENT CIRCUIT 5

Measurement Parameter: I_Z



MEASUREMENT CIRCUIT 6

Measurement Parameter: R_{PU1}, R_{PU2}



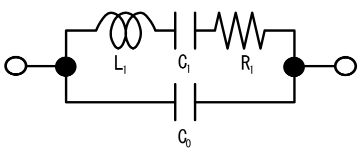
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

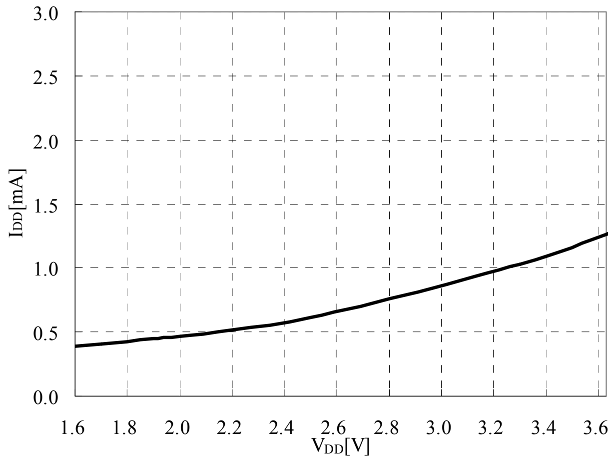
Crystal used for measurement

Parameter	27MHz	40MHz
C_0(pF)	1.7	1.4
R_1(Ω)	8	8

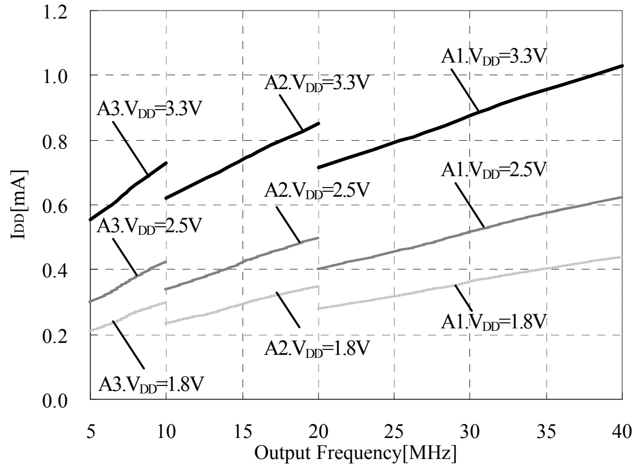
Crystal parameters



Current Consumption

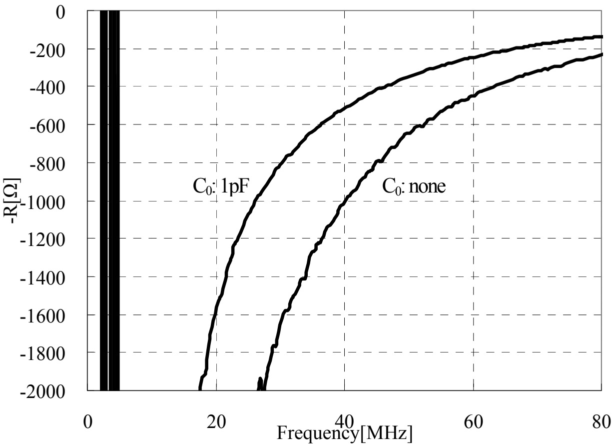


5055A1, f_{OSC}=40MHz, T_a: Room temperature, C_{LOUT}: none

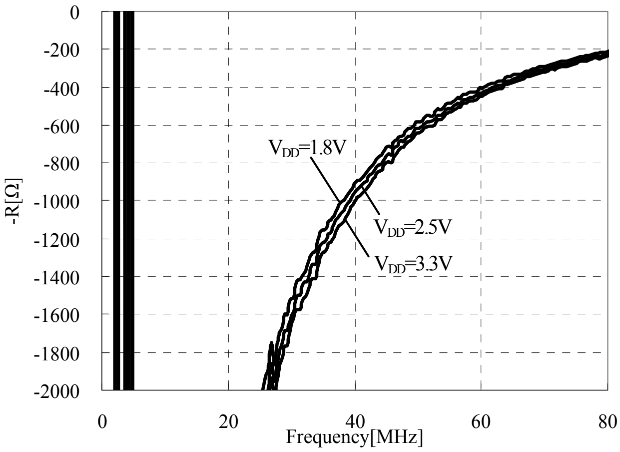


5055Ax, T_a: Room temperature, C_{LOUT}: none

Negative Resistance



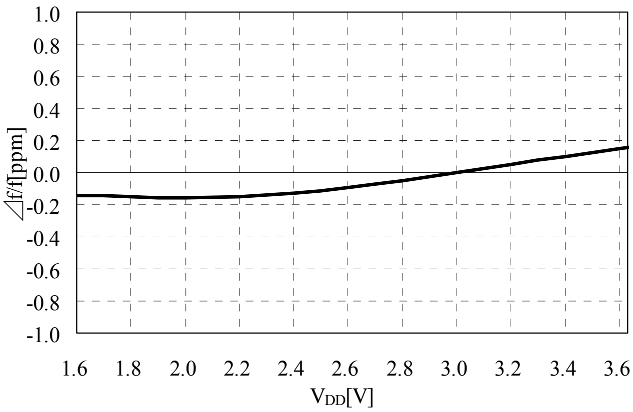
5055A1, V_{DD}=3.3V, T_a: Room temperature
Measurement equipment: Agilent Impedance analyzer 4396B



5055A1, T_a: Room temperature, C_0: none

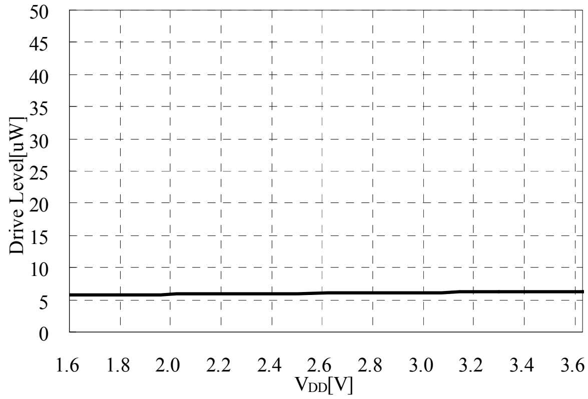
The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XT and XTN pins.
They were performed with Agilent 4396B using the NPC test jig.
They may vary in a measurement jig, and measurement environment.

Frequency Deviation by Voltage



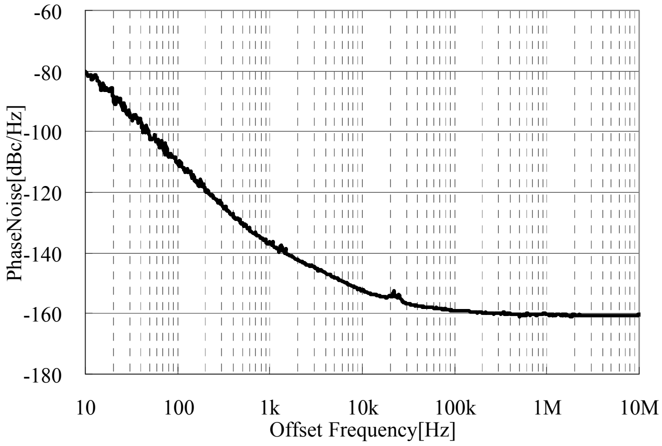
5055A1, f_{OSC}=40MHz, T_a: Room temperature, 3.0V std

Drive Level



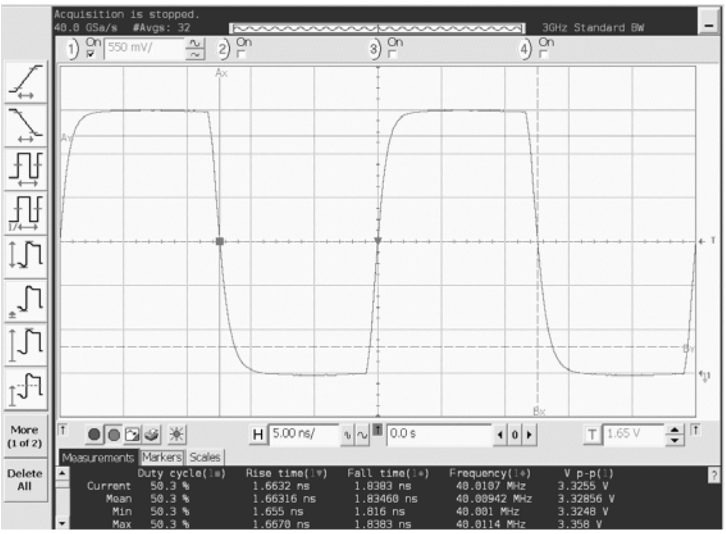
5055A1, f_{OSC}=40MHz, T_a: Room temperature

Phase Noise



5055A1, f_{OSC}=40MHz, V_{DD}=3.3V, T_a: Room temperature
Measurement equipment: Signal Source Analyzer Agilent E5052B

Output Waveform



5055A1 version, V_{DD}=3.3V, f_{OUT}=40MHz, C_{LOUT}=15pF, T_a: Room temperature
Measurement equipment: Oscilloscope Agilent DSO80604B

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