

### OVERVIEW

The 5053 series are miniature crystal oscillator module ICs supported 80MHz to 170MHz fundamental oscillation mode.

The Oscillator circuit stage has voltage regulator drive, significantly reducing current consumption and crystal current, compared with existing devices, and significantly reducing the oscillator characteristics supply voltage dependency.

There are 3 pad layout package options available for optimized mounting, making these devices ideal for miniature crystal oscillators.

### FEATURES

- Wide range of operating supply voltage: 1.60 to 3.63V
- Regulated voltage drive oscillator circuit for reduced power consumption and crystal drive current
- Optimized low crystal drive current oscillation for miniature crystal units
- 3 pad layout options for mounting
  - 5053Ax: for Flip Chip Bonding
  - 5053Bx: for Wire Bonding (Type I)
  - 5053Cx: for Wire Bonding (Type II)
- Recommended oscillation frequency range (fundamental oscillator): 80 to 133MHz (x1 ver.)  
100 to 170MHz (xP ver.)
- -40 to 105°C operating temperature range
- Standby function
  - High impedance in standby mode, oscillator stops
- CMOS output
- 50±5% output duty (1/2V<sub>DD</sub>)
- ±8mA output drive capability
- 15pF output load capacitance
- Wafer form (WF5053xx)
- Chip form (CF5053xx)

### APPLICATIONS

- 3.2×2.5, 2.5×2.0, 2.0×1.6 size miniature crystal oscillator modules

### SERIES CONFIGURATION

Version <sup>*1*2</sup>	Operating supply voltage range [V]	Recommended oscillation frequency range <sup>*3</sup> [MHz]	C0 cancellation circuit / Recommended C0 value [pF]	PAD layout
(5053A1)	1.60 to 3.63	80 to 133	Yes/1 to 2	Flip Chip Bonding
(5053B1)				Wire Bonding Type I
5053C1				Wire Bonding Type II
(5053AP)	2.25 to 3.63	100 to 170	Yes/1 to 2	Flip Chip Bonding
(5053BP)				Wire Bonding Type I
5053CP				Wire Bonding Type II

\*1. The version name in parentheses is being developed.

\*2. It becomes WF5053xx in case of the wafer form and CF5053xx in case of the chip form.

\*3. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

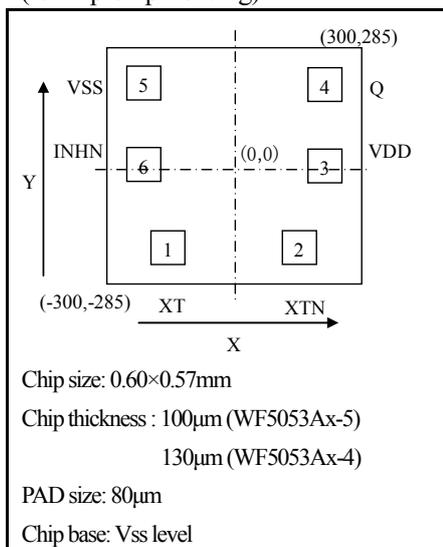
### ORDERING INFORMATION

Device	Package	Version name
WF5053xx-x	Wafer form	WF5053□□-□ Form WF : Wafer form CF : Chip(Die) form Chip thickness 5: 100μm 4: 130μm Oscillation frequency range PAD layout (A: for Flip Chip Bonding) <sup>*1</sup> (B: for Wire Bonding (Type I)) <sup>*1</sup> C: for Wire Bonding (Type II) *1. 5053Ax, Bx are under development.
CF5053xx-x	Chip form	

### PAD LAYOUT

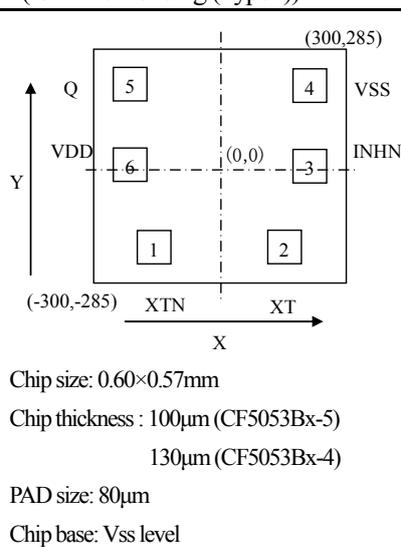
▪ WF5053Ax

(for Flip Chip Bonding)



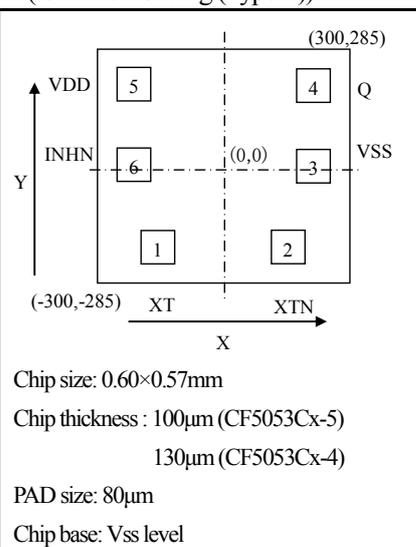
▪ CF5053Bx

(for Wire Bonding (Type I))



▪ CF5053Cx

(for Wire Bonding (Type II))



· Coordinates at the chip center are (0,0). The chip size is the value measured between scribe line centers.

### PAD COORDINATES

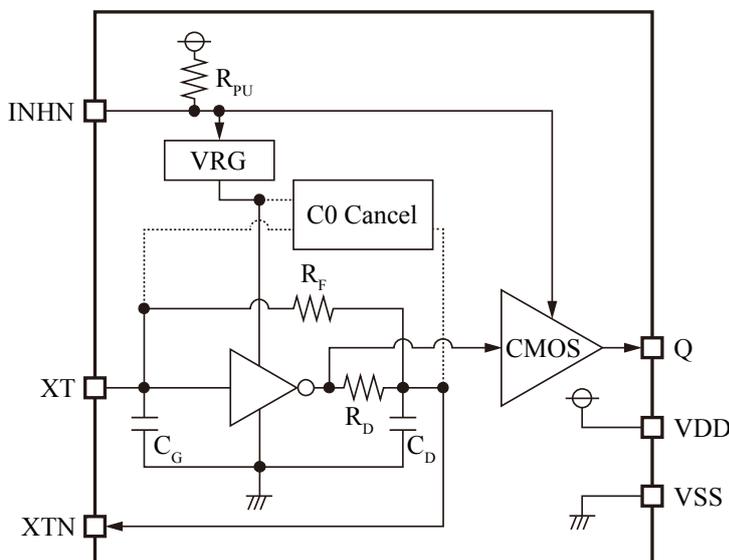
PAD No.	PAD coordinates[μm]	
	X	Y
1	-145.2	-193.5
2	145.2	-193.5
3	208.5	-1.1
4	208.5	193.5
5	-208.5	193.5
6	-208.5	-1.1

### PIN DESCRIPTION

PAD No.	Pin	Function		
			(5053Ax)*1	(5053Bx)*1
1	2	1	XT	Crystal connection pins. Crystal is connected between XT and XTN.
2	1	2	XTN	
3	6	5	VDD	(+) supply voltage
4	5	4	Q	Output pin
5	4	3	VSS	(-) ground
6	3	6	INH	Input pin controlled output state (oscillator stops when LOW), Power-saving pull-up resistor built-in

\*1. 5053Ax, Bx are under development.

### BLOCK DIAGRAM



## SPECIFICATIONS

### Absolute Maximum Ratings

 $V_{SS}=0V$ 

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range <sup>*1</sup>	$V_{DD}$	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range <sup>*1*2</sup>	$V_{IN}$	Input pins	-0.3 to $V_{DD}+0.3$	V
Output voltage range <sup>*1*2</sup>	$V_{OUT}$	Output pins	-0.3 to $V_{DD}+0.3$	V
Output current <sup>*3</sup>	$I_{OUT}$	Q pin	$\pm 20$	mA
Junction temperature <sup>*3</sup>	$T_j$		150	°C
Storage temperature range <sup>*4</sup>	$T_{STG}$	Chip form, Wafer form	-55 to +150	°C

\*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded.

Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

\*2.  $V_{DD}$  is a  $V_{DD}$  value of recommended operating conditions.

\*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

\*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

### Recommended Operating Conditions

 $V_{SS}=0V$ 

Parameter	Symbol	Condition	Rating			Unit	
			MIN	TYP	MAX		
Oscillator frequency <sup>*1</sup>	$f_{OSC}$	$V_{DD}=1.60$ to $3.63V$	5053x1 ver.	80	-	133	MHz
		$V_{DD}=2.25$ to $3.63V$	5053xP ver.	100		170	
Output frequency	$f_{OUT}$	$V_{DD}=1.60$ to $3.63V$ , $C_L \leq 15pF$	5053x1 ver.	80	-	133	MHz
		$V_{DD}=2.25$ to $3.63V$ , $C_L \leq 15pF$	5053xP ver.	100		170	
Operating supply voltage	$V_{DD}$	Between VDD and VSS <sup>*2</sup>	5053x1 ver.	1.60	-	3.63	V
			5053xP ver.	2.25			
Input voltage	$V_{IN}$	Input pins	$V_{SS}$	-	-	$V_{DD}$	V
Operating temperature	$T_a$		-40	-	-	+105	°C
Output load capacitance	$C_L$	Q output	-	-	-	15	pF

\*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

\*2. Mount a ceramic chip capacitor that is larger than  $0.01\mu F$  proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5053 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

## Electrical Characteristics

## DC Characteristics

$V_{DD}=1.60$  to  $3.63$  V,  $V_{SS}=0$  V,  $T_a=-40$  to  $+105^\circ\text{C}$  unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	
			MIN	TYP	MAX		
HIGH-level output voltage	$V_{OH}$	Q pin, measurement circuit 3, $I_{OH}=-8\text{mA}$ $T_a=-40$ to $+85^\circ\text{C}$	$V_{DD}$ -0.4	-	$V_{DD}$	V	
		Q pin, measurement circuit 3, $I_{OH}=-8\text{mA}$	$V_{DD}$ -0.45	-	-		
LOW-level output voltage	$V_{OL}$	Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$ $T_a=-40$ to $+85^\circ\text{C}$	0	-	0.4	V	
		Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$		-	0.45		
HIGH-level input voltage	$V_{IH}$	INH pin, measurement circuit 4	$0.7V_{DD}$	-	-	V	
LOW-level input voltage	$V_{IL}$	INH pin, measurement circuit 4	-	-	$0.3V_{DD}$	V	
Output leakage current	$I_Z$	Q pin, measurement circuit 5, INH="Low", $T_a=-40$ to $+85^\circ\text{C}$	$V_{OH}=V_{DD}$	-	-	10	$\mu\text{A}$
			$V_{OL}=V_{SS}$	-10	-	-	
		Q pin, measurement circuit 5, INH="Low"	$V_{OH}=V_{DD}$	-	-	100	
			$V_{OL}=V_{SS}$	-100	-	-	
Current consumption *1	$I_{DD}$	5053x1( $f_{OSC}$ ), measurement circuit 1, no load, INH="OPEN", $f_{OSC}=125\text{MHz}$ , $f_{OUT}=125\text{MHz}$	$V_{DD}=3.3\text{V}$	-	6.3	11.0	mA
			$V_{DD}=2.5\text{V}$	-	4.7	8.5	
			$V_{DD}=1.8\text{V}$	-	3.8	7.0	
		5053xP( $f_{OSC}$ ), measurement circuit 1, no load, INH="OPEN", $f_{OSC}=155\text{MHz}$ , $f_{OUT}=155\text{MHz}$	$V_{DD}=3.3\text{V}$	-	9.8	17.5	
			$V_{DD}=2.5\text{V}$	-	8	15	
Standby current	$I_{ST}$	Measurement circuit 1, INH="Low" $T_a=-40$ to $+85^\circ\text{C}$	-	-	10	$\mu\text{A}$	
		Measurement circuit 1, INH="Low"	-	-	100		
INH pull-up resistance	$R_{PU1}$	Measurement circuit 6	0.8	3	24	$\text{M}\Omega$	
	$R_{PU2}$	Measurement circuit 6	30	70	150	$\text{k}\Omega$	
Oscillator feedback resistance	$R_f$	Design value	50	100	200	$\text{k}\Omega$	
Oscillator capacitance	$C_G$	5053x1 ver. Design value (a monitor pattern on a wafer is tested),	0.8	1.0	1.2	$\text{pF}$	
	$C_D$	Excluding parasitic capacitance.	2.4	3.0	3.6		
	$C_G$	5053xP ver. Design value (a monitor pattern on a wafer is tested),	0.8	1.0	1.2	$\text{pF}$	
	$C_D$	Excluding parasitic capacitance.	2.4	3.0	3.6		

\*1. The consumption current  $I_{DD}(C_L)$  with a load capacitance( $C_L$ ) connected to the Q pin is given by the following equation, where  $I_{DD}$  is the no load consumption current and  $f_{OUT}$  is the output frequency.

$$I_{DD}(C_L)[\text{mA}] = I_{DD}[\text{mA}] + C_L[\text{pF}] \times V_{DD}[\text{V}] \times f_{OUT}[\text{MHz}] \times 10^{-3}$$

AC Characteristics

$V_{DD}=1.60$  to  $3.63V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $+105^{\circ}C$  unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Output rise time	$t_{r1}$	Measurement circuit 1, $C_L=15pF$ , $0.1V_{DD} \rightarrow 0.9V_{DD}$ , $V_{DD}=2.25$ to $3.63V$	-	1.0	2.0	ns
	$t_{r2}$	Measurement circuit 1, $C_L=15pF$ , $T_a=-40$ to $+85^{\circ}C$ $0.1V_{DD} \rightarrow 0.9V_{DD}$ , $V_{DD}=1.60$ to $2.25V$	-	1.5	2.5	
		Measurement circuit 1, $C_L=15pF$ , $0.1V_{DD} \rightarrow 0.9V_{DD}$ , $V_{DD}=1.60$ to $2.25V$	-	1.5	3.0	
Output fall time	$t_{f1}$	Measurement circuit 1, $C_L=15pF$ , $0.9V_{DD} \rightarrow 0.1V_{DD}$ , $V_{DD}=2.25$ to $3.63V$	-	1.0	2.0	ns
	$t_{f2}$	Measurement circuit 1, $C_L=15pF$ , $T_a=-40$ to $+85^{\circ}C$ $0.9V_{DD} \rightarrow 0.1V_{DD}$ , $V_{DD}=1.60$ to $2.25V$	-	1.5	2.5	
		Measurement circuit 1, $C_L=15pF$ , $0.9V_{DD} \rightarrow 0.1V_{DD}$ , $V_{DD}=1.60$ to $2.25V$	-	1.5	3.0	
Output duty cycle	DUTY	5053x1 ver. Measurement circuit 1, $T_a=25^{\circ}C$ , $C_L=15pF$ , $V_{DD}=1.60$ to $3.63V$	45	50	55	%
		5053xP ver. Measurement circuit 1, $T_a=25^{\circ}C$ , $C_L=15pF$ , $V_{DD}=2.25$ to $3.63V$	45	50	55	
Output disable delay time	$t_{OD}$	Measurement circuit 2, $T_a=25^{\circ}C$ , $C_L \leq 15pF$	-	-	200	ns

The ratings above are values obtained by measurements using NPC evaluation standard crystal element on a standards testing jig.

Ratings may have wide tolerances due to crystal element characteristics; thorough evaluation is recommended.

Timing Chart

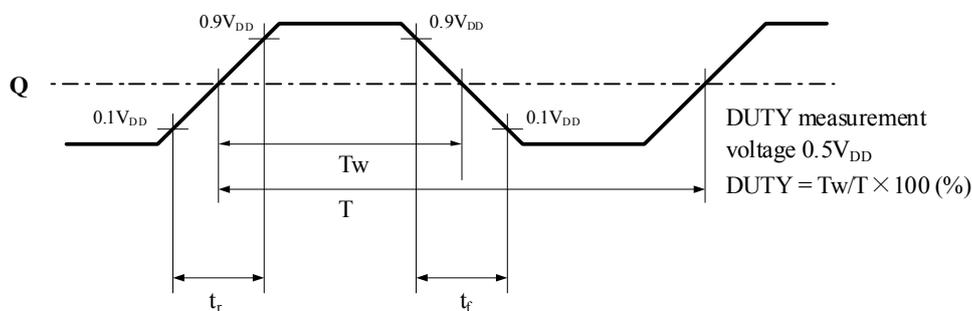


Figure 1. Output switching waveform

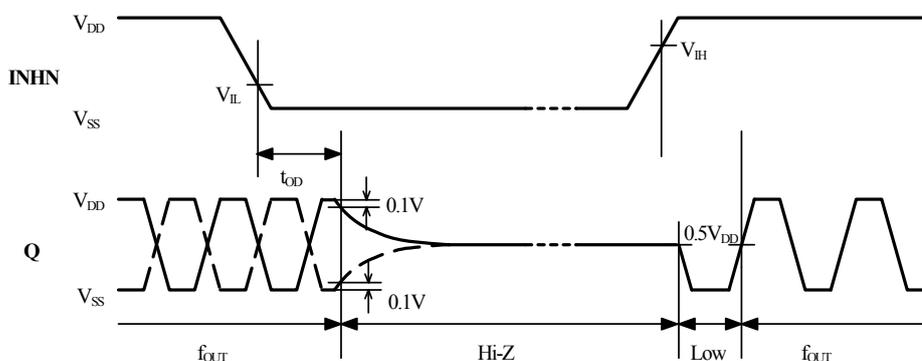


Figure 2. Output disable and oscillation start timing chart

## FUNCTIONAL DESCRIPTION

### INH N Function

Q output is stopped and becomes high impedance.

INH N	Q	Oscillator
HIGH(Open)	$f_{OUT}$	Operating
LOW	Hi-Z	Stopped

### Power Saving Pull-up Resistor

The INH N pin pull-up resistance changes its value to  $R_{PU1}$  or  $R_{PU2}$  in response to the input level (HIGH or LOW).

When INH N is tied to LOW level, the pull-up resistance becomes large ( $R_{PU1}$ ), thus reducing the current consumed by the resistance.

When INH N is left open circuit or tied to HIGH level, the pull-up resistance becomes small ( $R_{PU2}$ ), thus internal circuit of INH N becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

### Oscillation Detection Function

The 5053 series incorporate an oscillation detection circuit. The oscillation detection circuit disables the output until the oscillator circuit starts up. This function avoids the problem where the oscillator does not start, due to abnormal oscillation conditions, where power is applied or when the oscillator is restarted using INH N.

### C0 cancellation circuit

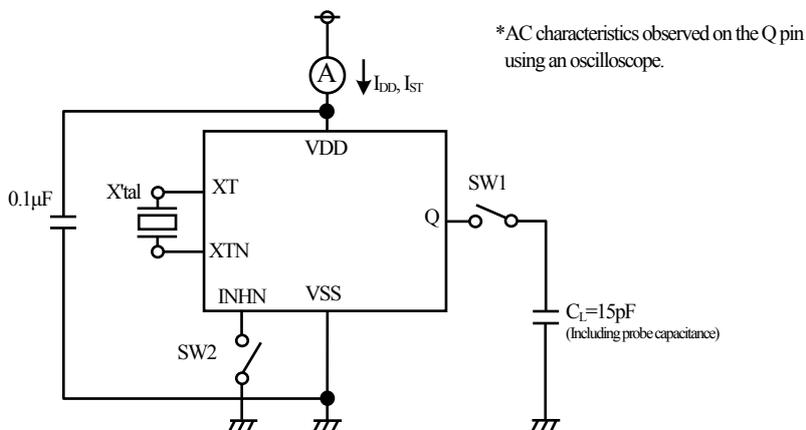
Oscillation circuit with a built-in C0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C0. It reduces the C0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C0.

This cancellation circuit makes it easier to maintain the oscillation margin.

## MEASUREMENT CIRCUITS

### MEASUREMENT CIRCUIT 1

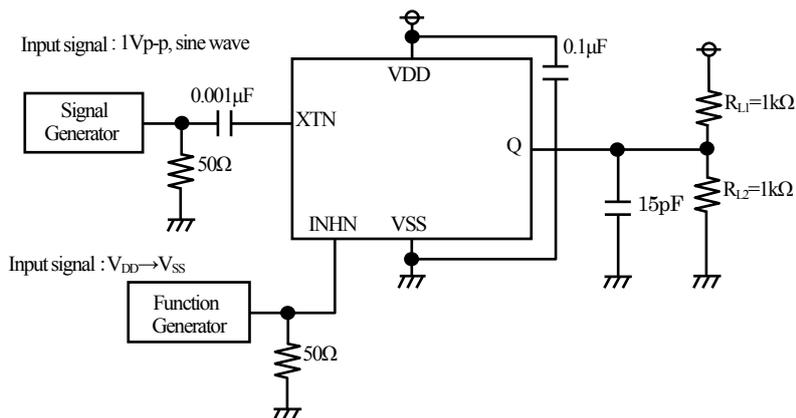
Measurement Parameter:  $I_{DD}$ ,  $I_{ST}$ , DUTY,  $t_b$ ,  $t_f$



Parameter	SW1	SW2
$I_{DD}$	OFF	OFF
$I_{ST}$	ON or OFF	ON
DUTY, $t_b$ , $t_f$	ON	OFF

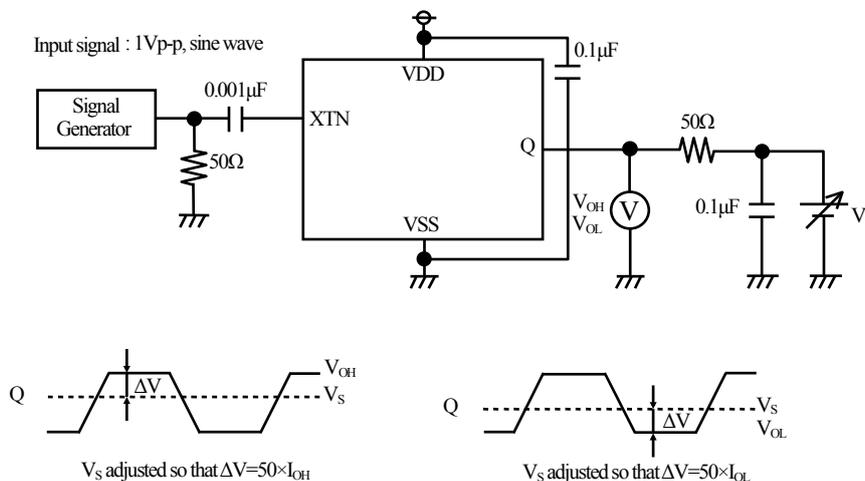
### MEASUREMENT CIRCUIT 2

Measurement Parameter:  $t_{OD}$



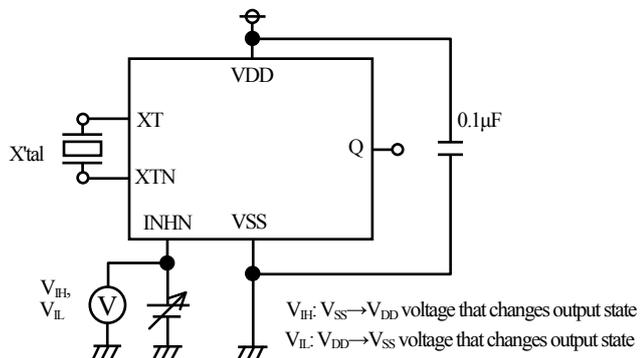
### MEASUREMENT CIRCUIT 3

Measurement Parameter:  $V_{OH}$ ,  $V_{OL}$



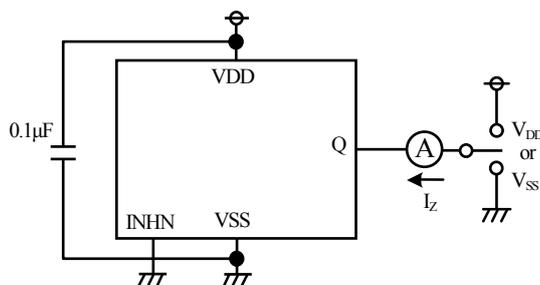
**MEASUREMENT CIRCUIT 4**

Measurement Parameter:  $V_{IH}$ ,  $V_{IL}$



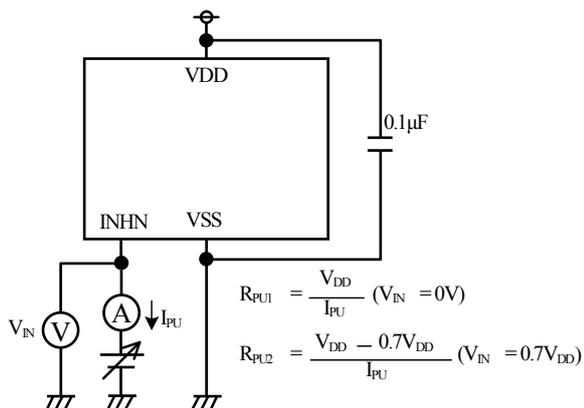
**MEASUREMENT CIRCUIT 5**

Measurement Parameter:  $I_Z$



**MEASUREMENT CIRCUIT 6**

Measurement Parameter:  $R_{PU1}$ ,  $R_{PU2}$



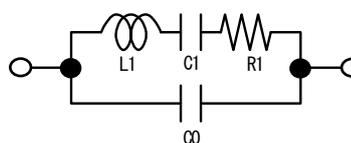
## REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

Crystal used for measurement

Parameter	125MHz	155MHz
C0(pF)	2.8	1.7
R1( $\Omega$ )	10	10

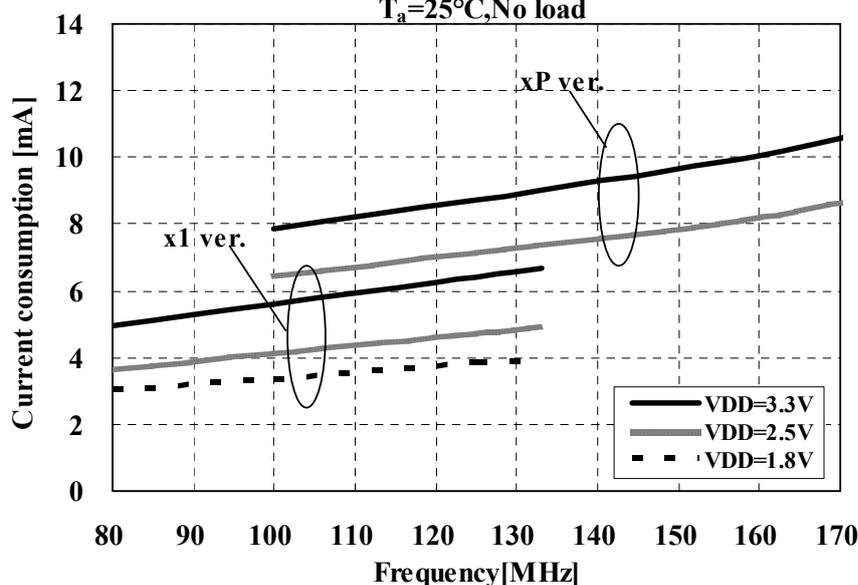
Crystal parameters



## Current Consumption

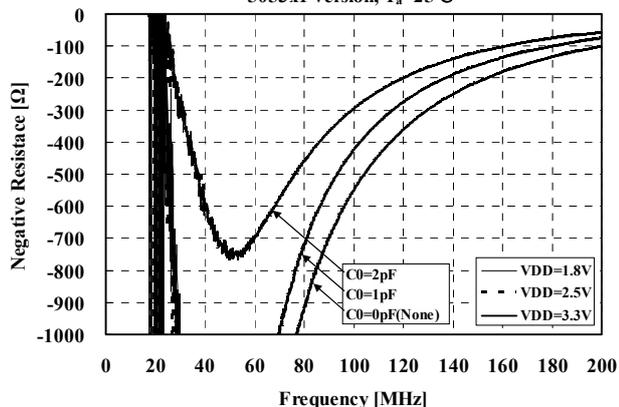
### Current Consumption Characteristics

$T_a=25^\circ\text{C}$ , No load

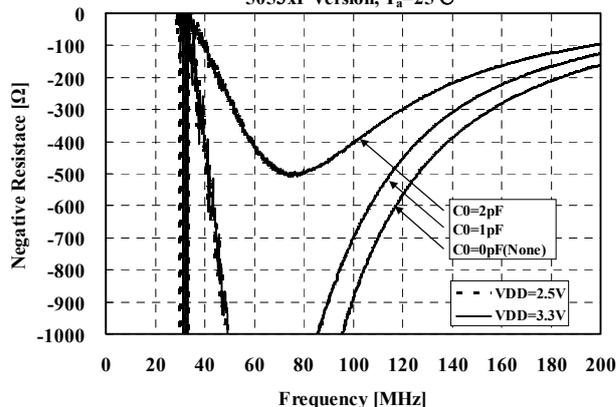


## Negative Resistance

Negative Resistance Characteristics  
5053x1 version,  $T_a=25^\circ\text{C}$

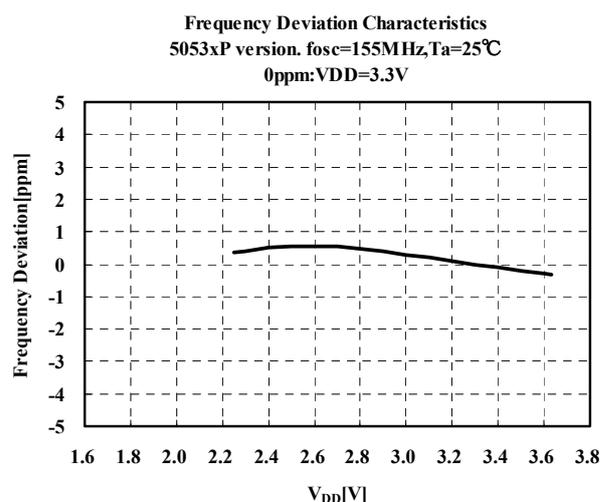
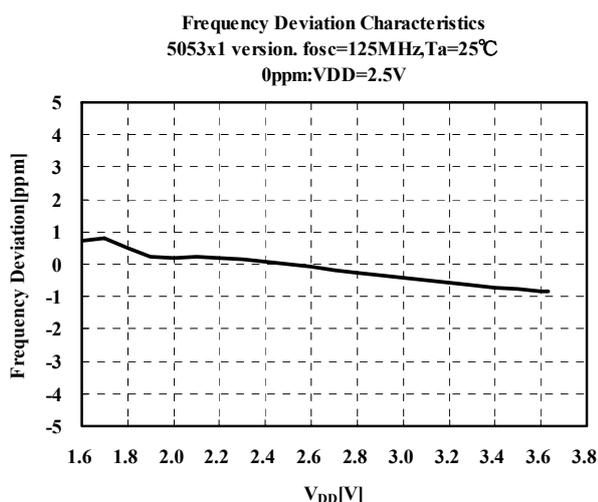


Negative Resistance Characteristics  
5053xP version,  $T_a=25^\circ\text{C}$

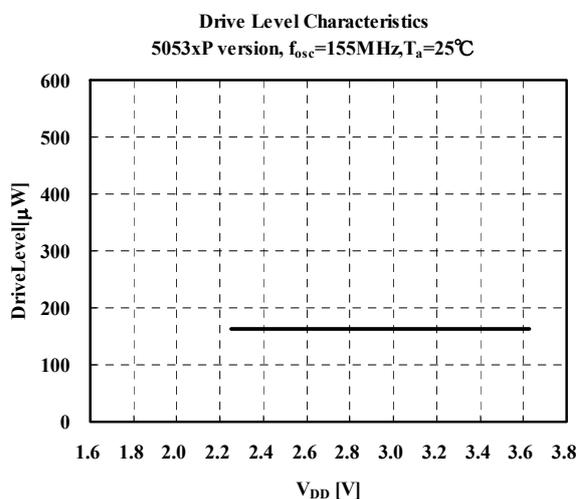
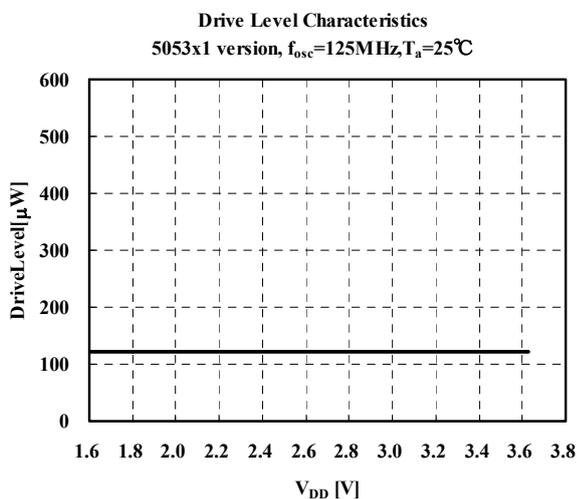


The figures show the measurement result of the crystal equivalent circuit C0 capacitance, connected between the XT and X1N pins. They were performed with Agilent 4396B using the NPC test jig. They may vary in a measurement jig, and measurement environment.

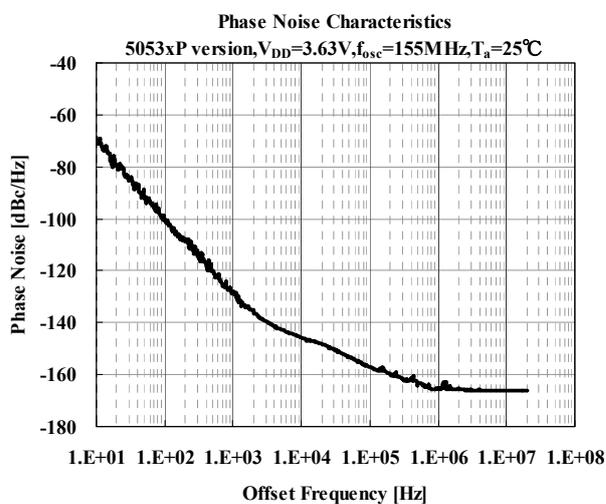
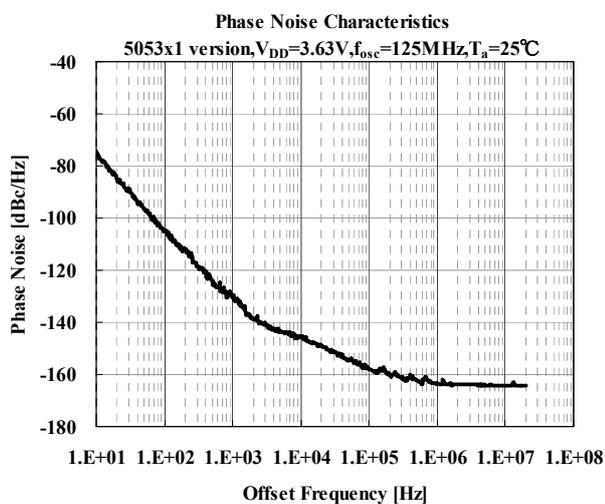
### Frequency Deviation by Voltage



### Drive Level

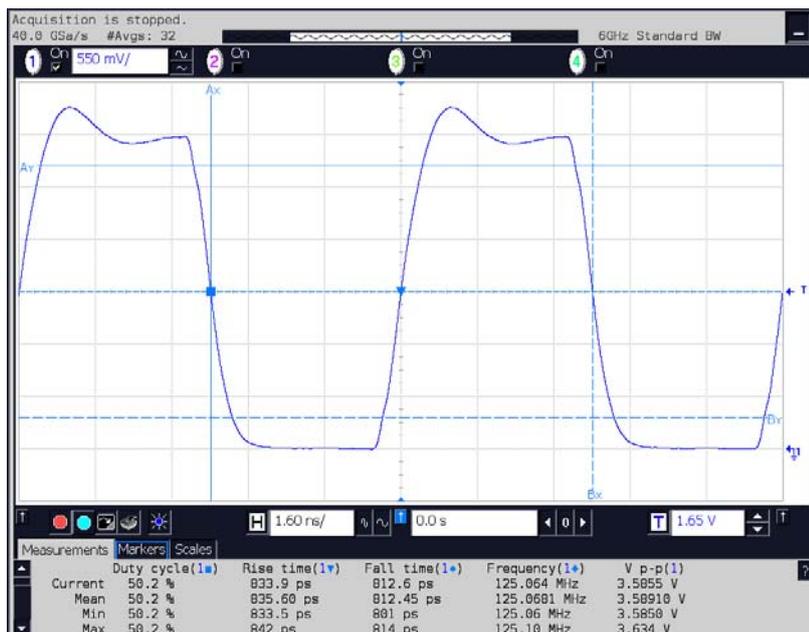


### Phase Noise

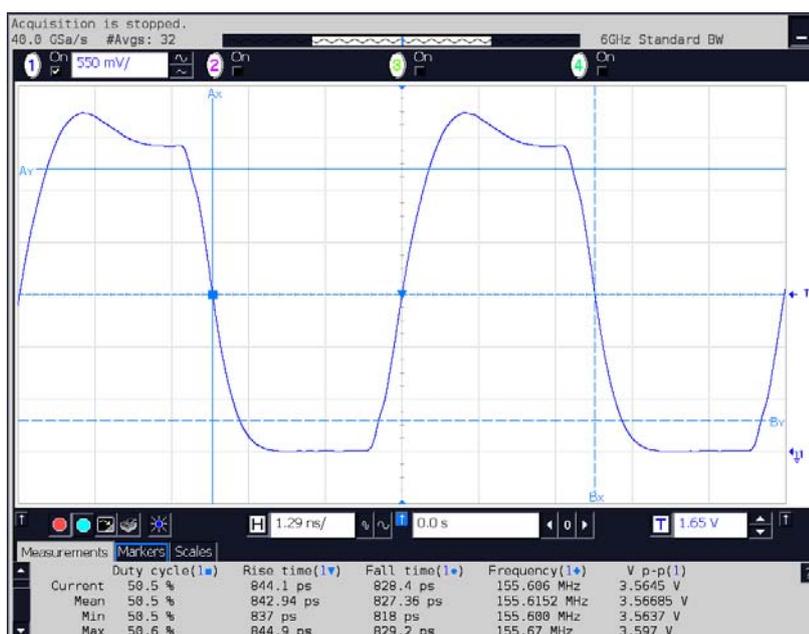


Measurement equipment: Signal Source Analyzer Agilent E5052B

## Output Waveform



x1 ver.,  $V_{DD}=3.3V$ ,  $f_{OUT}=125MHz$ ,  $C_L=15pF$ ,  $T_a=R.T.$



xP ver.,  $V_{DD}=3.3V$ ,  $f_{OUT}=155MHz$ ,  $C_L=15pF$ ,  $T_a=R.T.$

Measurement equipment: Oscilloscope Agilent 54855A

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