OVERVIEW

The 5052H series are miniature crystal oscillator module ICs supported 20MHz to 80 MHz fundamental oscillation mode and 125°C operation. The Oscillator circuit stage has voltage regulator drive, significantly reducing current consumption and crystal drive current, compared with existing devices, and significantly reducing the oscillator characteristics supply voltage dependency. There are 3 pad layout package options available for optimized mounting, making these devices ideal for miniature crystal oscillators.

FEATURES

- Wide range of operating supply voltage: 1.60 to 3.63V
- Regulated voltage drive oscillator circuit for reduced power consumption and crystal drive current
- Optimized low crystal drive current oscillation for miniature crystal units
- 3 pad layout options for mounting
  5052HAx: for Flip Chip Bonding
  5052HBx: for Wire Bonding (Type I)
  5052HCx: for Wire Bonding (Type II)
- Recommended oscillation frequency range
  (fundamental oscillator) :20 to 60MHz (Hx1~Hx5 ver.)
  40 to 80MHz (HxP~HxT ver.)
- Multi-stage frequency divider for low-frequency output support: 1.25MHz (Hx1~Hx5 ver.)
  2.5MHz (HxP~HxT ver.)
- Frequency divider built-in
  Selectable by version: f_{OSC},f_{OSC}/2,f_{OSC}/4,f_{OSC}/8,f_{OSC}/16
- Output drive capability: ±4mA
- -40 to 125°C operating temperature range
- Standby function
  High impedance in standby mode, oscillator stops
- CMOS output duty level (1/2V_{DD})
- 50±5% output duty
- 15pF output drive capability
- Wafer form (WF5052Hxx), Chip form (CF5052Hxx)

APPLICATIONS

- 3.2 x 2.5 , 2.5 x 2.0 , 2.0 x 1.6 size miniature crystal oscillator modules

SERIES CONFIGURATION

Operating supply voltage range[V]	PAD layout	Oscillation frequency range*1 [MHz]	Output frequency and version name*2				
			f_{OSC}	f_{OSC}/2	f_{OSC}/4	f_{OSC}/8	f_{OSC}/16
1.60 to 3.63	Flip Chip Bonding	20 to 60	5052HA1	5052HA2	5052HA3	5052HA4	5052HA5
		40 to 80	5052HAP	5052HAQ	5052HAR	5052HAS	5052HAT
	Wire Bonding Type I	20 to 60	5052HB1	5052HB2	5052HB3	5052HB4	5052HB5
		40 to 80	5052HBP	-	-	-	-
	Wire Bonding Type II	20 to 60	5052HC1	5052HC2	5052HC3	5052HC4	5052HC5
		40 to 80	5052HCP	-	-	-	-

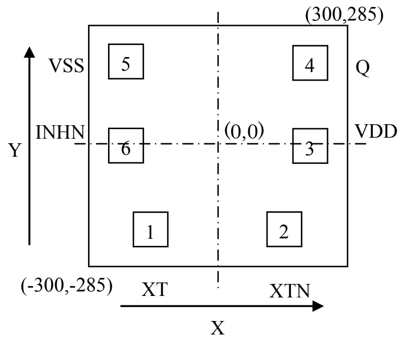
*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. It becomes WF5052Hxx in case of the wafer form and CF5052Hxx in case of the chip form.

ORDERING INFORMATION

Device	Package	Version name
WF5052Hxx-5	Wafer form	WF5052H□□-5 Form WF : Wafer form CF : Chip(Die) form Frequency divider function/Oscillation frequency range PAD layout A: for Flip Chip Bonding B: for Wire Bonding (Type I) C: for Wire Bonding (Type II)
CF5052Hxx-5	Chip form	

PAD LAYOUT

- WF5052HAx (for Flip Chip Bonding)
- CF5052HBx (for Wire Bonding (Type I))
- CF5052HCx (for Wire Bonding (Type II))

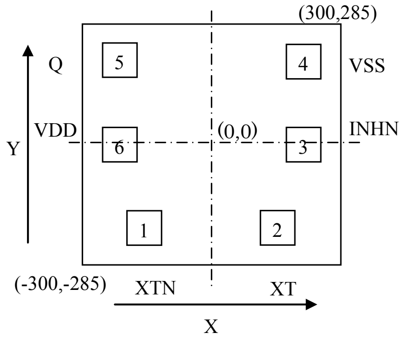


Chip size : 0.60x0.57mm

Chip thickness : 100μm

PAD size : 80μm

Chip base : V_{SS} level



Chip size : 0.60x0.57mm

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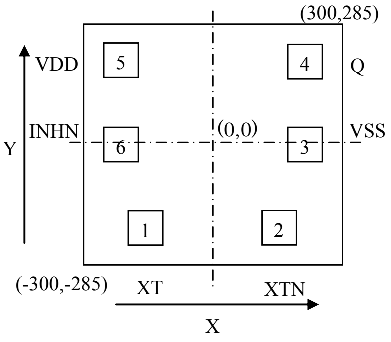


Chip size : 0.60x0.57mm

Chip thickness : 100μm

PAD size : 80μm

Chip base : V_{SS} level

· Coordinates at the chip center are (0,0).

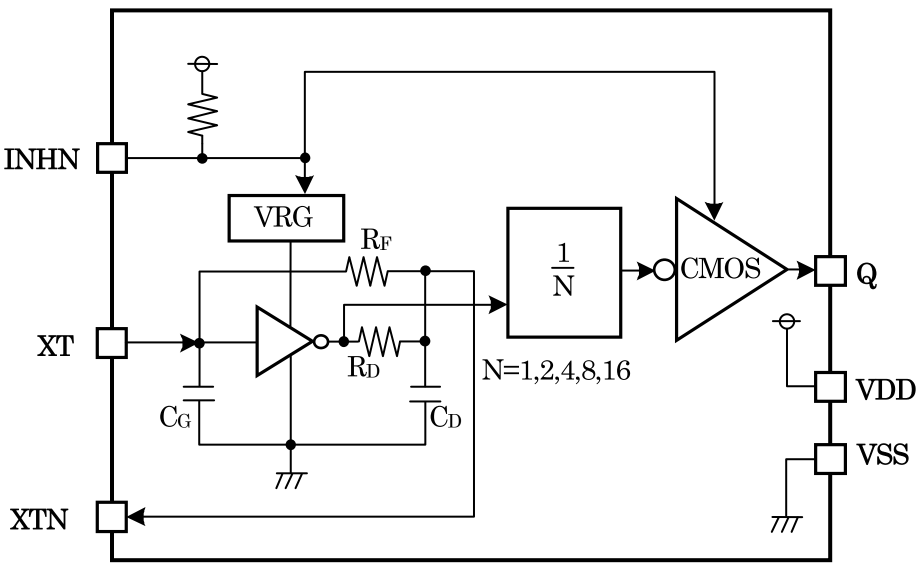
PAD COORDINATES

PAD No.	PAD coordinate[μm]	
	X	Y
1	-145.2	-193.5
2	145.2	-193.5
3	208.5	-1.1
4	208.5	193.5
5	-208.5	193.5
6	-208.5	-1.1

PIN DESCRIPTION

PAD No.			Pin	Function
5052HAx	5052HBx	5052HCx		
1	2	1	XT	Crystal connection pins.
2	1	2	XTN	Crystal is connected between XT and XTN.
3	6	5	VDD	(+)supply voltage
4	5	4	Q	Output one of f_{OSC},f_{OSC}/2,f_{OSC}/4,f_{OSC}/8,f_{OSC}/16
5	4	3	VSS	(-)ground
6	3	6	INHN	Input pin controlled output state(oscillator stops when LOW), Power-saving pull-up resistor built-in

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range[*1]	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range[*1*2]	V_{IN}	Input pins	-0.3 to V_{DD}+0.3	V
Output voltage range[*1*2]	V_{OUT}	Output pins	-0.3 to V_{DD}+0.3	V
Output current[*3]	I_{OUT}	Q pin	±20	mA
Junction temperature[*3]	T_j		150	°C
Storage temperature range[*4]	T_{STG}	Chip form, Wafer form	-65 to +150	°C

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Condition		Rating			Unit
				MIN	TYP	MAX	
Oscillator frequency[*1]	f_{OSC}	V_{DD}=1.60 to 3.63V	5052Hx1 ~ Hx5 ver.	20		60	MHz
			5052HxP ~ HxT ver.	40		80	
Output frequency	f_{OUT}	V_{DD}=1.60 to 3.63V	5052Hx1 ~ Hx5 ver.	1.25		60	MHz
		C_{LOUT}≤15pF	5052HxP ~ HxTver.	2.5		80	
Operating supply voltage	V_{DD}	Between VDD and VSS[*2]		1.60		3.63	V
Input voltage	V_{IN}	Input pins		V_{SS}		V_{DD}	V
Operating temperature	T_a			-40		+125	°C
Output load capacitance	C_{LOUT}	Q output				15	pF

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5052H series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
DC Characteristics (Hx1~Hx5 version)

V_{DD}=1.60 to 3.63V, V_{SS}=0V, T_a= -40 to +125°C unless otherwise noted.

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Q pin HIGH-level output voltage	V_{OH}	measurement circuit 3, I_{OH}=-4mA		V_{DD}-0.4		V_{DD}	V
Q pin LOW-level output voltage	V_{OL}	measurement circuit 3, I_{OL}=4mA		0		0.4	V
INHN pin HIGH-level input voltage	V_{IH}	measurement circuit 4		0.7V_{DD}			V
INHN pin LOW-level input voltage	V_{IL}	measurement circuit 4				0.3V_{DD}	V
Q pin Output leakage current	I_Z	measurement circuit 5, INHN="Low"	Q=V_{DD}			10	μA
			Q=V_{SS}	-10			
Current consumption*1	I_{DD}	5052Hx1(f_{OSC}), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=48MHz, f_{OUT}=48MHz	V_{DD}=3.3V		1.4	2.8	mA
			V_{DD}=2.5V		0.9	1.8	
			V_{DD}=1.8V		0.7	1.4	
		5052Hx2(f_{OSC}/2), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=48MHz, f_{OUT}=24MHz	V_{DD}=3.3V		1.2	2.4	mA
			V_{DD}=2.5V		0.8	1.6	
			V_{DD}=1.8V		0.6	1.2	
		5052Hx3(f_{OSC}/4), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=48MHz, f_{OUT}=12MHz	V_{DD}=3.3V		1.0	2.0	mA
			V_{DD}=2.5V		0.7	1.4	
			V_{DD}=1.8V		0.5	1.0	
		5052Hx4(f_{OSC}/8), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=48MHz, f_{OUT}=6MHz	V_{DD}=3.3V		1.0	2.0	mA
			V_{DD}=2.5V		0.6	1.2	
			V_{DD}=1.8V		0.5	1.0	
		5052Hx5(f_{OSC}/16),measurement circuit 1, no load, INHN="OPEN", f_{OSC}=48MHz, f_{OUT}=3MHz	V_{DD}=3.3V		0.9	1.8	mA
			V_{DD}=2.5V		0.6	1.2	
			V_{DD}=1.8V		0.4	0.8	
Standby current	I_{ST}	Measurement circuit 1 INHN="Low"	T_a=-40 to +85°C			10	μA
			T_a=-40 to +125°C			20	
INHN pin pull-up resistance	R_{PU1}	Measurement circuit 6		0.8	3	24	MΩ
	R_{PU2}	Measurement circuit 6		30	70	150	kΩ
Oscillator feedback resistance	R_f			50	100	200	kΩ
Oscillator capacitance	C_G	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		4.0	5.0	6.0	pF
	C_D			6.4	8.0	9.6	

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA]+C_{LOUT}[pF]\times V_{DD}[V]\times f_{OUT}[MHz]\cdot 10^{-3}$$

DC Characteristics (HxP~HxT version)

V_{DD}=1.60 to 3.63V, V_{SS}=0V, T_a= -40 to +125°C unless otherwise noted.

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit
Q pin HIGH-level output voltage	V_{OH}	measurement circuit 3, I_{OH}=-4mA		V_{DD}-0.4		V_{DD}	V
Q pin LOW-level output voltage	V_{OL}	measurement circuit 3, I_{OL}=4mA		0		0.4	V
INHN pin HIGH-level input voltage	V_{IH}	measurement circuit 4		0.7V_{DD}			V
INHN pin LOW-level input voltage	V_{IL}	measurement circuit 4				0.3V_{DD}	V
Q pin Output leakage current	I_Z	measurement circuit 5, INHN="Low"	Q=V_{DD}			10	µA
			Q=V_{SS}	-10			
Current consumption[*1]	I_{DD}	5052HxP(f_{OSC}), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=80MHz, f_{OUT}=80MHz	V_{DD}=3.3V		2.4	4.8	mA
			V_{DD}=2.5V		1.7	3.4	
			V_{DD}=1.8V		1.3	2.6	
		5052HxQ(f_{OSC}/2), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=80MHz, f_{OUT}=40MHz	V_{DD}=3.3V		2.0	4.0	mA
			V_{DD}=2.5V		1.3	2.6	
			V_{DD}=1.8V		0.9	1.8	
		5052HxR(f_{OSC}/4), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=80MHz, f_{OUT}=20MHz	V_{DD}=3.3V		1.7	3.4	mA
			V_{DD}=2.5V		1.1	2.2	
			V_{DD}=1.8V		0.8	1.6	
		5052HxS(f_{OSC}/8), measurement circuit 1, no load, INHN="OPEN", f_{OSC}=80MHz, f_{OUT}=10MHz	V_{DD}=3.3V		1.5	3.0	mA
			V_{DD}=2.5V		0.9	1.8	
			V_{DD}=1.8V		0.7	1.4	
		5052HxT(f_{OSC}/16),measurement circuit 1, no load, INHN="OPEN", f_{OSC}=80MHz, f_{OUT}=5MHz	V_{DD}=3.3V		1.4	2.8	mA
			V_{DD}=2.5V		0.9	1.8	
			V_{DD}=1.8V		0.7	1.4	
Standby current	I_{ST}	Measurement circuit 1 INHN="Low"	T_a=-40 to +85°C			10	µA
			T_a=-40 to +125°C			20	
INHN pin pull-up resistance	R_{PU1}	Measurement circuit 6		0.8	3	24	MΩ
	R_{PU2}	Measurement circuit 6		30	70	150	kΩ
Oscillator feedback resistance	R_f			50	100	200	kΩ
Oscillator capacitance	C_G	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.		1.6	2.0	2.4	pF
	C_D			2.4	3.0	3.6	

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[mA] = I_{DD}[mA]+C_{LOUT}[pF]\times V_{DD}[V]\times f_{OUT}[MHz]\cdot 10^{-3}$$

AC Characteristics (Hx1~Hx5 version)

V_{DD} = 1.60 to 3.63V, V_{SS} = 0V, T_a = -40 to +125°C unless otherwise noted

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Q pin Output rise time	t_{r1}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=2.25 to 3.63V		1.5	5.0	ns
	t_{r2}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=1.60 to 2.25V		2.0	6.0	
Q pin Output fall time	t_{f1}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=2.25 to 3.63V		1.5	5.0	ns
	t_{f2}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=1.60 to 2.25V		2.0	6.0	
Q pin Output duty cycle	DUTY	Measurement circuit 1, T_a=25°C, C_{LOUT}=15pF, V_{DD}=1.60 to 3.63V	45	50	55	%
Q pin Output disable delay time	t_{OD}	Measurement circuit 2, T_a=25°C, C_{LOUT}≤15pF			200	ns

AC Characteristics (HxP~HxTversion)

V_{DD} = 1.60 to 3.63V, V_{SS} = 0V, T_a = -40 to +125°C unless otherwise noted

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Q pin Output rise time	t_{r1}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=2.25 to 3.63V		1.0	3.5	ns
	t_{r2}	Measurement circuit 1, C_{LOUT}=15pF, $0.1V_{DD} \rightarrow 0.9V_{DD}$, V_{DD}=1.60 to 2.25V		1.5	5.0	
Q pin Output fall time	t_{f1}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=2.25 to 3.63V		1.0	3.5	ns
	t_{f2}	Measurement circuit 1, C_{LOUT}=15pF, $0.9V_{DD} \rightarrow 0.1V_{DD}$, V_{DD}=1.60 to 2.25V		1.5	5.0	
Q pin Output duty cycle	DUTY	Measurement circuit 1, T_a=25°C, C_{LOUT}=15pF, V_{DD}=1.60 to 3.63V	45	50	55	%
Q pin Output disable delay time	t_{OD}	Measurement circuit 2, T_a=25°C, C_{LOUT}≤15pF			200	ns

Timing chart

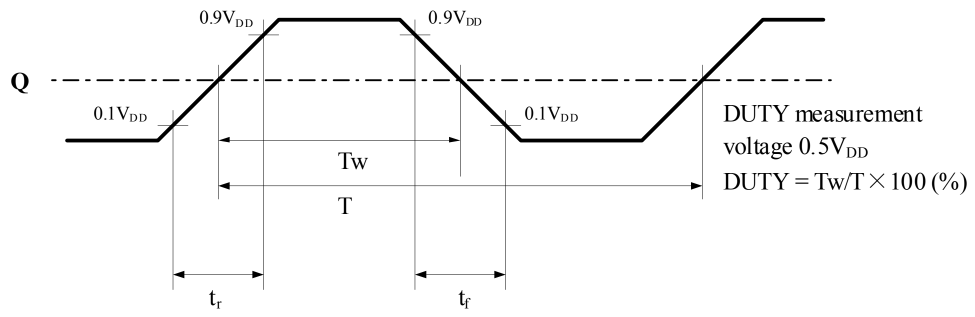
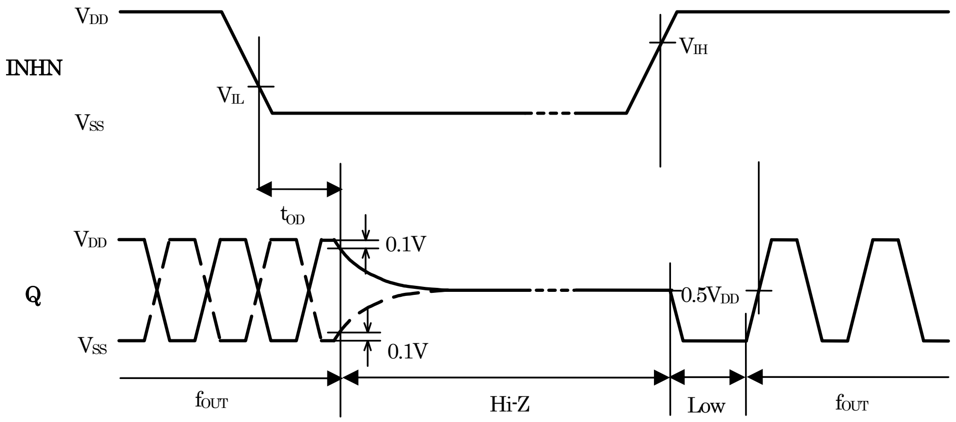


Figure 1. Output switching waveform



When INHN goes HIGH to LOW, the Q output becomes high impedance.

When INHN goes LOW to HIGH, the Q output goes LOW once and then becomes normal output operation after having detected oscillation signals.

Figure 2. Output disable and oscillation start timing chart

FUNCTIONAL DESCRIPTION

INHN Function

Q output is stopped and becomes high impedance.

INHN	Q	Oscillator
HIGH or Open	f_{OUT}	Operating
LOW	Hi-Z	Stopped

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).
When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level.
Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

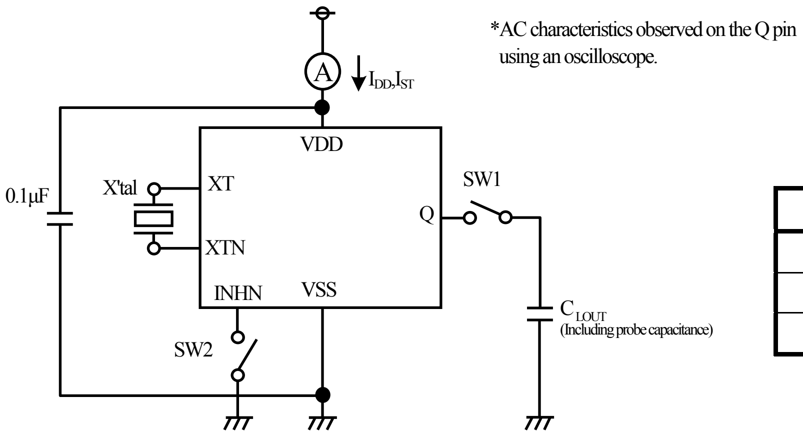
Oscillation Detection Function

The 5052H series have an oscillation detection circuit.
The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

MEASUREMENT CIRCUITS

MEASUREMENT CIRCUIT 1

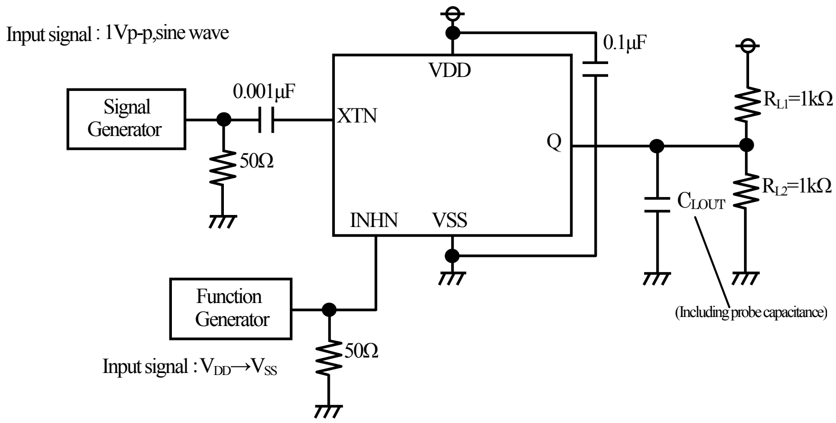
Measurement Parameter : I_{DD}, I_{ST}, DUTY t_r, t_f



Parameter	SW1	SW2
I_{DD}	OFF	OFF
I_{ST}	ON or OFF	ON
DUTY, t_r, t_f	ON	OFF

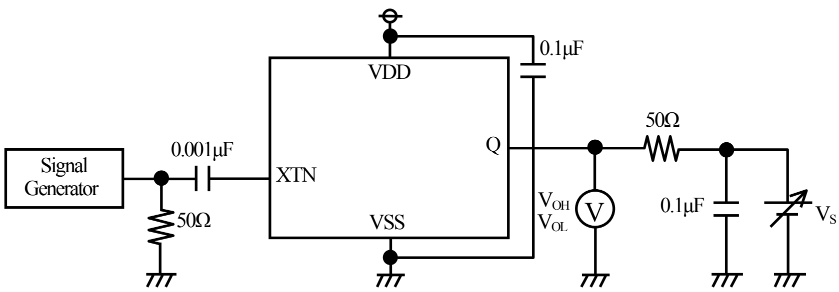
MEASUREMENT CIRCUIT 2

Measurement Parameter : t_{OD}

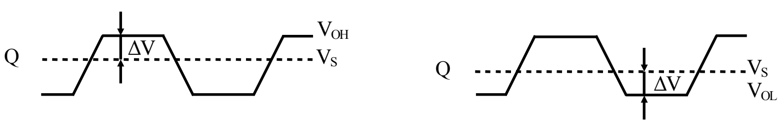


MEASUREMENT CIRCUIT 3

Measurement Parameter : V_{OH} ,V_{OL}



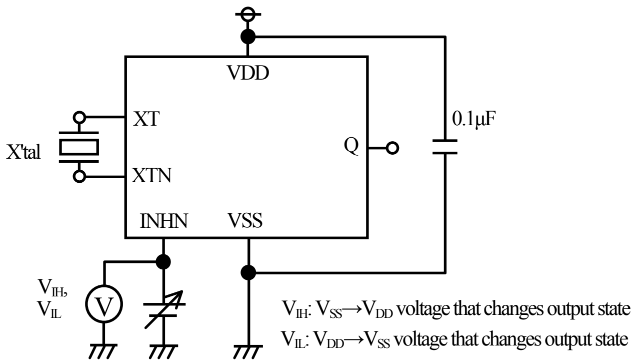
XTN input signal : 1Vp-p,sine wave



V_S adjusted so that $\Delta V=50\times I_{OH}$ V_S adjusted so that $\Delta V=50\times I_{OL}$

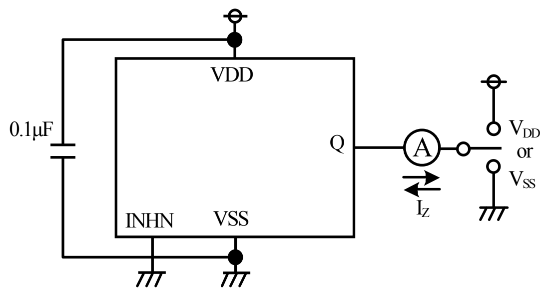
MEASUREMENT CIRCUIT 4

Measurement Parameter : V_{IH}, V_{IL}



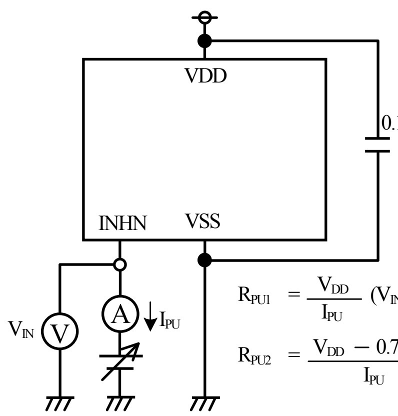
MEASUREMENT CIRCUIT 5

Measurement Parameter : I_Z



MEASUREMENT CIRCUIT 6

Measurement Parameter : R_{PU1}, R_{PU2}



$$R_{PU1} = \frac{V_{DD}}{I_{PU}} \quad (V_{IN} = 0V)$$

$$R_{PU2} = \frac{V_{DD} - 0.7V_{DD}}{I_{PU}} \quad (V_{IN} = 0.7V_{DD})$$

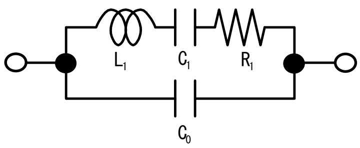
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

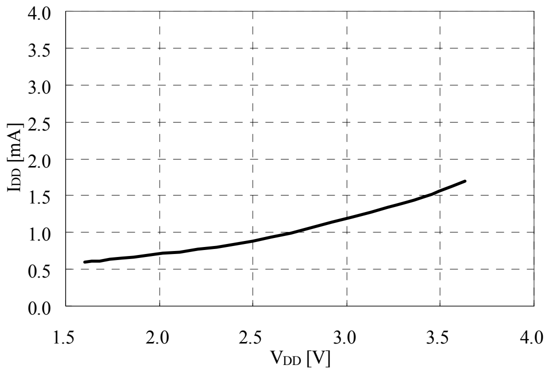
Crystal used for measurement

Parameter	40MHz	48MHz	80MHz
C_0(pF)	1.4	1.8	3.2
R_1(Ω)	8	7	13

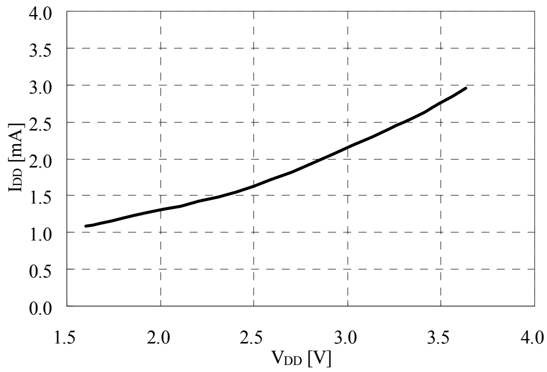
Crystal parameters



Current Consumption

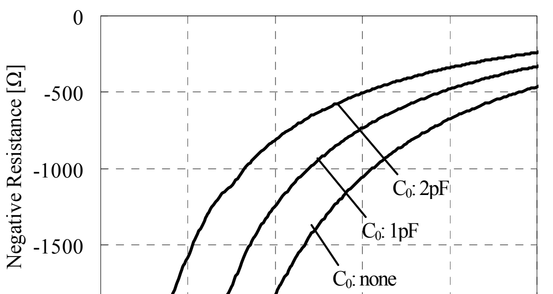


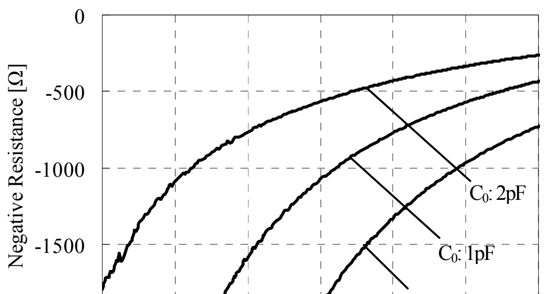
5052Hx1, f_{OSC}=48MHz, T_a=25°C, no load



5052HxP, f_{OSC}=80MHz, T_a=25°C, no load

Negative Resistance





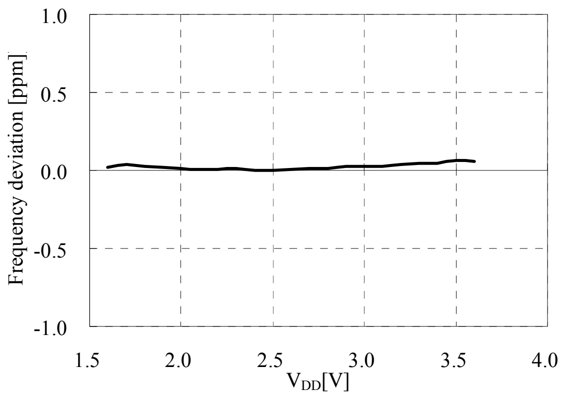
5052Hx1, V_{DD}=3.3V, T_a=25°C

5052HxP, V_{DD}=3.3V, T_a=25°C

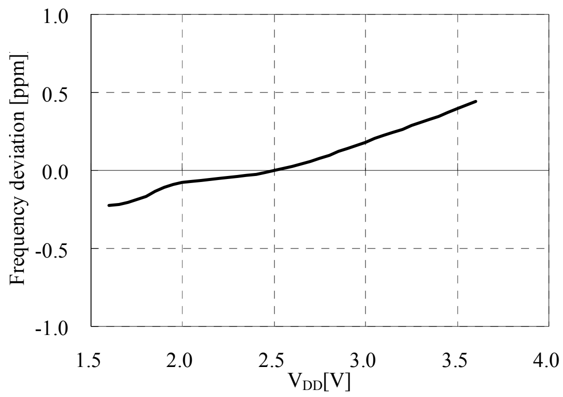
Measurement equipment: Agilent Impedance analyzer 4396B

The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XT and XTN pins.
They were performed with Agilent 4396B using the NPC test jig.
They may vary in a measurement jig, and measurement environment.

Frequency Deviation by Voltage

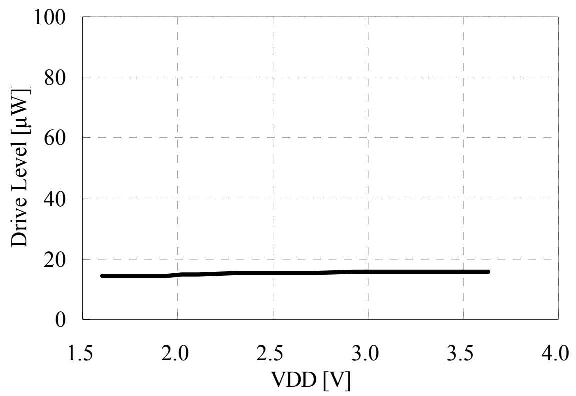


5052Hx1, f_{OSC}=40MHz, T_a=25°C, 2.5V std.

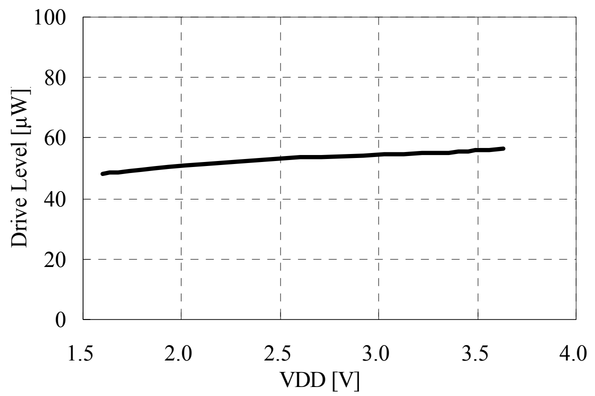


5052HxP, f_{OSC}=80MHz, T_a=25°C, 2.5V std.

Drive Level

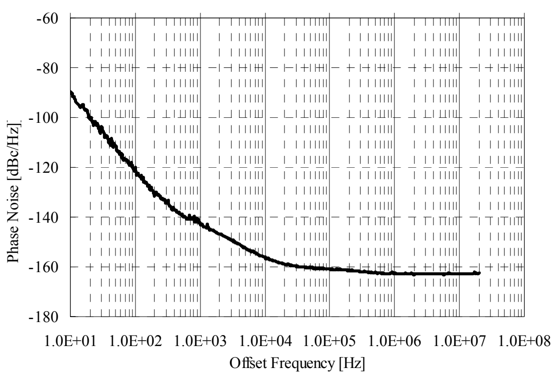


5052Hx1, f_{OSC}=40MHz, T_a=25°C

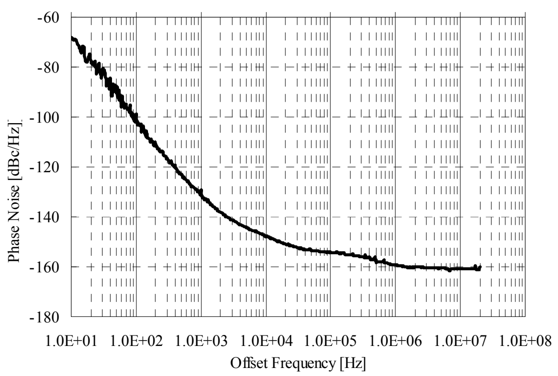


5052HxP, f_{OSC}=80MHz, T_a=25°C

Phase Noise



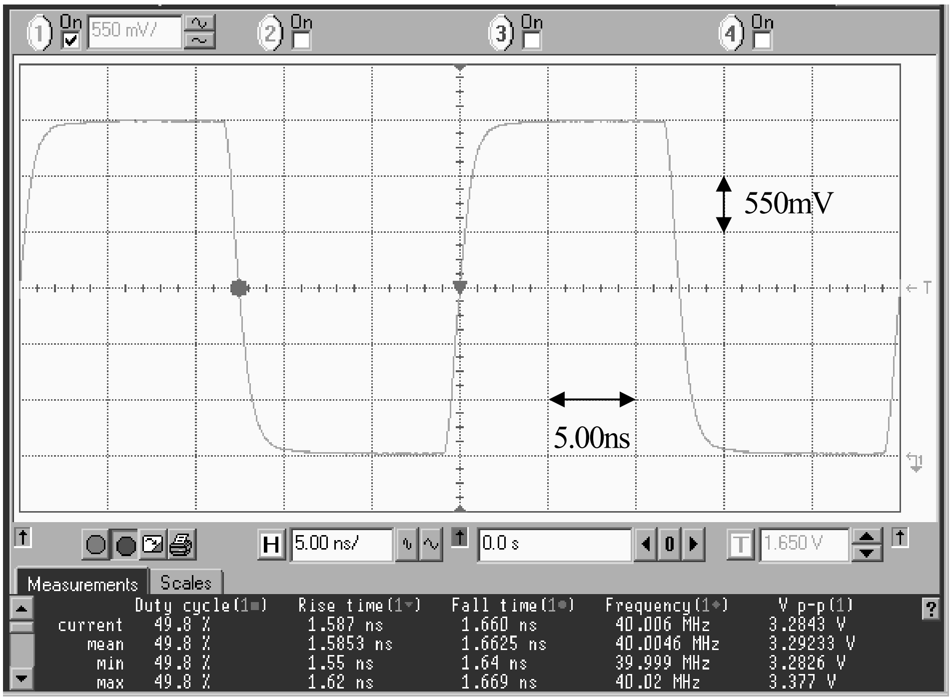
5052Hx1, f_{OSC}=40MHz, V_{DD}=3.3V, T_a=25°C



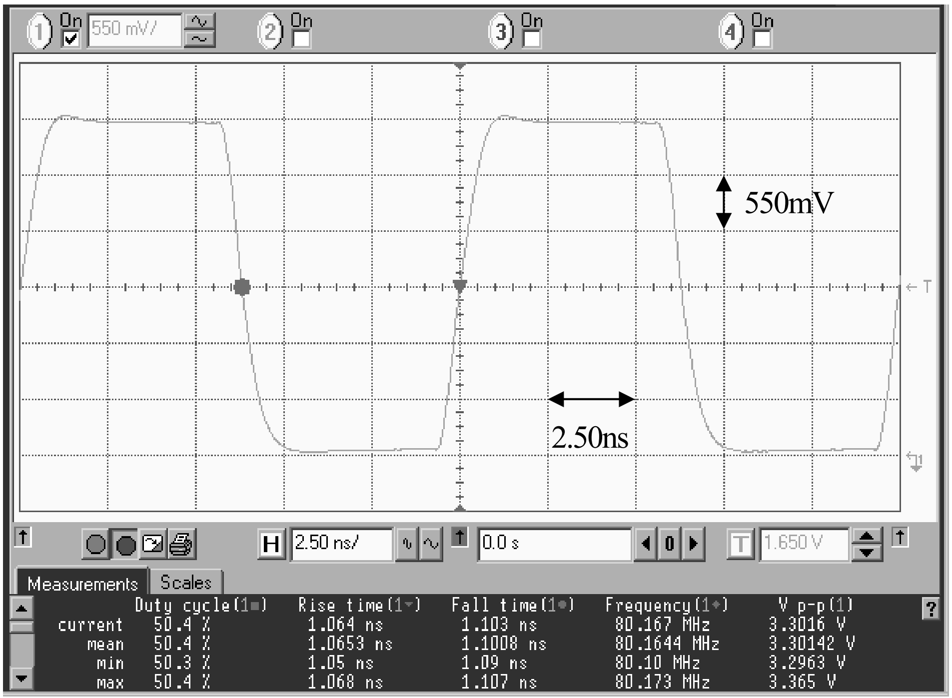
5052HxP, f_{OSC}=80MHz, V_{DD}=3.3V, T_a=25°C

Measurement equipment: Signal Source Analyzer Agilent E5052B

Output Waveform



5052Hx1 version, V_{DD}=3.3V, f_{OUT}=40MHz, C_{LOUT}=15pF, T_a: Room temperature



5052HxP version, V_{DD}=3.3V, f_{OUT}=80MHz, C_{LOUT}=15pF, T_a: Room temperature
Measurement equipment: Oscilloscope Agilent DSO80604B

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