

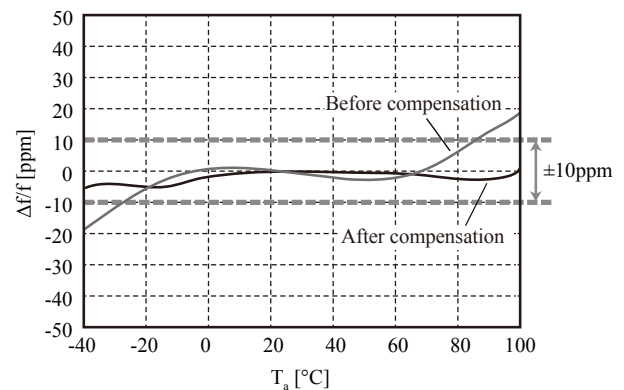
OVERVIEW

The 5041 series are high-stability clock oscillator ICs with built-in frequency adjustment functions. The frequency adjustment functions can be optimized, by the addition of a minimal adjustment process, to improve the frequency stability. The function is implemented using frequency adjustment data written to a built-in EEPROM over a 1-wire serial interface. The ICs are ideal for compact crystal oscillators for use in applications such as Wireless-LAN that require high frequency stability in the order of ± 30 to ± 10 ppm. They use a pad layout suitable for flip chip bonding mounting.

FEATURES

- Realizing frequency stability improvement with minimal additional process
- Temperature compensation range / operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Frequency adjustment functions built-in
 - <Frequency-temperature characteristics compensation function>
 - AT-cut crystal, 3rd order frequency-temperature characteristics compensation, with independent low-temperature and high-temperature compensation settings
 - Center frequency adjustment function
 - Temperature rotation compensation function
 - Low-temperature characteristics compensation
 - High-temperature characteristics compensation
- Rewritable EEPROM built-in
- 6 pads: same as general clock oscillator ICs
- Operating supply voltage range
 - 5041AxB: 2.25V to 3.63V
 - 5041BxB: 1.60V to 2.25V
- Recommended oscillation frequency range (for fundamental oscillation): 20MHz to 55MHz
- Frequency divider built-in
 - Frequency divider output for 1.25MHz (min) low frequency output
 - Selectable by version: f_{osc} , $f_{osc}/2$, $f_{osc}/4$, $f_{osc}/8$, $f_{osc}/16$
- Standby function
 - High-impedance in standby mode, oscillator stops
- CMOS output
- 15pF output load capacitance
- Pad layout for flip chip bonding
- Wafer form (WF5041xxB)

FREQUENCY CHARACTERISTICS COMPENSATION BEFORE and AFTER ADJUSTMENT



APPLICATIONS

- 3.2mm \times 2.5mm, 2.5mm \times 2.0mm, 2.0mm \times 1.6mm size miniature crystal oscillator modules
- Wireless-LAN and applications requiring high-stability clock oscillators

ORDERING INFORMATION

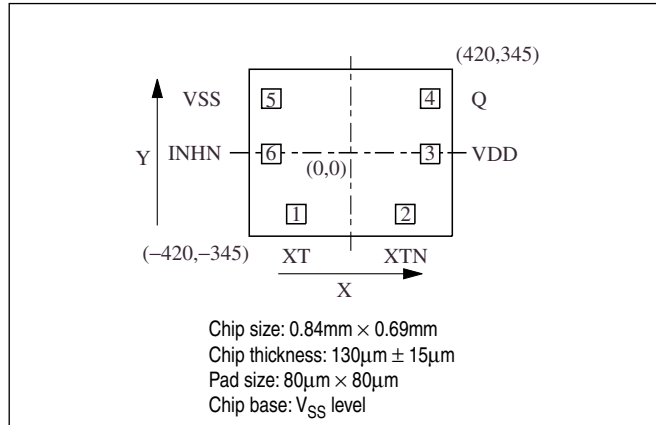
Device	Package	Version name
WF5041xxB-4	Wafer form	WF5041 <input type="checkbox"/> <input type="checkbox"/> B-4 Form WF: Wafer form ↑ ↑ ↑ ↑ Frequency divider function (output frequency) ↑ Operating supply voltage

SERIES CONFIGURATION

Version name	Operating supply voltage range [V]	Output frequency f_{OUT} (divider ratio)
5041A1B	2.25 to 3.63	f_{OSC}
5041A2B		$f_{OSC}/2$
5041A3B		$f_{OSC}/4$
5041A4B		$f_{OSC}/8$
5041A5B		$f_{OSC}/16$
5041B1B	1.60 to 2.25	f_{OSC}
5041B2B		$f_{OSC}/2$
5041B3B		$f_{OSC}/4$
5041B4B		$f_{OSC}/8$
5041B5B		$f_{OSC}/16$

PAD LAYOUT

(Unit: μm)

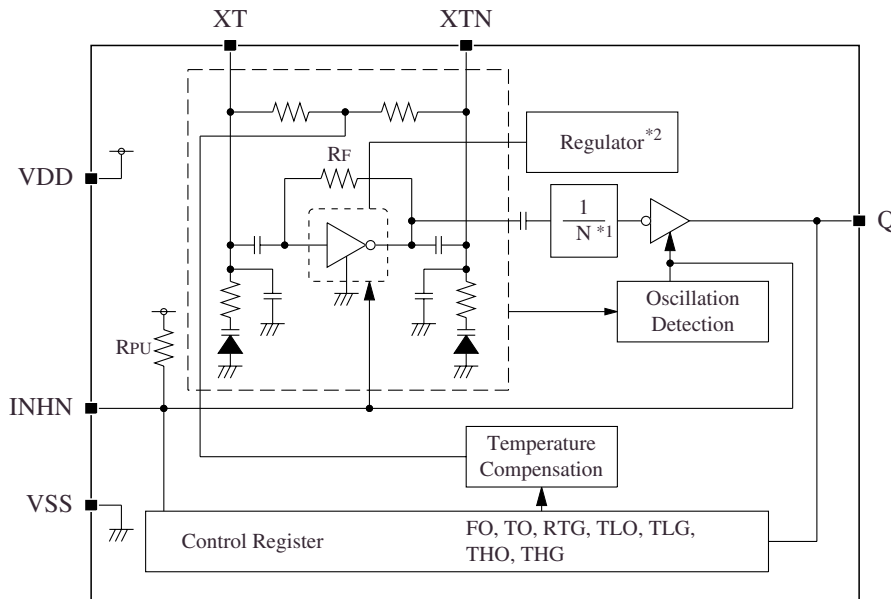


PAD DIMENSIONS PIN DESCRIPTION

Pad No.	Pin	I/O ^{*1}	Name	Description	Pad dimensions [μm]	
					X	Y
1	XT	I	Amplifier input	Crystal connection pins. Crystal is connected between XT and XTN.	-225.2	-253.5
2	XTN	O	Amplifier output		225.2	-253.5
3	VDD	-	(+) supply voltage	-	328.5	-5.0
4	Q	O	Output	Output frequency determined by internal circuit to one of f_{OSC} , $f_{\text{OSC}}/2$, $f_{\text{OSC}}/4$, $f_{\text{OSC}}/8$, $f_{\text{OSC}}/16$. High impedance in standby mode	328.5	223.8
5	VSS	-	(-) ground	-	-328.5	223.8
6	INH	I	Output state control input	High impedance when LOW (oscillator stops). Power-saving pull-up resistor built-in.	-328.5	-5.0

*1. I: Input, O: Output

BLOCK DIAGRAM



*1. N = 1, 2, 4, 8, 16 (mask option)

*2. 5041AxB version only

ABSOLUTE MAXIMUM RATINGS

$V_{SS} = 0V$ unless otherwise noted.

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range ^{*1}	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Program read/write input voltage range ^{*1}	V_{PP}	Between INHN and VSS	-0.3 to +16.5	V
Input voltage range ^{*1 *2}	V_{IN}	Input pins	-0.3 to $V_{DD} + 0.3$	V
Output voltage range ^{*1 *2}	V_{OUT}	Output pins	-0.3 to $V_{DD} + 0.3$	V
Output current ^{*1}	I_{OUT}	Q pin	± 20	mA
Storage temperature range ^{*3}	T_{STG}	Wafer form	-65 to +150	°C
EEPROM maximum writes	N_{EW}		100	times

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

RECOMMENDED OPERATING CONDITIONS

$V_{SS} = 0V$ unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
Supply voltage	V_{DD}	Between VDD and VSS	5041AxB	2.25	-	3.63	V
			5041BxB	1.60	-	2.25	V
Input voltage	V_{IN}	Input pins (XT, INHN)	V_{SS}	-	V_{DD}	V	
Operating temperature	T_{OPR}		-40	-	+85	°C	
Oscillation frequency ^{*1}	f_{OSC}	5041AxB	20	-	55	MHz	
		5041BxB	20	-	55	MHz	
Output frequency ^{*1}	f_{OUT}	Q pin	5041AxB	1.25	-	55	MHz
			5041BxB	1.25	-	55	MHz
Output load capacitance	C_{LOUT}	Q pin	-	-	15	pF	

*1. The recommended oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

- Mount a ceramic chip capacitor that is larger than 0.01 μ F proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5041 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.
- Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

ELECTRICAL CHARACTERISTICS

DC Characteristics (5041A1B to A5B)

$V_{DD} = 2.25V$ to $3.63V$, $V_{SS} = 0V$, $T_{OPR} = -40^{\circ}C$ to $+85^{\circ}C$, $C_{LOUT} = 15pF$ unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			MIN	TYP	MAX		
Operating-mode current consumption ^{*1}	I_{DD}	5041A1B ($f_{OUT} = f_{OSC}$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$	$V_{DD} = 2.5V$	–	1.4	2.8	mA
			$V_{DD} = 3.3V$	–	1.7	3.4	mA
		5041A2B ($f_{OUT} = f_{OSC}/2$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$	$V_{DD} = 2.5V$	–	1.1	2.2	mA
			$V_{DD} = 3.3V$	–	1.4	2.7	mA
		5041A3B ($f_{OUT} = f_{OSC}/4$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$	$V_{DD} = 2.5V$	–	1.0	1.9	mA
			$V_{DD} = 3.3V$	–	1.2	2.4	mA
5041A4B ($f_{OUT} = f_{OSC}/8$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$	$V_{DD} = 2.5V$	–	0.9	1.7	mA		
	$V_{DD} = 3.3V$	–	1.0	2.1	mA		
5041A5B ($f_{OUT} = f_{OSC}/16$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$	$V_{DD} = 2.5V$	–	0.8	1.7	mA		
	$V_{DD} = 3.3V$	–	1.0	2.0	mA		
Standby-mode current consumption	I_{ST}	Measurement circuit 1, INHN = LOW	–	–	10	μA	
HIGH-level output voltage	V_{OH}	Q pin, Measurement circuit 3, $I_{OH} = -4mA$	$V_{DD}-0.4$	–	–	V	
LOW-level output voltage	V_{OL}	Q pin, Measurement circuit 3, $I_{OL} = 4mA$	–	–	0.4	V	
Output leakage current	I_Z	Measurement circuit 4, INHN = LOW	$Q = V_{DD}$	–	–	10	μA
			$Q = V_{SS}$	–10	–	–	μA
HIGH-level input current	V_{IH}	INHN pin, Measurement circuit 5	$0.7V_{DD}$	–	–	V	
LOW-level input current	V_{IL}		–	–	$0.3V_{DD}$	V	
INHN pull-up resistance	R_{PU1}	Measurement circuit 6	INHN = V_{SS}	0.4	1.5	10	$M\Omega$
	R_{PU2}		INHN = $0.7V_{DD}$	50	100	200	$k\Omega$

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT}) [mA] = I_{DD} [mA] + C_{LOUT} [pF] \times V_{DD} [V] \times f_{OUT} [MHz] \times 10^{-3}$$

5041 series

DC Characteristics (5041B1B to B5B)

$V_{DD} = 1.60V$ to $2.25V$, $V_{SS} = 0V$, $T_{OPR} = -40^{\circ}C$ to $+85^{\circ}C$, $C_{LOUT} = 15pF$ unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit	
			MIN	TYP	MAX		
Operating-mode current consumption*1	I_{DD}	5041B1B ($f_{OUT} = f_{OSC}$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$, $V_{DD} = 1.8V$	–	1.7	3.4	mA	
		5041B2B ($f_{OUT} = f_{OSC}/2$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$, $V_{DD} = 1.8V$	–	1.5	3.3	mA	
		5041B3B ($f_{OUT} = f_{OSC}/4$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$, $V_{DD} = 1.8V$	–	1.4	3.2	mA	
		5041B4B ($f_{OUT} = f_{OSC}/8$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$, $V_{DD} = 1.8V$	–	1.4	3.1	mA	
		5041B5B ($f_{OUT} = f_{OSC}/16$), Measurement circuit 1, no load, INHN = HIGH, $f_{OSC} = 48MHz$, $V_{DD} = 1.8V$	–	1.3	3.1	mA	
Standby-mode current consumption	I_{ST}	Measurement circuit 1, INHN = LOW	–	–	10	μA	
HIGH-level output voltage	V_{OH}	Q pin, Measurement circuit 3, $I_{OH} = -4mA$	$V_{DD}-0.4$	–	–	V	
LOW-level output voltage	V_{OL}	Q pin, Measurement circuit 3, $I_{OL} = 4mA$	–	–	0.4	V	
Output leakage current	I_Z	Measurement circuit 4, INHN = LOW	Q = V_{DD}	–	–	10	μA
			Q = V_{SS}	–10	–	–	μA
HIGH-level input current	V_{IH}	INHN pin, Measurement circuit 5	$0.7V_{DD}$	–	–	V	
LOW-level input current	V_{IL}		–	–	$0.3V_{DD}$	V	
INHN pull-up resistance	R_{PU1}	Measurement circuit 6	INHN = V_{SS}	0.4	1.5	10	$M\Omega$
	R_{PU2}		INHN = $0.7V_{DD}$	50	100	200	$k\Omega$

*1. The consumption current I_{DD} (C_{LOUT}) with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT}) [mA] = I_{DD} [mA] + C_{LOUT} [pF] \times V_{DD} [V] \times f_{OUT} [MHz] \times 10^{-3}$$

AC Characteristics

Clock output characteristics (5041A1B to A5B, Q pin)

$V_{DD} = 2.25V$ to $3.63V$, $V_{SS} = 0V$, $T_{OPR} = -40^{\circ}C$ to $+85^{\circ}C$, $C_{LOUT} = 15pF$ unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Output rise time	t_r	Measurement circuit 1, $0.1V_{DD} \rightarrow 0.9V_{DD}$	-	-	4.5	ns
Output fall time	t_f	Measurement circuit 1, $0.9V_{DD} \rightarrow 0.1V_{DD}$	-	-	4.5	ns
Output duty cycle ^{*1}	Duty	Measurement circuit 1, threshold voltage $0.5V_{DD}$, Duty = $T_w/T \times 100$	45	50	55	%
Output enable delay time ^{*2}	t_{OE}	Measurement circuit 2 ^{*3} , INHN = LOW \rightarrow HIGH	-	-	10	μs
Output disable delay time	t_{OD}	Measurement circuit 2 ^{*3} , INHN = HIGH \rightarrow LOW	-	-	100	ns

Clock output characteristics (5041B1B to B5B, Q pin)

$V_{DD} = 1.60V$ to $2.25V$, $V_{SS} = 0V$, $T_{OPR} = -40^{\circ}C$ to $+85^{\circ}C$, $C_{LOUT} = 15pF$ unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Output rise time	t_r	Measurement circuit 1, $0.1V_{DD} \rightarrow 0.9V_{DD}$	-	-	5	ns
Output fall time	t_f	Measurement circuit 1, $0.9V_{DD} \rightarrow 0.1V_{DD}$	-	-	5	ns
Output duty cycle ^{*1}	Duty	Measurement circuit 1, threshold voltage $0.5V_{DD}$, Duty = $T_w/T \times 100$	45	50	55	%
Output enable delay time ^{*2}	t_{OE}	Measurement circuit 2 ^{*3} , INHN = LOW \rightarrow HIGH	-	-	10	μs
Output disable delay time	t_{OD}	Measurement circuit 2 ^{*3} , INHN = HIGH \rightarrow LOW	-	-	100	ns

*1. This parameter is measured using the NPC's standard crystal. Note that the values will vary with the crystal characteristics used or mounting conditions.

*2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

*3. Measurement circuit 2 takes an external input on the XT pin, without using a crystal.

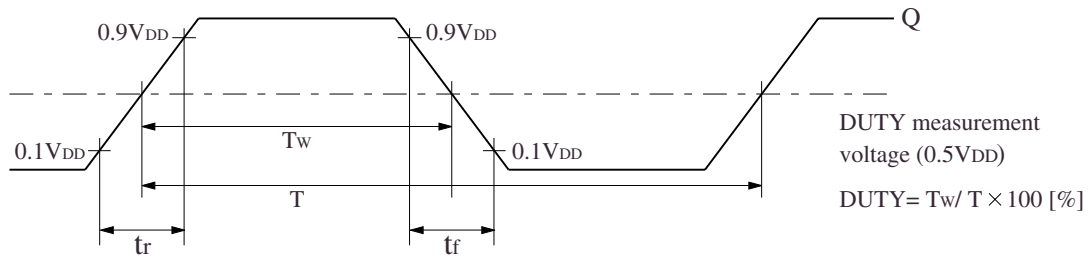


Figure 1. Output switching waveform

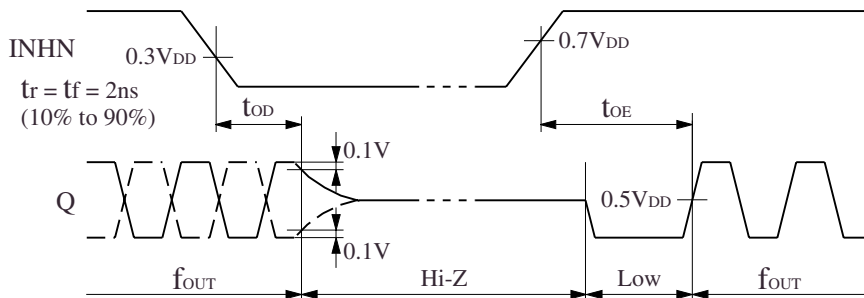
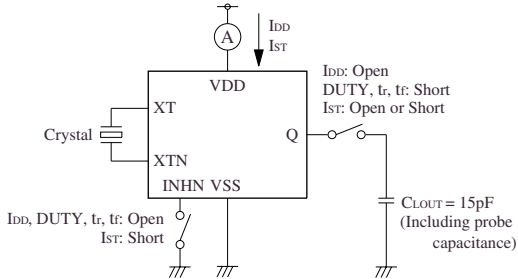


Figure 2. Output disable timing chart

MEASUREMENT CIRCUITS

Measurement Circuit 1

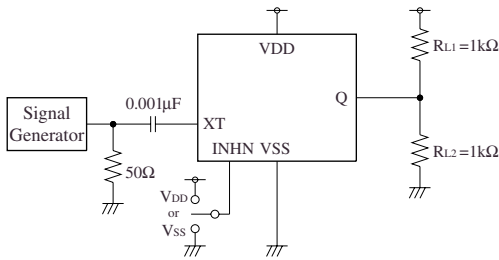
Parameters: I_{DD} , I_{ST} , Duty, t_r , t_f



Note: The AC characteristics are observed using an oscilloscope on pin Q.

Measurement Circuit 2

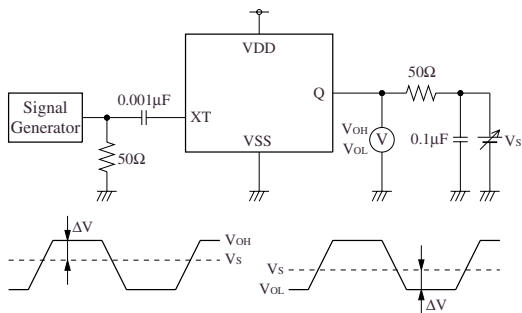
Parameters: t_{OD} , t_{OE}



XT input signal: 1Vp-p, sine wave

Measurement Circuit 3

Parameters: V_{OH} , V_{OL}



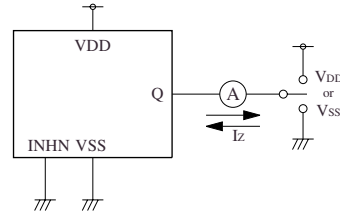
V_S adjusted such that $\Delta V = 50 \times I_{OH}$.

V_S adjusted such that $\Delta V = 50 \times I_{OL}$.

XT input signal: 1Vp-p, sine wave

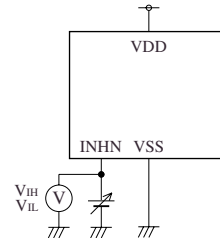
Measurement Circuit 4

Parameters: I_Z



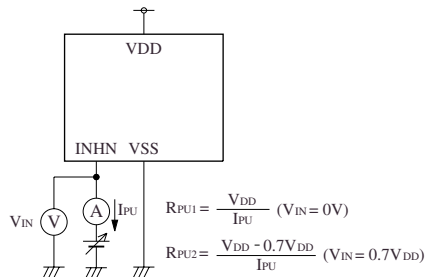
Measurement Circuit 5

Parameters: V_{IH} , V_{IL}



Measurement Circuit 6

Parameters: R_{PU1} , R_{PU2}



FUNCTIONAL DESCRIPTION

Frequency Adjustment Function

The 5041 series ICs have a built-in oscillator frequency adjustment function. The frequency adjustment settings are written to and stored in internal EEPROM, making the devices easy to setup. A typical compensation sequence is shown below.

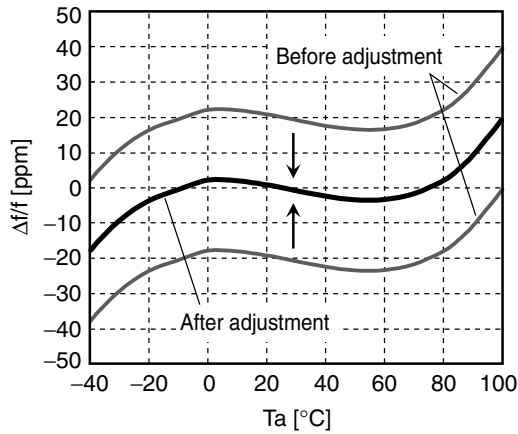


Figure 3. Center frequency adjustment

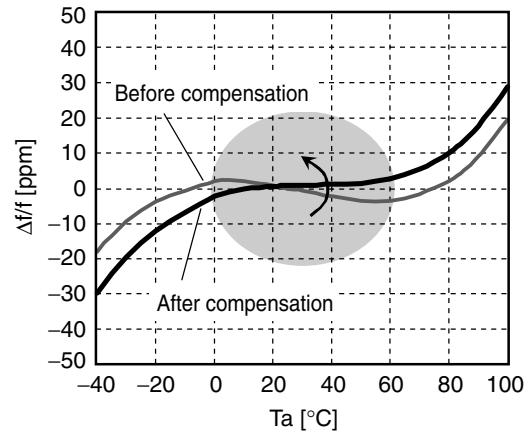


Figure 4. Temperature rotation compensation

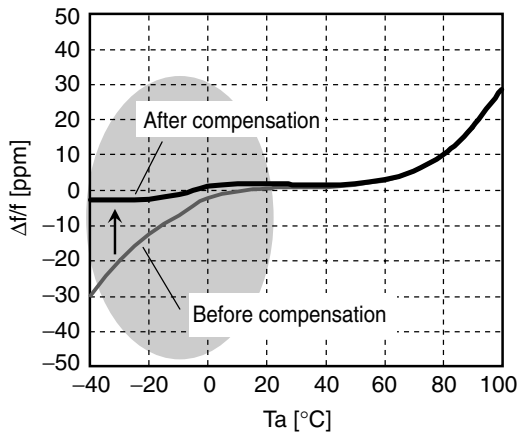


Figure 5. Low-temperature characteristics compensation

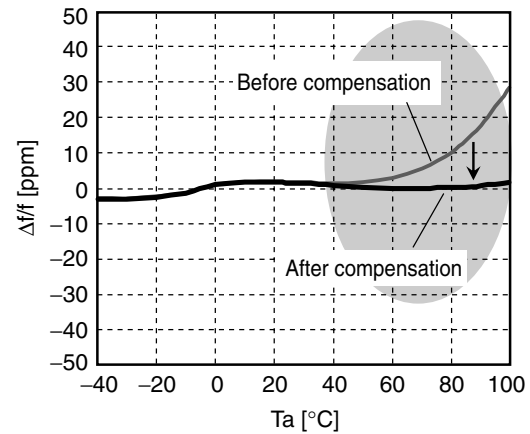


Figure 6. High-temperature characteristics compensation

Power-saving Pull-up Resistor

The INHN pin pull-up resistance R_{PU1} or R_{PU2} changes in response to the input level (open, HIGH, or LOW). When INHN is tied LOW level, the pull-up resistance is large (R_{PU1}), reducing the current consumed by the resistance. When INHN is left open circuit (HIGH), the pull-up resistance is small (R_{PU2}), which decreases the input susceptibility to external noise. The pull-up resistance ties the INHN pin HIGH level, helping to avoid problems such as the output stopping unexpectedly.

Oscillation Detector Function

The 5041 series also feature an oscillation detector circuit. This circuit functions to disable the outputs until the oscillator circuit starts and oscillation becomes stable. This alleviates the danger of abnormal oscillator output at oscillator start-up when power is applied or when INHN is switched.

USAGE NOTES

Consideration for Mounting IC

A ceramic chip capacitor that is larger than $0.01\mu\text{F}$ should be mounted proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5041 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Please pay your attention to the following points at time of using the products shown in this document.

1. The products shown in this document (hereinafter "Products") are designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools and measurement equipment. The Products are not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment. The Products are not designed and manufactured to be used for the apparatus that exerts harmful influence on the human lives due to the defects, failure or malfunction of the Products. If you wish to use the Products in that apparatus, please contact our sales section in advance.
In the event that the Products are used in such apparatus without our prior approval, we assume no responsibility whatsoever for any damages resulting from the use of that apparatus.
2. NPC reserves the right to change the specifications of the Products in order to improve the characteristics or reliability thereof.
3. The information described in this document is presented only as a guide for using the Products. No responsibility is assumed by us for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of the third parties. Then, we assume no responsibility whatsoever for any damages resulting from that infringements.
4. The constant of each circuit shown in this document is described as an example, and it is not guaranteed about its value of the mass-production products.
5. In the case of that the Products in this document falls under the foreign exchange and foreign trade control law or other applicable laws and regulations, approval of the export to be based on those laws and regulations are necessary. Customers are requested appropriately take steps to obtain required permissions or approvals form appropriate government agencies.



SEIKO NPC CORPORATION

1-9-9, Hatchobori, Chuo-ku,
Tokyo 104-0032, Japan
Telephone: +81-3-5541-6501
Facsimile: +81-3-5541-6510
<http://www.npc.co.jp/>
Email: sales@npc.co.jp